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Active Gate Drivers and Loss Modeling for the Investigation of the Controlled Shoot-through Phenomenon

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Dedicated to my family.

Sommario

L'elettronica di potenza sta diventando sempre più importante a causa della necessità di mobilità elettrica e dei sistemi altamente efficienti e affidabili necessari per combattere il cambiamento climatico. Il duplice utilizzo di convertitori elettronici di potenza come riscaldatori sarà estremamente utile.

Nel metodo dello shoot-through controllato, il cortocircuito controllato viene creato per riscaldare il dispositivo di potenza. Questo è utile per riscaldare l'intero convertitore elettronico di potenza, creando un cortocircuito controllato senza danneggiare il dispositivo. Questa tecnica è utile per utilizzare un convertitore elettronico di potenza come riscaldatore e come dispositivo di riscaldamento per misurare la resistenza nello stato on del MOSFET. Il gate driver attivo a due livelli (0, V_{gs}) proposto per la tecnica dello shoot-through controllato, invece, aveva dei limiti. Le limitazioni in termini di tensione di gate variabile, devono apportare manualmente modifiche al circuito per ottenere una tensione di gate diversa, ecc.

Le limitazioni vengono superate sviluppando tre livelli (0, V'_{gs}, V_{gs}); dove V'_{gs} è la tensione di gate dinamica compresa tra zero e V_{gs}. Il gate driver ha una tensione di gate di terzo livello variabile che può essere bassa quanto la tensione di soglia del dispositivo, il che lo rende adatto per testare i MOSFET SiC.

Il diodo Zener della serie viene utilizzato per la generazione della tensione di passaggio. L'impedenza transitoria del diodo Zener in serie influisce sulla corrente di sourcing del gate e si traduce in un profilo V_{gs} diverso rispetto a quello senza la condizione del diodo Zener in serie. Pertanto, è necessario considerare un modello di perdita che consideri l'area persa. Nel caso di un diodo Zener NO in serie, la corrente di passaggio è un'onda quadra a bassa corrente di passaggio (l'autoriscaldamento non si avvia per bassa corrente). Pertanto, è possibile utilizzare il modello diretto. Se consideriamo l'autoriscaldamento del MOSFET, la resistenza nello stato on del MOSFET cambia a causa della variazione della temperatura di giunzione causata dalla corrente di drain. La forma alterata della corrente di propagazione ei rispettivi modelli di perdita sono discussi in modo approfondito. Vengono inoltre sviluppati i modelli matematici di perdita considerando l'autoriscaldamento.

La tesi si conclude con la futura applicazione del gate driver sviluppato per la scarica attiva del condensatore del collegamento CC attraverso moduli di potenza, convertitori elettronici di potenza come riscaldatore, estrazione di parametri termosensibili generando calore a livello del die ecc.

Abstract

Power electronics is becoming more important due to the need for e-mobility and the highly efficient and reliable systems required to beat climate change. The dual use of power electronics converters as heaters will be extremely helpful.

In controlled shoot-through method, the controlled short-circuit is created to generate heat within the power electronics switches. This is helpful to heat-up complete power electronic converter, creating a controlled short circuit without damaging the device. This technique is useful for using a power electronic converter as a heater as well as a heating device in order to measure the on-state resistance of the MOSFET. The two-level (0, V_{gs}) active gate driver proposed for the controlled shoot-through technique, on the other hand, had limitations. The limitations in terms of variable gate voltage, need to manually make changes in the circuit to get different gate voltages etc.

The limitations are overridden by developing three-level (0, V'_{gs}, V_{gs}); where V'_{gs} is dynamic gate voltage in between zero to V_{gs}. The gate driver has a variable third level gate voltage that can be as low as threshold voltage of the device, making it appropriate for testing SiC MOSFETs or GaN Devices. The controlled shoot-through was invented and tested on the SiC MOSFET. Therefore, while developing three-level converter the SiC MOSFET is considered.

Traditionally, the series Zener diode is used for the generation of the shoot-through voltage. The transient impedance of the series Zener diode affects the gate sourcing current and results in a different gate voltage (V_{gs}) profile than without the series Zener diode condition. Therefore, a loss model considering lost area needs to be considered. In the case of a NO Zener diode in series, the shoot-through current is a square wave at low shoot-through current (self-heating does not start for low current). Therefore, the direct model can be used. If the self-heating of the MOSFET considered, the on-state resistance of the MOSFET changes due to the change in the junction temperature caused by drain current. The altered shape of the shoot-through current and respective loss models are discussed in-depth. The mathematical loss models considering self-heating are also developed.

The thesis concludes with the future application of the developed gate driver for active discharge of DC-link capacitor through power modules, power electronic converter as a heater, extracting thermo-sensitive parameters by generating heat at the die level etc.

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Introduction

The UN Climate Change Conference of the Parties (COP26) conducted in Glasgow in 2021 aimed to unite all nations in a single forum to fight against climate change. Its first aspiration is to assure global net zero by 2050 and keep 1.5 °C within achievable reach. Countries are being advised to come forward with challenging 2030 emissions reduction targets that coordinate with accomplishing net zero by 2050. Collective efforts by all countries are essential. Therefore, most countries have committed to their independence from fossil fuels or net-zero carbon emissions [1].

One of the main reasons behind the electrification of the transportation system is increasing environmental awareness and oil shortages. The fluctuation in oil prices also gives motivation for electrified transportation. According to the International Energy Agency (IEA), greenhouse gas emissions are expected to grow by two-fold between 2005 and 2050, necessitating major policy initiatives [2].

Power electronics is the key driving system of the present day. Therefore, efficiency and reliability directly impact the environment. With an increase in temperature, the reliability of the power device's life decreases. Active gate drivers are important parts of achieving efficiency and reliability of the power switches.

Therefore, thermal swing (also called temperature gradient) plays a vital role in the reliability of power devices. The temperature gradient decreased either by reducing the generated junction temperature or by increasing the junction temperature when power cycling is not active. In the case of lowering the temperature, generating heat is reduced in the first place. However, it is not possible in most applications due to the high demand for current. In another case, by increasing junction temperature,

the temperature gradient is reduced to avoid consequences that lead to reduced life of the power devices [3].

In the literature, many active thermal control techniques are available. This thesis focuses on improved models proposed in the controlled shoot-through-based active thermal control technique. The controlled shoot-through technique creates a short-circuit but in a controlled condition (by controlling the gate to source voltage). Along with commutation losses, the controlled shoot-through generated additive losses. These additive losses are used for active thermal control. The power semiconductor companies like Infineon®, Wolfspeed®, STMicroelectronics® etc., does not guarantee the lifetime of the power MOSFET die if operated in the short-circuit condition. Therefore, the controlled short circuit method using proposed gate driver in this thesis will enable opportunity to generate short circuit (controlled) without damaging the power die.

The conditions for the controlled shoot-through are summarized below [36]:

- Operation of the application should not affect.
- CST technique does not contribute to the load current. HS and LS MOSFETs are shorted.
- Load voltage should not change.
- DC voltage across half-bridge should not change.
- Applied shoot-through voltage should operate MOSFET in saturation mode.

There are many ways to obtain shoot-through voltage, like a PWM-controlled low dropout regulator, voltage follower circuit, etc. However, using a series Zener diode is an easier and comparable solution with existing two-level gate drivers. In the proposed controlled shoot-through technique series Zener diode is used to obtain shoot-through voltage. The transient impedance of the series Zener diode impacts the shoot-through current. Therefore in-depth analysis of the series Zener diode on loss model is required.

To avoid a series Zener diode, a dynamic gate voltage is required. Therefore, a three-level two-degree-of-freedom active gate driver has been designed and developed. Third-level refers to shoot-through voltage, which can dynamically vary from 0 to V_{gs}. The variable gate voltage is generated using a PWM-controlled low-dropout voltage regulator.

Not only the series Zener diode but also the self-heating of the MOSFET also affects the shoot-through current. Due to the high shoot-through current, the junction temperature suddenly rises. This results in a decrease in mobility for the carrier. Therefore, the increase in on-state resistance changes the shoot-through current shape (not an exact square wave as expected).

This thesis builds up an understanding of change in controlled shoot-through current shape. The self-heating phenomenon during shoot-through events is explained. The impact of self-heating on the loss model is discussed. A three-level two-degree-of-freedom active gate driver has been developed, which can generate dynamic gate voltage changes in time and amplitude. The hardware developed can be used as a test bench for testing short-circuit capability and analyzing self-heating phenomena.

Relation between chapters

Chapter 1: Explains the importance of active thermal control and various methods to achieve it. This chapter also classifies various methods depending on the implementation techniques.

Chapter 2: The controlled shoot-through techniques were proposed in 2017 [36]. To obtain shoot-through voltage, the Zener diode was used (between gate driver IC output and gate of MOSFET). However, using a series Zener diode alters the shape of the gate current. The gate driver proposed in this thesis does not need a series Zener diode to achieve variable shoot-through voltage. The use of a series zener diode is interesting from the cost point of view. Therefore, this chapter discusses the loss model with the help of the proposed gate driver and series Zener diode.

The loss model also affects due to the self-heating of the MOS devices. The

inflection point of MOSFET is discussed to know the instance when the self-heating of the device starts.

Chapter 3: This chapters explains design and development of Three-level two-degree-of-freedom active gate driver. The detailed circuit diagram and logic required are explained. The various design parameters, Low dropout regulator saturation, optocoupler non-linearity, and gate resistor power requirement are explained.

Chapter 4: The controlled short circuit current by using a Zener diode in series and the proposed gate driver are compared. The shape of the controlled short circuit current is discussed when the self-heating of the devices is avoided (assumption: heat generated at the junction immediately removed).

Discussion In the final section discusses the outcome of the research work and future work and explains possible directions and applications of the developed gate driver.

Chapter 1

State of the art in active thermal control for power electronics devices

Failure is simply the opportunity to begin again
this time more intelligently.

– Henry Ford

Wide-bandgap semiconductor materials are widely utilized in wireless charging, electric cars, and wind power production. They may be used to increase converter reliability due to their superior chemical stability and high power density. Temperature, however, has the most impact on reliability [4]. Temperature, however, has the most impact on reliability [4]. According to MILitary STandard (MIL-STD 217), behind capacitors, insulated-gate bipolar transistors (IGBTs) are the second most unreliable components causing inverter failure [5].

Junction temperature variations are The most significant factors driving SiC MOSFET aging and failure. When the temperature varies, mechanical stress between the material layers arises because copper and the ceramic of the substrate have differing

thermal expansion coefficients (CTE) as shown in Figure 1.1 [6].

The power module packaging use solder joints over wire bonds, which are more susceptible to thermal fatigue. The strain on the solder joints due to thermal cycling is given as,

$$\varepsilon = \Delta\alpha\Delta T(DNP/t) \tag{1.1}$$

Where ε is the shear strain in the solder joint, $\Delta\alpha$ is the coefficient of thermal expansion (CTE) mismatch between the die and the substrate, ΔT is maximum temperature change during a cycle, DNP is the distance of the solder joint from the neutral point of the die, and t is threshold joint stand-off height [7]. The magnitude of strain is proportional to the maximum temperature change. Therefore, active thermal control techniques become more critical for achieving reliability and longer life [7].

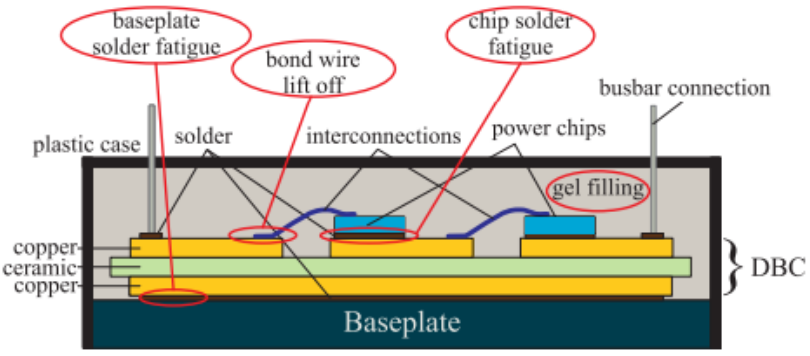


Figure 1.1: Inside structure of power electronic module.

Suppressing or smoothing down the junction temperature fluctuation is an efficient technique to increase the reliability of MOSFETs. Lower temperature swing increases the life of the power devices [3]. The concept of Active Thermal Control (ATC) is to regulate junction temperature and thermal stress [8], [9].

The ATC can be used to achieve reliability in power electronics devices. Power device thermal cycling results in package-related wear-out, including bond-wire dete-

rioration, chip metallization reconstruction, and solder fatigue [10], [11]. These result from mechanical stress between materials in contact with one another that have varying thermal expansion coefficients and thermal gradients. Life estimation of power switches is done by reducing the junction temperature swing ΔT_J [11].

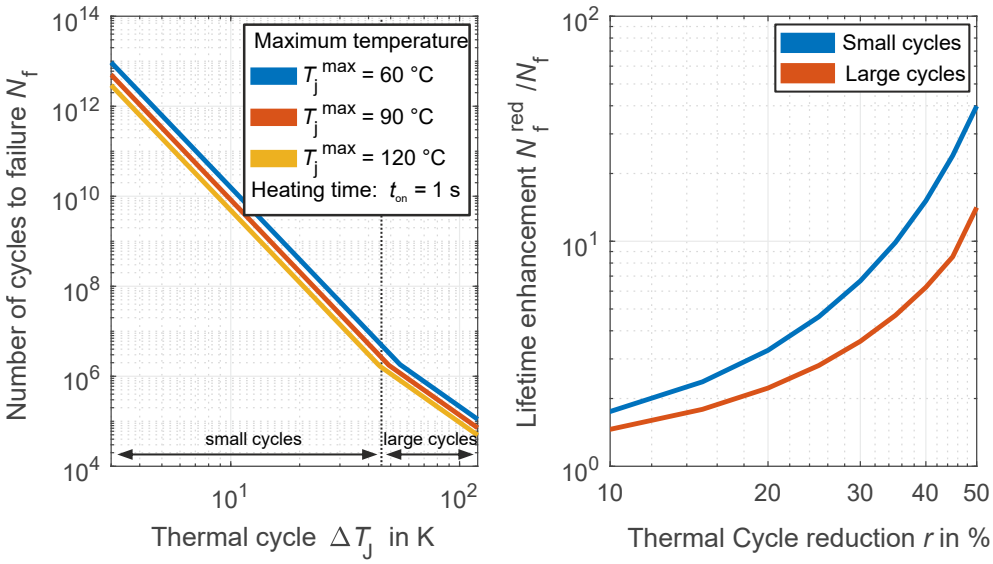


Figure 1.2: Lifetime plot of Hybridpack^{TM}2.

The active thermal control (ATC) techniques can be classified into following categories [12] as shown in Table 1.1.

The Coffin–Manson–Arrhenius model is well known for estimating power electronic switches life [13].

$$N_f = a \cdot \Delta T^{-\alpha} \cdot e^{\frac{E_a}{k_B T_{j,m}}} \tag{1.2}$$

N_f is the number of cycles to failure depending on thermal cycling magnitude ΔT and average temperature T_{jm}. The parameters a, α, and E_a extracted from the datasheet, and k_B is Boltzmann constant. From plots in Figure 1.2, the power module's life reduces with the temperature gradient increase during the cycle. Therefore, it is important to reduce the temperature gradient. For this, additive losses are required to

Active thermal control methods	
Loss manipulation	1) Varying switching frequency 2) Varying gate voltage to change $R_{ds_{on}}$ 3) Buffer capacitor 4) Switchable gate resistor array 5) Dynamic gate driving 6) Controlled shoot-through technique
Loading manipulation	1) reactive power circulation 2) voltage and current limit
Manipulation of convection interface	1) Thermo-electric cooling 2) Air and liquid 3) Liquid metal magneto-hydrodynamic pump

Table 1.1: Active thermal control methods discussed in this following sections.

introduce in addition to switching losses. In the literature, many techniques have been proposed as active thermal controls. Those techniques are discussed in the following section.

This thesis is only focused on the SiC MOSFET. This state of art chapter analyzes the active thermal control techniques for Si MOSFET, SiC MOSFET, IGBT, and GaN devices because these methods can be extended across all MOS devices.

1.1 Switching loss manipulation

Turn-on and turn-off of power switches generate switching losses, and this energy dissipates as heat in the package and heatsink. The loss manipulation can be done by increasing or decreasing the switching frequency, varying the gate to source voltage, changing the input capacitor to increase the turn-on time of the MOSFET, and changing the gate resistor. This manipulation of the loss can be used to keep a lower temperature gradient from its peak operating junction temperature. All these tech-

niques are discussed in detail in this section.

The experimental/simulation plot data shown in Figure 1.4 is extracted using WebPlotDigitizer [14] and re-plotted using MATLAB.

Varying switching frequency

The authors in [15] proposed a technique to reduce junction temperature by varying switching frequency. Power losses of the power module include loss in the die and body diode. To estimate the junction temperate, the Foster-type model is used. The junction temperature T_j compared to $T_{j_{max}}$ at a particular frequency. If T_j is more than $T_{j_{max}}$, the switching frequency reduced until T_j is less than $T_{j_{max}}$. Here $T_{j_{max}}$ means the maximum junction temperature set in the algorithm (not the absolute junction temperature specified by the manufacturer). The algorithm for this technique is presented as shown in Figure 1.3 [15].

The junction temperature is estimated as,

$$T_{j_{max}} = 2P_{av} \sum_{i=1}^{n} R_i \left(\frac{1 - e^{1/2 f_o \tau_i}}{1 - e^{1/f_o \tau_i}} \right) + T_{ref} \tag{1.3}$$

Where P_{av} is average power loss, f_o is switching frequency/output current frequency, and $\tau_i = R_i C_i$ is the time constant for the curve fitting in the Foster model.

The switching frequency is decreased if the junction temperature exceeds the specified limit. The algorithm for this technique is presented as shown in Figure 1.3 [15].

The simulation results for variable switching frequency are shown in Figure 1.4. The junction temperature keeps rising with an increase in the current. If the junction temperature exceeds the maximum junction temperature specified by the manufacturer, it can damage the power module.

There are several limitations and disadvantages associated with this technique.

- The components in the circuit like capacitors and inductors, are designed by considering specific switching frequency.

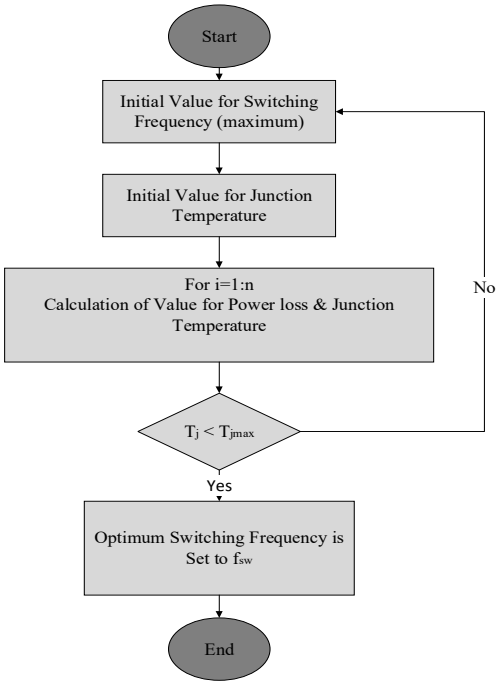


Figure 1.3: Variable switching frequency flowchart to maintain T_{jmax} within limits.

- The ripple current produce unwanted ripple in the motor torque and can cause damage to the bearings in the long term.

- The harmonic present in the load current will change with the switching frequency; therefore, EMC filters should be designed for a broad frequency range.

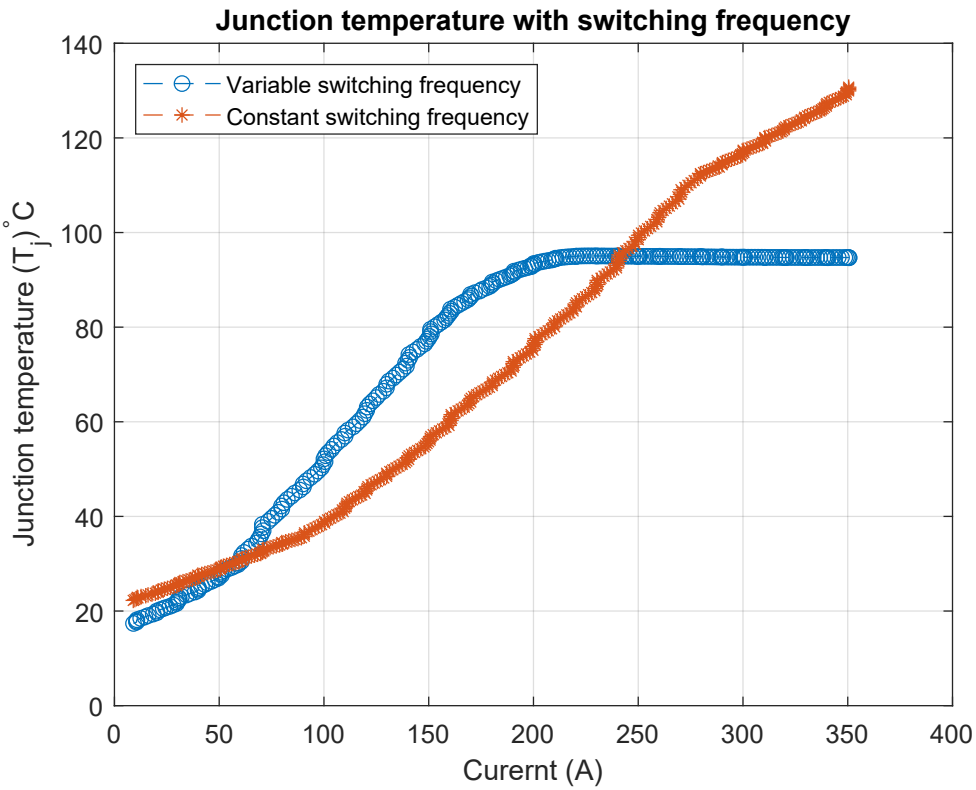


Figure 1.4: Junction temperature with constant switching frequency and variable switching frequency.

Varying gate voltage to change $R_{ds_{on}}$

The authors in [16] propose decreasing gate voltage to increase the on-state voltage to reduce the thermal swing. varying gate voltage to change on-state resistance ($R_{ds(on)}$). The buck converter with 12 V input and 6 V output with 200 kHz switching frequency is realized [16]. The gate voltage varies during the conduction phase to change the on-state resistance.

The buck converter is kept in the thermal chamber, and $R_{ds_{on}}$ is calculated for the different case temperate T_c with different V_{gs}. The look-up table of $R_{ds_{on}}$ and V_{gs} is prepared. Therefore, the buck converter is in the linear region, and the drain current is linear with V_{gs}. The on-state voltage V_{ds} is given as,

$$V_{ds} = R_{ds_{on}} I_D \tag{1.4}$$

The temperature rise is given as,

$$\Delta T = R_{TH}.P_{av} \approx R_{TH} \cdot d \cdot V_{DS} \cdot I_D \tag{1.5}$$

Where the R_{TH} is the device's thermal resistance, d is the duty cycle, and P_{av} is the average power loss. The microcontroller gate voltage for specific R_{TH} and specific temperature is achieved. To achieve ΔT temperature rise, the R_{TH} required is calculated as,

$$R_{TH} = \frac{\Delta T}{d \cdot V_{DS} \cdot I_D} \tag{1.6}$$

The selected MOSFET's $R_{ds_{on}}$ is $\approx$ 20 mΩ at room temperature and for V_{gs}= 10 V, its value can be increased above 200 mΩ if a gate voltage lower than 3 V is applied as shown in Figure 1.6. Moreover, the reduction of gate voltage is expected to increase the switching losses since the switching time increases by reducing the gate voltage. The active thermal control approach, considering an ideal power cycling effect, is illustrated in [16]. A reference temperature T_{ref} is defined, determining the minimum temperature of the device. When the temperature overcomes this value, the gate voltage is increased (to its maximum value) in order to minimize $R_{ds_{on}}$ and hence the heating. On the other hand, when the temperature tends to be lower than

the reference value, the gate voltage is reduced (to increase $R_{ds_{on}}$), allowing to keep the desired temperature. Thanks to this strategy, the ΔT swing is reduced with respect to the case of no active thermal control.

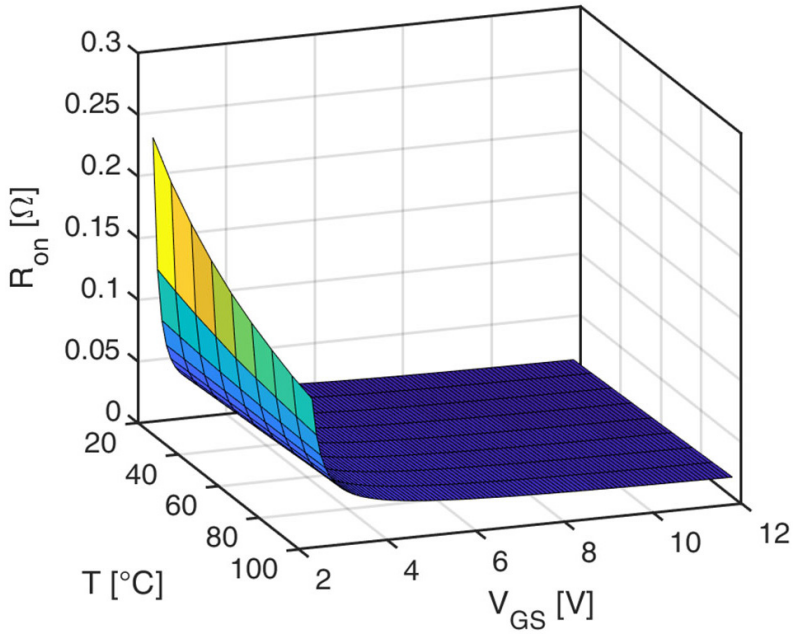


Figure 1.5: $R_{ds_{on}}$ as a function of operating temperature and gate voltage.

The experimental work conducted in [16] considers dynamic junction and case temperature same. If switching cycling has a lower time constant than the thermal time constant, the proposed method is not valid for active thermal control. Therefore, this method holds practical limitations due to such a hypothesis.

Similarly, a two-level gate driver for active thermal control of GaN devices is proposed in [7], [17]. The gate driver has two stages, as shown in Figure 1.7. However, the design and development of the gate driver are not explained in the papers [7], [17]. The proposed gate driver may be used for the active thermal control of SiC MOSFET.

The rise time and fall time can controlled by using gate driver [17]. The turn-on loss becomes,

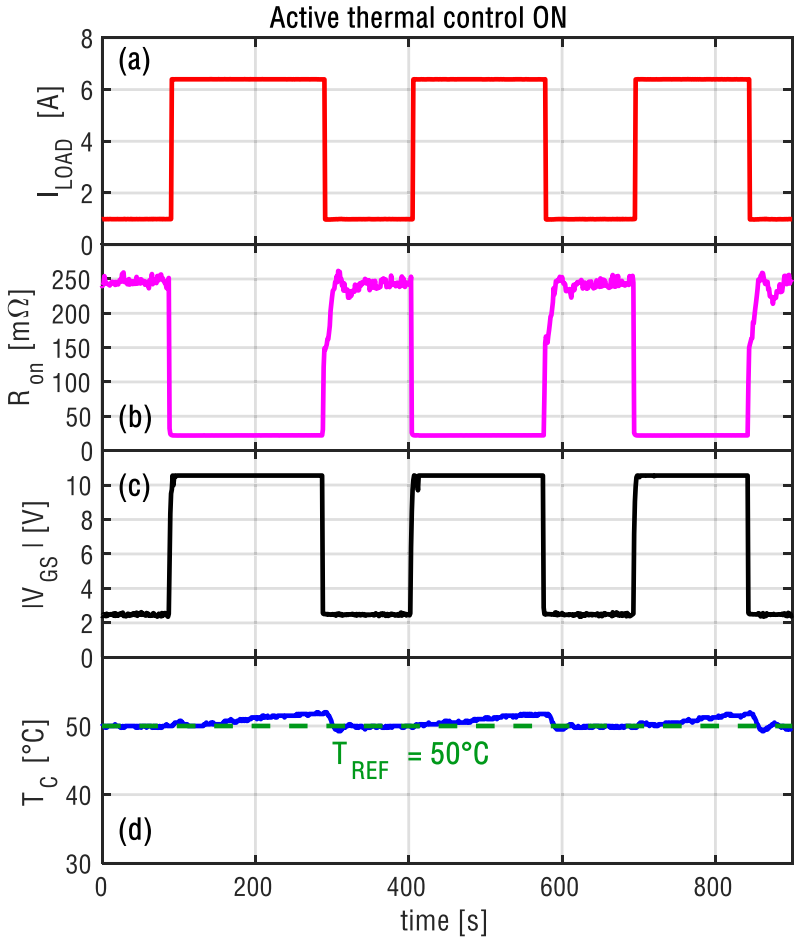


Figure 1.6: On-state resistance increase with decrease in the gate voltage. The thermal swing limited to 50 °C.

$$E_{on} = \frac{1}{2} V_{ds} I_{ds} (t_r + t_{cr}) \tag{1.7}$$

Where E_{on} is energy lost during turn-on of the device (as shown in Figure 1.8 [7]), t_r is rise-time of the device and t_{cr} is current rise time. In this case, the switching losses are controlled by varying either the device $\mathrm{d}V_{ds}/\mathrm{d}t$ (current slew rate) or (current slew rate). That is achieved by varying either device rise time t_r or drain current rise time t_{cr}.

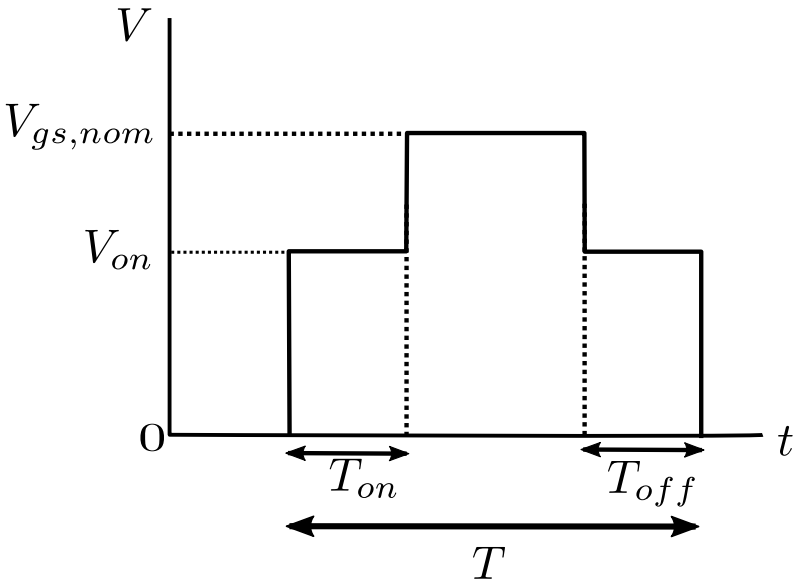


Figure 1.7: Two level gate driver to turn-on and turn-off MOSFET in two stages.

With the help of a two-level gate driver [17], the active thermal control is achieved by on-stage resistance as well as by controlling switching losses.

Buffer Capacitor

The RC snubber circuit is well-known for reducing voltage overshoot. The RC snubber circuit can also be used for an active thermal control (ATC) by a capacitor acting as an add-on capacitance to the drain-source (C_{ds}) [4]. During the OFF state of the

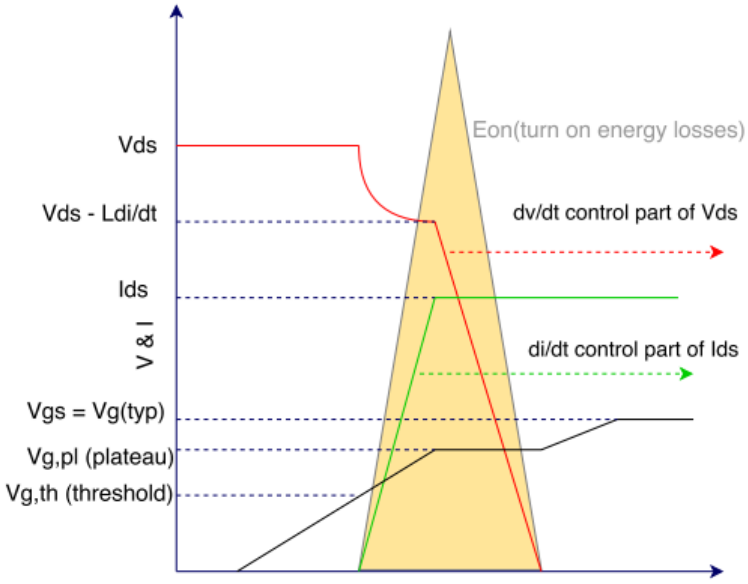


Figure 1.8: Energy lost during turn-on of WBG devices.

MOSFET, the drain current starts to drop, and the voltage across the drain to source starts to rise. By using tunable capacitance values of the RC snubber circuit, the turn-off time can be adjusted as shown in Figure 1.9 [4].

As a result, the RC buffer circuit can help lower the turn-off loss for SiC MOSFETs. The tunable capacitor is called an equivalent adjustment of buffer capacitor (EABC). The buffer circuit operates at C_{min} when the SiC MOSFET begins to switch off. The voltage curve increases slowly at T if C_{max} is connected in parallel after a delay time T through the delay switch because the buffer capacitor grows bigger to adjust the turn-off loss as shown in Figure 1.10 [4].

As a result, the delay time T may be continuously changed to control the switching loss. The swing in the junction temperature can be suppressed by adjusting the buffer capacitance. For continuous online adjustment of the capacitor, a delay switch is specifically used to modify the equivalent buffer capacitance [4].

The disadvantages of this technique are,

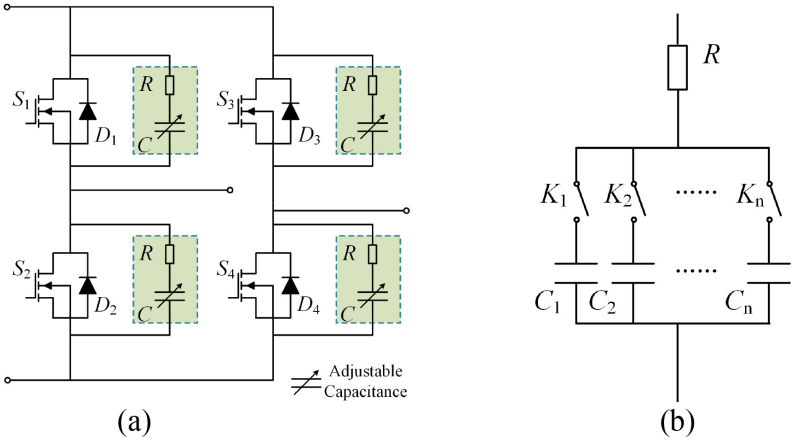


Figure 1.9: (a) System overview, (b) Capacitance adjustment.

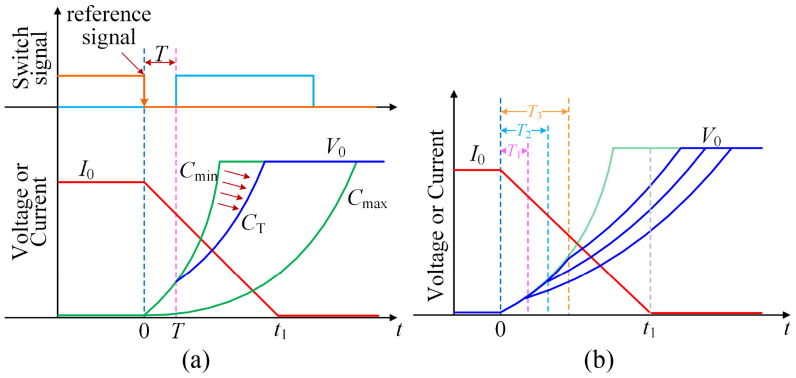
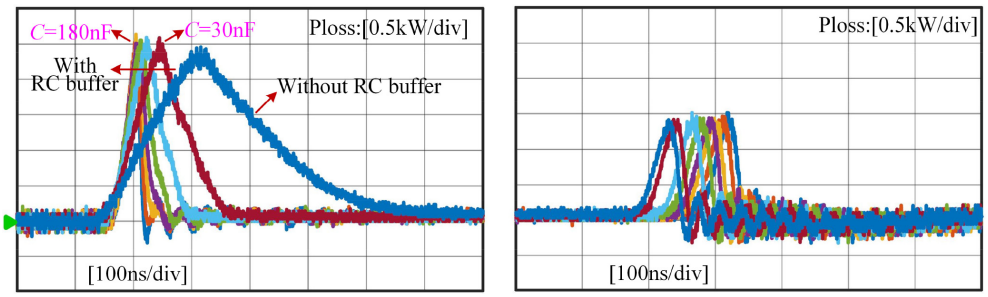


Figure 1.10: (a) Varying RC snubber's capacitance from C_{min} to C_{max}, (b) Delay in voltage rise. For logic representation only.



(a) (b)

Figure 1.11: Experimental validation for switching loss with various value of buffer capacitors. Power dissipation for (a) Turn-on stage and (b) Turn-off stage.

- If snubber capacitance is higher, the heat dissipation condition increases [4]. Instead, optimize gate loop inductance is always a better idea than placing snubber capacitor. Using a snubber circuit may require more than four layers in PCBs and decrease the converter efficiency [18].
- Depending on the capacitance inserted for the required loss, dead time must be changed dynamically. Any miscalculation of dead time leads to an uncontrolled shoot-through.

Switchable gate resistor arrays

The power cycling leads to a temperature change at the junction of power devices. The high-temperature gradient causes cracking at the bond wire [19]. To control the shape of the gate voltage and increase the reliability of power devices, the switchable gate resistor array is proposed in [13, 20–22]. The proposed method uses gate circuitry with adjustable gate resistances to increase or decrease the gate sourcing current. The gate-sourcing current controls the switching speed of the power device. This is accomplished by choosing a small, middle, and large with a high gate resistance to control the gate sourcing current. However, this technique is not practical for

parallel power switches.

$$\Delta T_j = f(V_{dc}, I_L, f_o, f_{sw}, \ V_{ge}, R_g) \tag{1.8}$$

As stated in Equation 1.8, the switching loss is function of various terms like V_{dc} DC-link voltage, I_L load current, f_o output current frequency, f_{sw} switching frequency, V_{ge} on-state gate to emitter voltage (eventually $R_{ds_{on}}$) and R_g gate resistance. The switching losses during turn-on and turn-off are adjusted by manipulating the gate resistance. However, these approaches would alter the output voltage harmonic spectrum and may affect the load current [23].

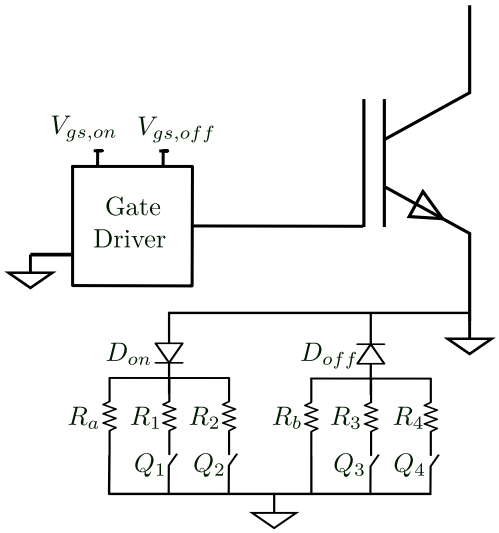


Figure 1.12: Switchable gate resistor array to control switching losses for Active Thermal Control (ATC).

Implementing gate resistor array selection for automotive and aerospace applications is challenging due to space and higher gate loop inductance. The gate loop inductance varies depending on the selection of the gate array. This should be taken into consideration in the final application. The power converter operates at ultra-high switching frequency then; there is no time to select the gate resistor array [20].

The algorithm for the switchable gate resistor array is shown in Figure 1.13. The

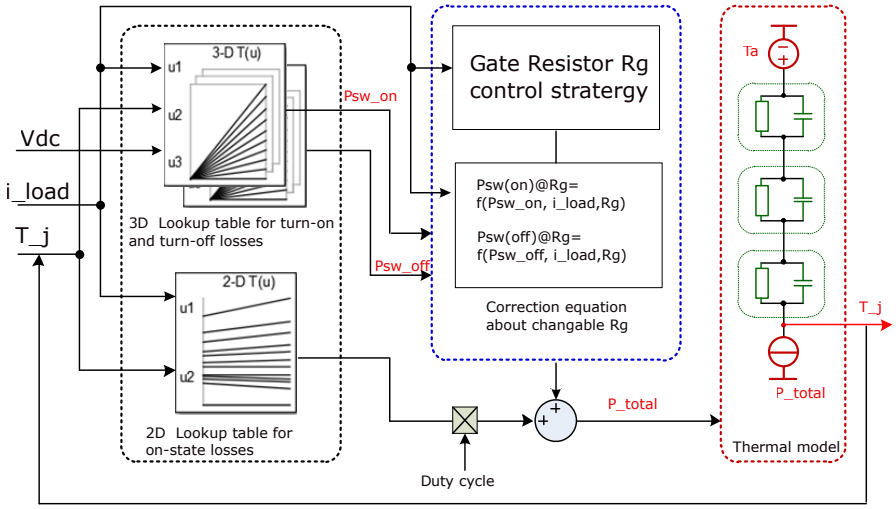


Figure 1.13: Algorithm to select equivalent gate resistance value.

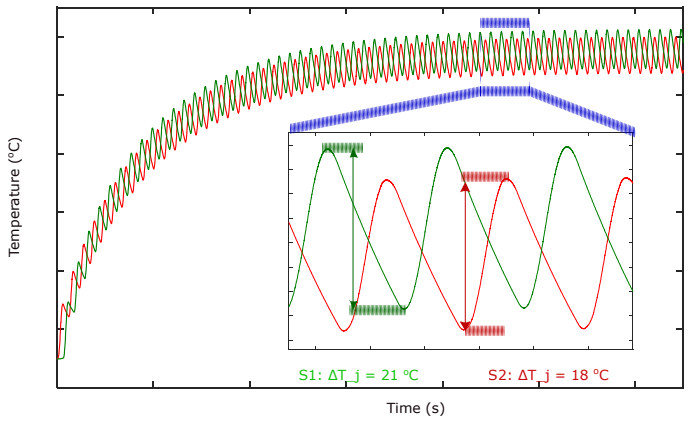


Figure 1.14: Junction temperature variation with variable gate resistor array (Red) and conventional gate driver (Green).

lookup table is set to control turn-on, turn-off, and conduction loss. The gate resistor combination is selected to control the turn-on and turn-off losses.

Dynamic gate driving

Dynamic gate driving gives control over the shape and switching timing of the power devices. Various dynamic gate-driving methods for active thermal control are discussed.

The three-level dynamic gate driver is proposed in [23], [24]. In order to quickly switch the power device, the higher gate voltage is applied (18 V) as shown in Figure 1.15. The operational amplifier-based circuit generates the dynamic voltage as shown in Figure 1.15. The detailed circuit design and implementation of dynamic gate voltage is not discussed in [23], therefore comparing it with the proposed gate driver in this thesis (Chapter 3) is not possible.

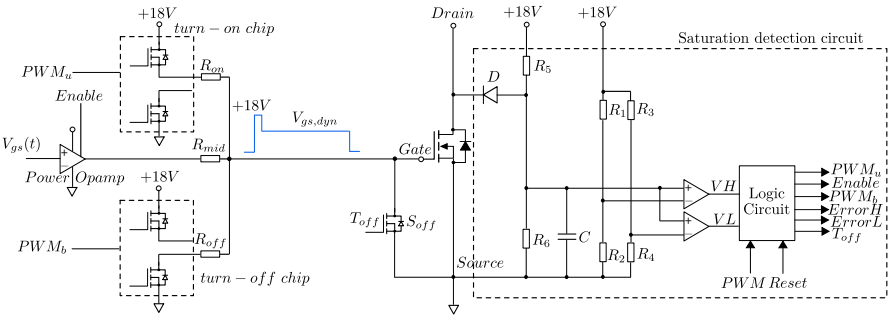


Figure 1.15: Three-level dynamic gate voltage generation using operational amplifier.

The gate output of dynamic gate voltage is shown in Figure 1.16(a). The gate driver can vary gate voltage dynamically, as shown in Figure 1.16(b). The Conduction losses can be shaped as shown in Figure 1.16(c); P_{ref} and P_{dyn} are conduction losses with traditional two-level gate driver and three-level gate driver, respectively [23]. The junction temperature swing is lowered by 3 K as shown in Figure 1.16(e) and (f).

The dynamic gate voltage is used to drive the gate of the power device to maintain consistent conduction losses [23]. The detailed time-instances for turn-off of the 18 V is not discussed. Higher gate voltage at the instance of peak drain current can cause ringing in the drain current due to high $\frac{di_{drain}}{dt}$ [25].

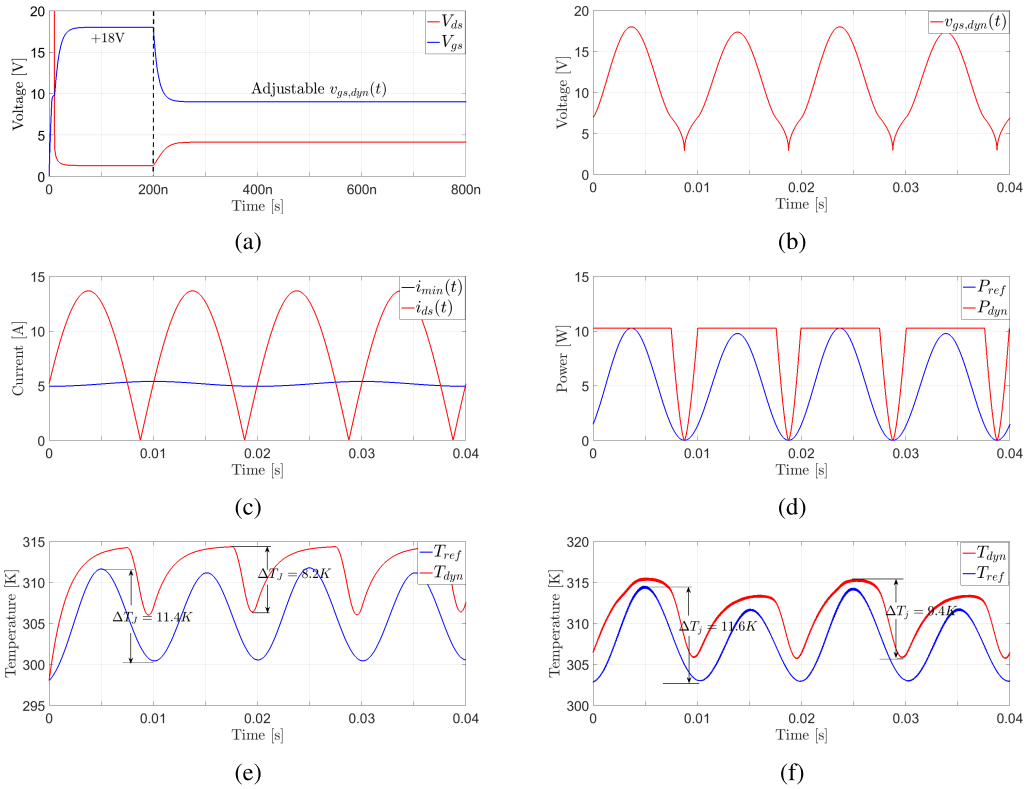
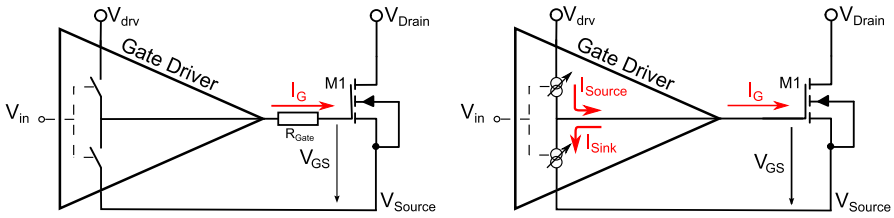


Figure 1.16: : (a) Three-level gate signal, (b) Dynamic gate voltage $V_{gs,dyn}$ waveform, (c) Drain-source current $i_{ds(t)}$ (t) and minimum current $i_{min(t)}$, (d) Conduction losses waveform, (e) Junction temperature response from analytical model, (f) Junction temperature response from equivalent circuit model (ECM).

Adaptive current source gate driver

The voltage source gate driver gives constant or variable gate voltage across the gate of the power switch. A gate resistor controls the gate charging current. In the current source gate driver, the constant or adaptive gate current is used to charge the gate capacitance. The symbolic representation of the voltage-controlled gate driver and current-controlled gate driver is shown in Figure 1.17.



(a) Hard switching gate driver (b) Current source gate driver

Figure 1.17: Voltage Source Gate Driver Vs. Current Source Gate Driver.

The current source gate driver enables possibility to change the slew rate [26], [27]. The authors in [26] proposed current source gate driver. The current source gate drivers reduce turn-on and turn-off delay times by approximately 57% and 33%. Voltage spikes and drain current oscillations [28], [29]. The adaptive current control active gate driver reduces the overshoot voltages until 28.2% and until 31.6% of the current peak. The reduction of the overshoots leads to total switching losses until about 53.3% less than conventional gate drivers with high gate resistance fixed [26]. The slew rate control also helps in controlling the radiated emissions [30] as well as reduced filter size [26].

The adaptive gate driver is designed in [26] as shown in Figure 1.18.

The two energy-storing elements are added in the convention current controlled gate driver named L_H and L_L. The Q_{aux} allows the second gate current injection and sinking. This gate driver has three characteristics: Variable $\frac{di_d}{dt}$ and $\frac{dV_{ds}}{dt}$ by varying I_m, Independent control of $\frac{di_d}{dt}$ and $\frac{dV_{ds}}{dt}$ and reduction of turn-on and turn-off times.

The authors in [25] used current source gate driver to control the di/dt and dv/dt. From Figure 1.19, it can be stated that the current source gate driver controls the

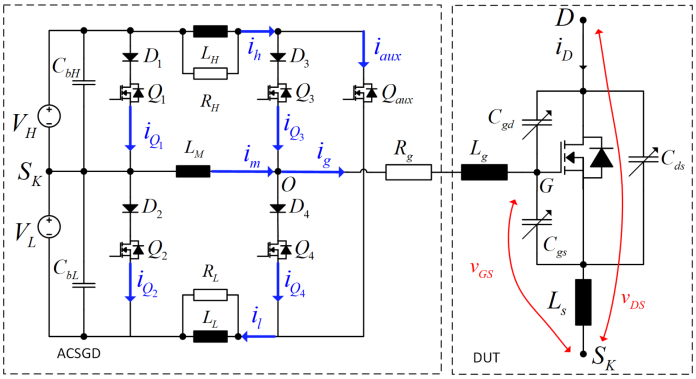


Figure 1.18: Circuit schematic for adaptive current source gate driver.

rise and fall time of drain current and voltage. Therefore radiated emission can be minimized.

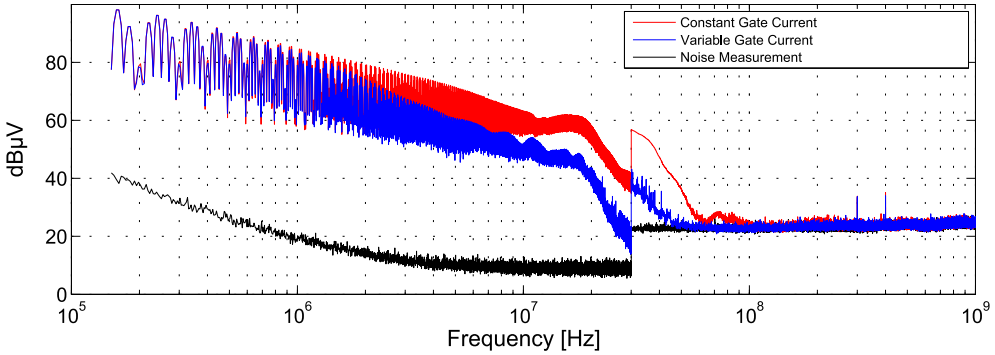


Figure 1.19: EMC measurement with low gate current in the voltage and the current transition.

The adaptive current source gate driver is more efficient than voltage controlled gate driver [31]. In case of voltage controlled gate driver, the energy is lost in the gate resistors. In the case of an adaptive current source gate driver, the current is controlled; therefore, there is no need to use gate resistors which also saves on the Bill of Material (BoM) cost. This helps in optimizing the gate loop inductance and eventually less switching losses [32].

In this paragraph, the commercial current source gate drivers are discussed. Due to precise gate current control, many companies are introducing commercial current source gate drivers. Infineon® introduced current source gate driver IC '1EDS20I12SV' which The current source gate driver uses an external current sense resistor to track the turn-on instance of the MOS Devices [30]. In 1EDS20I12SV, 11 gate current settings can be selected by applying specific analog voltage on the logic side of the gate driver IC. Similarly, the ROHM® also introduced current source gate driver IC BM60059FV-C, which can program gate current using reference voltage and external resistor. The gate drivers can be programmed with specific gate current for different gate turn-on and turn-off regions [33]. The BOSCH® introduced current source gate driver IC EG120®, which can be programmed with up to 133 different gate current profiles for charging and discharging of the power transistors [34].

Controlled shoot-through technique

An uncontrolled short circuit happens when high-side (HS) and low-side (LS) power electronics switches are on at the same time. The unintentional short circuit may cause due to the absence of dead time, false turn-on, etc. However, the authors in [35] proposed a "controlled shoot-through (CST)" technique. When the HS MOSFET is ON, the LS MOSFET is turned on at the midpoint of the HS PWM signal with a lower gate voltage, as shown in Fig 1.20. The LS gate voltage is lower than the HS gate voltage. In this way, the MOSFET will operate in a saturation region as a function of gate voltage (V_{gs}).

The shoot-through current shape is not a square wave as shown in Figure 1.21 [35]. Therefore, the area lost should be considered in the model. In addition, energy lost during the fall time of the controlled shoot-through can also be evaluated. However, this area can be neglected due to the lower fall time of the current.

The different models are presented by the authors for the calculation of the energy lost [36].

1. Direct Model:

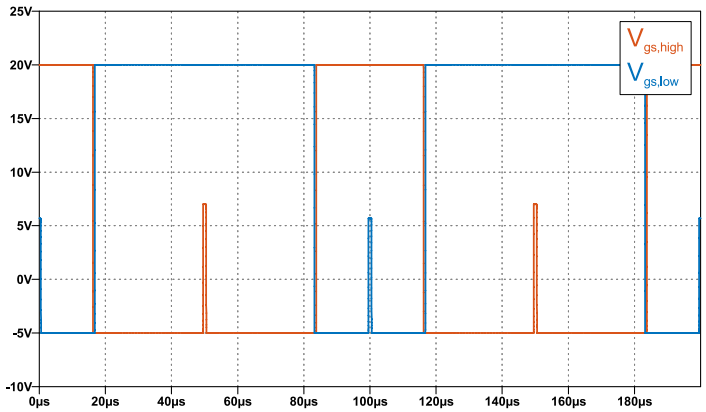


Figure 1.20: Controlled shoot-through technique.

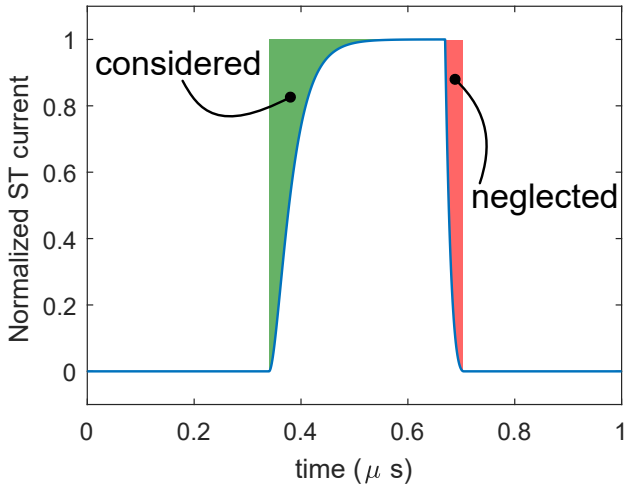


Figure 1.21: Area lost and neglected for controlled shoot-through current.

$$Est,H = (V_{dc} - V_o) \cdot I_{st} t_{st} \tag{1.9}$$

$$Est, L = V_o I_{st} t_{st} \tag{1.10}$$

2. Non-linear effects representation:

   The energy lost during shoot-through (ST) even is given as (Green area in Figure 1.21),

$$E_{st} = \int_0^{t_{st}} V_{dc} I_{st} dt \tag{1.11}$$

$$E_{st} = V_{dc} I_{st} t_{st} \left[1 - \frac{\tau}{t_{st}} (1 - e^{\frac{-t_{st}}{\tau}}) \right] \tag{1.12}$$

3. Inverse model:

$$P_{st} = E_{st} f_c = V_{dc} I_{st0} f_c \tau (x - 1 + e^{-x}) \tag{1.13}$$

Where $x = t_{st}.\tau$ normalized shoot-through time, along with active thermal control of power electronic switches, this technique is also used for online measurement of on-state resistance $R_{ds_{on}}$[37] and using power electronic converter as a heater [38–40]. A. Soldati [35, 38–40] invented the controlled shoot-through technique . One of this thesis's objectives is to develop an active gate driver for controlled shoot-through operation.

1.2 Loading manipulation

Reactive power circulation

The variation in the wind leads to a change in power generation. This results in stress on the power electronics converters. The excitation can increase or decrease the reactive power generation. The reactive power can result in the heating of the power electronics switches. This approach can is used in [41] for actively controlling the junction temperature of power electronics switches of three-level neutral point

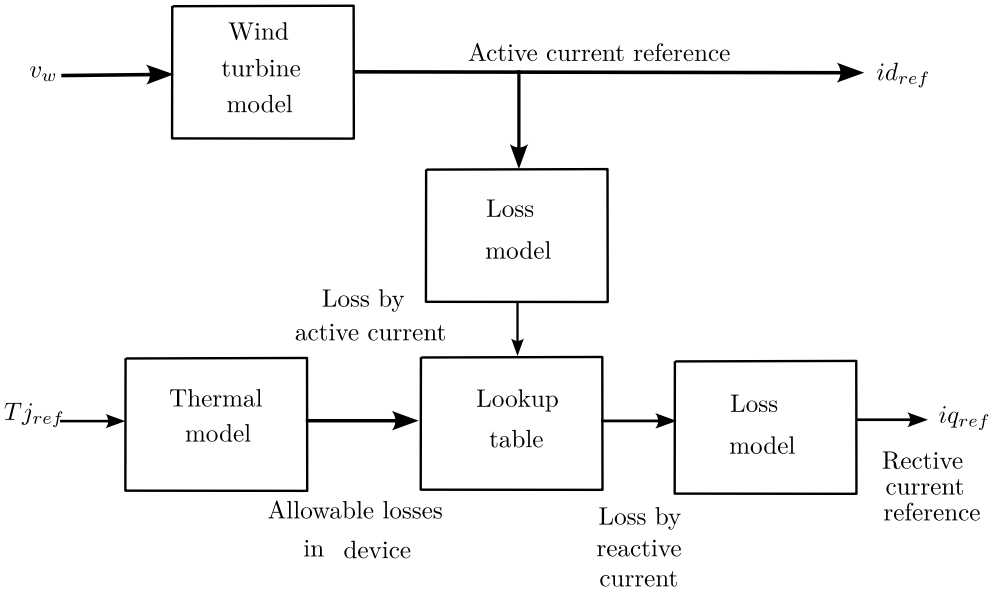


Figure 1.22: Controlling reactive power to reduce thermal cycling.

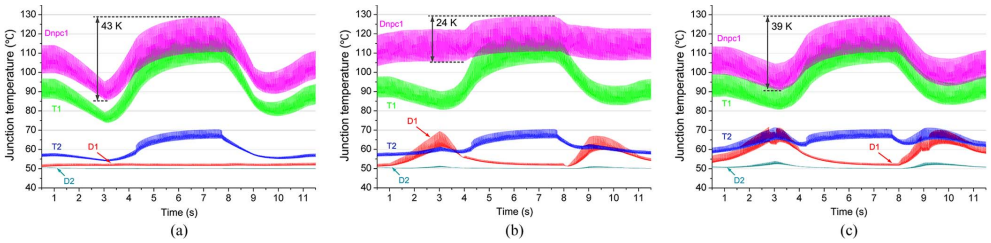


Figure 1.23: Thermal cycling of 3L-NPC inverter during wind gust. (a) Without reactive power; (b) With under-excited reactive power; (c) With overexcited reactive power.

clamped multi-megawatt inverter. The control system for the said system is shown in Figure 1.22.

From Figure 1.23, during low gust speed, the junction temperature swing increase by 43 K and by injecting reactive power the junction temperature reduced to 24 K and 39 K with under-excitation and over-excitation respectively [41]. Therefore by

implementing reactive power injection, the reliability of the power switches can be increased.

Load current limitation for active thermal control

The limitation on the voltage and current directly results in reduced switching loss. The applications that include temporarily high torque in a short amount of time result in a withdrawal of a high current. This results in high thermal cycling during the startup of the driver and can reduce the life of the power electronic switches. The authors in [6, 42, 43] propose maximum current limitation using field oriented control (FOC).

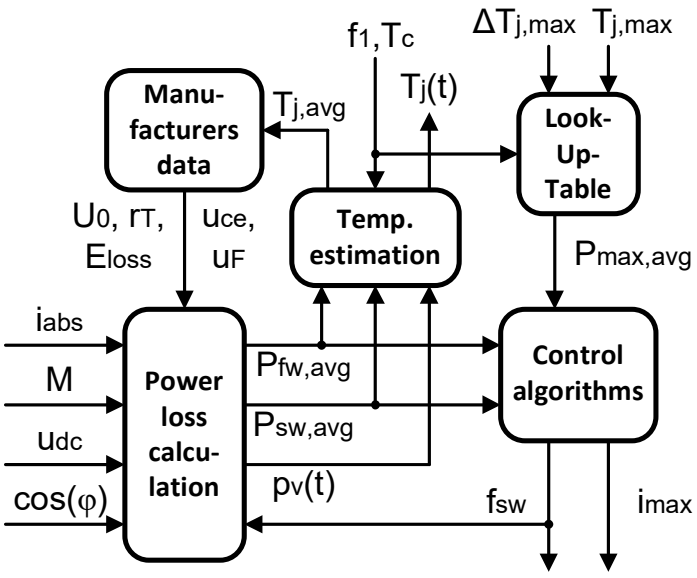


Figure 1.24: Limiting load current during peak current requirement.

The algorithm for controlling junction temperature by limiting load current and switching frequency is shown in Figure 1.24.

From Figure 1.25, the [42], the load current is limited for the active thermal control of the power module. Therefore, the thermal swing from 105 °C to 90 °C.

In many applications, peak power is a mandatory requirement to complete the

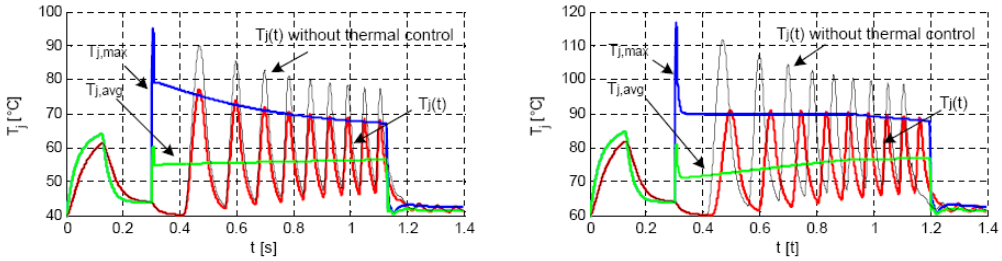


Figure 1.25: Simulation results of a startup process with (a) $T_c = 40\,^{\circ}\mathrm{C}$ (b) $T_c = 60\,^{\circ}\mathrm{C}$.

task (EVs and railways). Therefore, limiting current during peak power requirements may affect the complete operation of the system. As a result, applying this active thermal control in the EV and railways is impossible.

1.3 Manipulation of the convection interface

Thermo-electric Cooling

Forced air/liquid cooling, heat pipes, synthetic jets, and other regularly used classical cooling techniques can partially fulfill cooling needs but have several drawbacks, including large size, vibration, acoustic noise, slower reaction times, and challenging temperature management [44]. Thermoelectric cooling (TEC) differs from those conventional cooling techniques in several ways, including compact size, quick dynamic reaction due to TEC device's reduced physical size when compared to other cooling devices, no vibrations, no moving parts, and accurate temperature control of up to +/-0.01 °C as shown in Figure 1.26 [45]. There are some advantages to using TEC in power electronics as follows:

- Rapid and precise management of the power electronics equipment's base temperature.
- Having a base temperature that is lower than the ambient temperature.

Thermoelectric models for various circuits have been published on the power

electronics circuit side to analyze thermal performance and system reliability [46–49]. TECs must disperse heat created by the semiconductor chip as well as heat generated by its own power; nevertheless, their heat dissipation performance is limited [50].

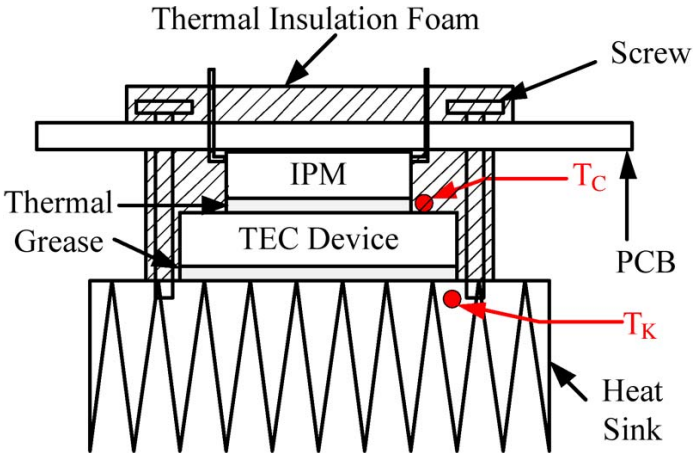


Figure 1.26: Water cooling for IGBT press pack.

Air and liquid cooling

The state space-based fan control system is used for the active thermal control of the MOSFET [51]. This is a traditional method to control the case temperature of the MOSFET with the help of a heat sink, as shown in Figure 1.27 [52]. The shape of the heat sink is optimized for heat exchange with ambient as shown in Figure 1.27.

For high power density power electronic converters, liquid cooling is used [52] as shown in Figure 1.29 [53]. Recently Danfoss® introduced half-bridge power module DCM™1000 with brand name "ShowerPower" as shown in Figure 1.30 [54].

Advantages of DCM™1000 power module are as follows [55], [56],

- Homogeneously cool large flat base-plate power modules due to swirl effect as shown in Figure 1.31(b).
- No TIM-related pump-out and dry-out effects.

- Very low differential pressure drop.

- Compact, low weight.

Liquid metal magneto-hydrodynamic pump

The adaptive heat sink is designed to compensate for variations in the case temperature of the IGBT. The adaptive heat sink is made up of actively controlled liquid metal (eutectic alloy $Ga_{68}In_{22}Sn_{10}$ (68% Ga, 22% In and 10% Sn)). The pump is used to circulate molten metal around the junction of the IGBT. The feedback of the junction temperature is taken in order to regulate the coolant rate of flow as shown in Figure 1.32 [57]. The water-filled heat exchanger is used to extract heat from the liquid metal. The water chiller is used to cool the water as shown in Figure 1.33 [57]. The disadvantage of this system is that it becomes bulky because of the additional components required to cool the metal liquid. The metal liquid is cooled using water, which is cooled using a water chiller as shown in Figure 1.33. This results in the application of this technique in limited areas.

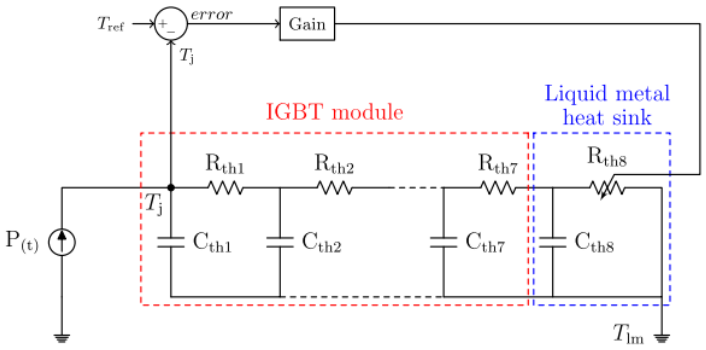


Figure 1.32: Control system for adaptive heat sink using Magnetohydrodynamic pump [40].

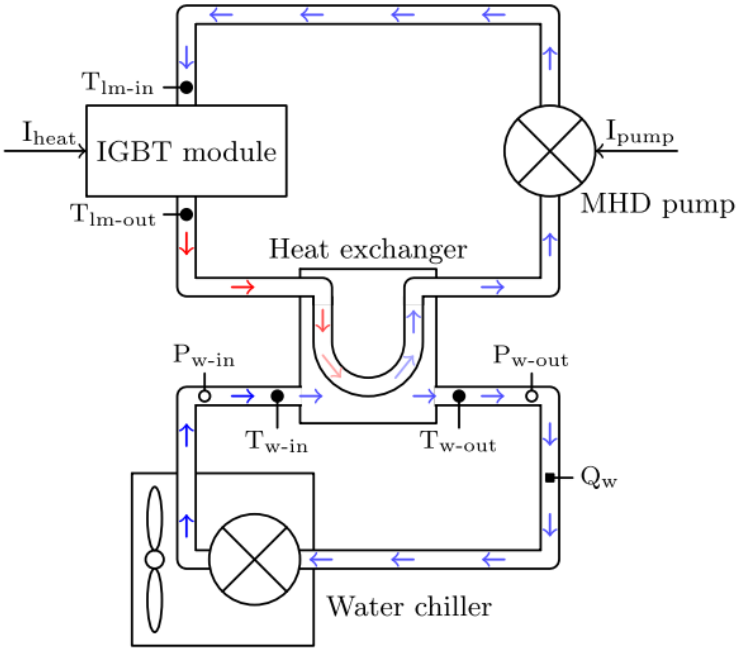


Figure 1.33: Block diagram of Magnetohydrodynamic pump for junction temperature control of IGBT.

1.4 Comparison of active thermal control methods

Active thermal control approaches are categorized into three groups based on switching loss control, loading manipulation, and convection interface manipulation, as explained in Table 1.2. Because no additional hardware is required, the techniques provided under switching loss manipulation may be widely applied in industrial applications. External hardware and space are required for loading manipulation and convection interface manipulation techniques. Loading manipulation is less practical than switching loss manipulation. The manipulation of the convection interface needs extra circuitry, although it is helpful for special-purpose applications requiring extremely high current. This technique is capable of being applied to chip-level active

thermal control. As a result, the switching loss manipulation approach is suitable for industrial applications, but the manipulation of the convection surface is suitable for special-purpose applications.

Classification	ATC technique	Remark
Loss manipulation	Varying switching frequency	Reducing switching frequency when load requirement is high reduces junction temperature. A ripple in the torque can occur.
	Varying $R_{ds(on)}$	The on-state resistance of the MOSFET decreased by decreasing gate voltage [16]. Another gate driver proposed in [17] varies gate voltage and switching losses to achieve active thermal control. Designed for GaN, and it can be implemented for other MOS devices.
	Buffer capacitor	RC snubber capacitor used. The selection of capacitor array. Reduces ringing in the drain current, but efficiency is a concern [18].
	Switchable gate resistor array	A switchable gate resistor array is used to manipulate the gate current. The changes in the gate current lead to changes in the turn-on and turn-off speed. The external circuit is required around the gate driver.
	Dynamic gate driving	Gate voltage varies to change the rise time and fall time of the drain current. This helps to reduce switching losses and reduction in the junction temperature swing [23]. The dynamic gate driving is also used to improve EMC performance [25].
	Controlled shoot-through	A controlled short-circuit is created, and the device is heated using a short-circuit current. The third-level gate voltage is required. The third-level gate voltage varied manually with the help of a series zener diode [35].
Loading manipulation	Reactive power circulation	Injection of reactive power in the low wind gust will reduce stress on the power modules. Increase in the reliability of the power devices.
	Load current limit	Limiting current during peak current requirement will reduce swing in the junction temperature. The implementation may be complex because the peak current requirement is from the system requirement for its operation.
Convection surface manipulation	Thermo-electric cooling	No moving part. Rapid management of the temperature. The base-plate temperature can be lower than ambient.
	Air and liquid cooling	The fins-based heat sink is the most common example of an air-cooled power module. Liquid cooling is used for high-power or high-power density applications like Automotive. Commercially available Danfoss® DCM™1000 power module discussed.
	Magneto-hydrodynamic pump	Magneto-hydrodynamic pump used liquid metal (eutectic alloy $Ga_{68}In_{22}Sn_{10}$ (68% Ga, 22% In and 10% Sn)). Liquid metal passes through the base plate of the power module, and a heat exchanger is used to regulate the temperature of liquid metal.

Table 1.2: Summary of active thermal control techniques.

1.5 State of the art on third-level gate voltage generation

The third-level gate voltage generation stage is proposed in this thesis. State of the art on this topic is covered to compare existing third-level gate voltage with the proposed in this thesis.

Dynamic gate voltage generation is essential in implementing a multi-level gate driver. This section discusses different dynamic gate voltage generation schemes. Authors in [23], proposed dynamic gate driver for the active thermal control of the power devices as discussed in Section 1.1. However, the detailed implementation of it is not discussed in the paper.

The authors in [58] and [59] proposed multi-level active gate driver as shown in Figure 1.34.

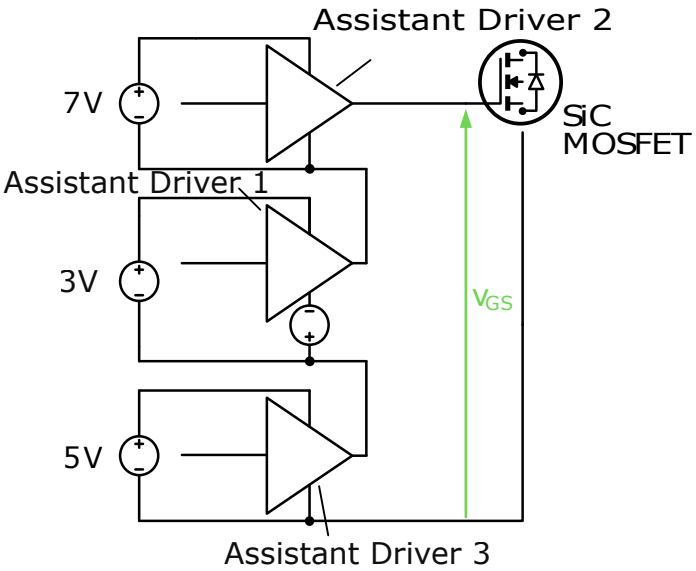


Figure 1.34: Multiple stages of voltages used for multi-level gate driver

The combination of different voltages is selected based on the requirement. The output of all three stages combined to fully turn-on the semiconductor switch. The space and cost required to implement this gate driver take almost three times more

than the convention gate driver.

In [60], the manually LDO-controlled gate driver is proposed as shown in Figure 1.35 and Figure 1.36. Manually changing the third-level gate voltage is not a feasible solution.

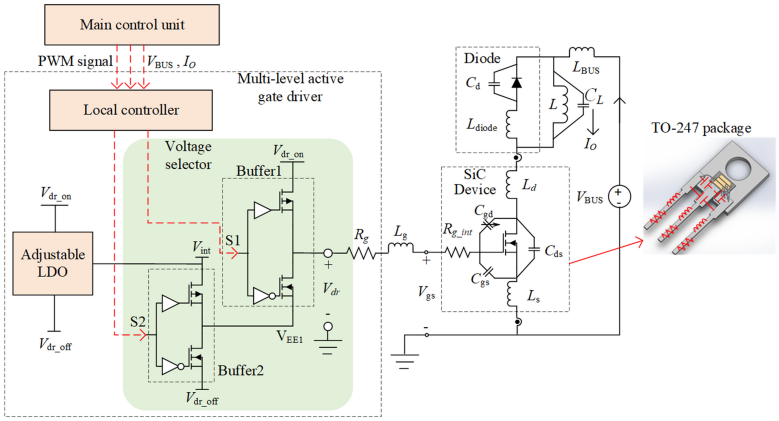


Figure 1.35: Manual adjustable LDO used to generate third-level dynamic gate voltage

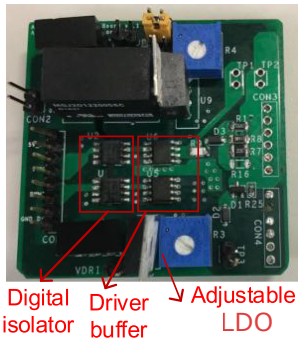


Figure 1.36: Realized gate driver showing manually changing third-level gate voltage.

In [61], the voltage-injection gate driver is proposed as shown in Figure 1.37. The V_{cc} is applied to turn-on, and the voltage injection circuit is used to generate a high voltage during the turn-off to slow down the falling rate of gate voltage. The circuit

consists of compactors and is controlled by external control signals.

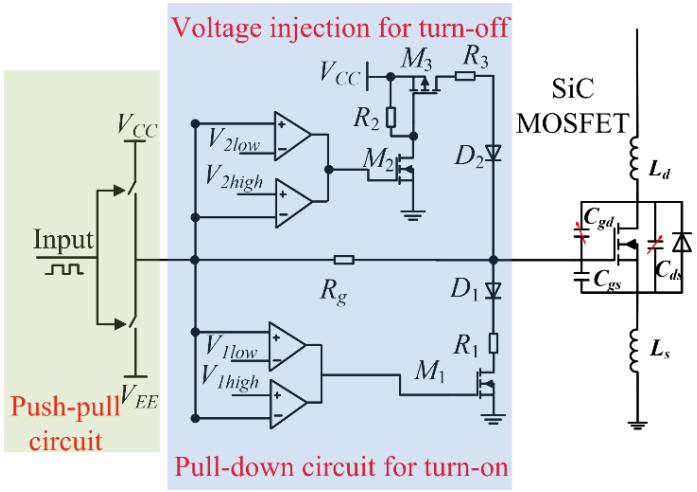


Figure 1.37: Voltage injection gate driver.

In this thesis, the third-level gate voltage (dynamic gate or shoot-through voltage) is achieved using PWM-controlled LDO. The conventional gate driver can also be converted into a multi-level gate driver using this technique, provided that LDO is used to supply the gate driver IC (Vcc). Therefore proposed third-level voltage generation circuit may have industrial applicability.

1.6 Summary

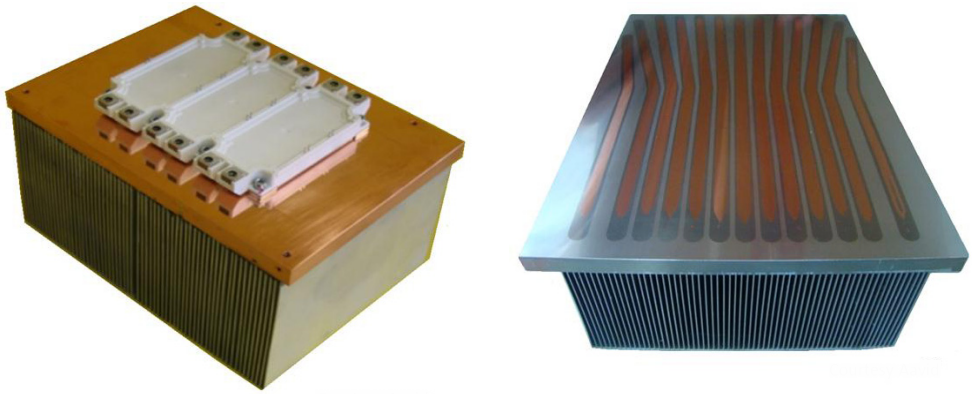
The introduction section gives a brief overview of the need for a special gate driver for the controlled shoot-through application. The introduction section also describes the flow of the thesis and the relations among chapters.

Chapter 1 starts with the various active thermal control methods for the reliability of the power semiconductor switches. Active thermal methods are broadly categorized into three sections loss manipulation, loading manipulation, and convection interface. The detailed methods proposed in these three categories are discussed in depth.

Technique	Implementation	Fine control	Bill of Material (BOM)
Gate driver assistant	Multiple gate assistants are used to achieve different stages in gate voltage. Fine control of the gate driver is not possible.	No	$$$
Manual LDO control	Manually changed the output of LDO. The manual interference does not allow fine-tuning during the operation of the gate driver.	No	$
Voltage injection	Voltage injection to manipulate turn-off gate voltage	No	$$ $
PWM controlled LDO (Proposed in this thesis)	PWM-controlled LDO allows dynamic change of gate voltage. Easy to implement in existing gate driver power supply circuit. Fine-tuning during the operation of the gate driver is possible.	Yes	$$

Table 1.3: Summary of Third level gate voltage generation techniques.
$$ represents more Bill of Material (BOM) cost than $. This is for relative cost comparison only.

The state-of-the-art third-level gate voltage generation is also proposed as this thesis proposes a new circuit for the dynamic gate voltage. The comparison of the dynamic gate voltage method proposed in this thesis is compared with other techniques. From Table 1.3, the proposed method has superior gate voltage control than other techniques.



(a) (b)

Figure 1.27: Air cooled power module (a) heat sink with multiple fins (b) heatsink with modified heat sink for better performance.

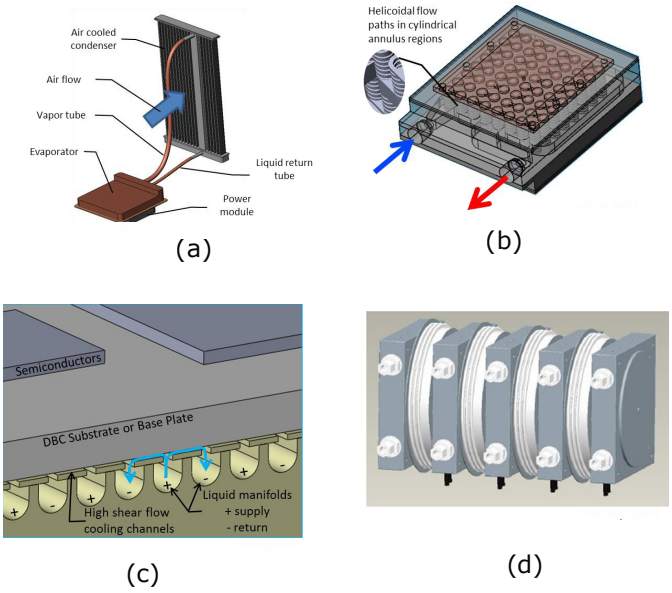


Figure 1.28: (a) Radiator based liquid cooling, (b) Helicoidal flow based cylindrical annulus heat sink for better performance, (c) Multichannel flow below Direct Bond Copper substrate, (d) Liquid cooling of diode for very high power application like hydro and wind power generation.

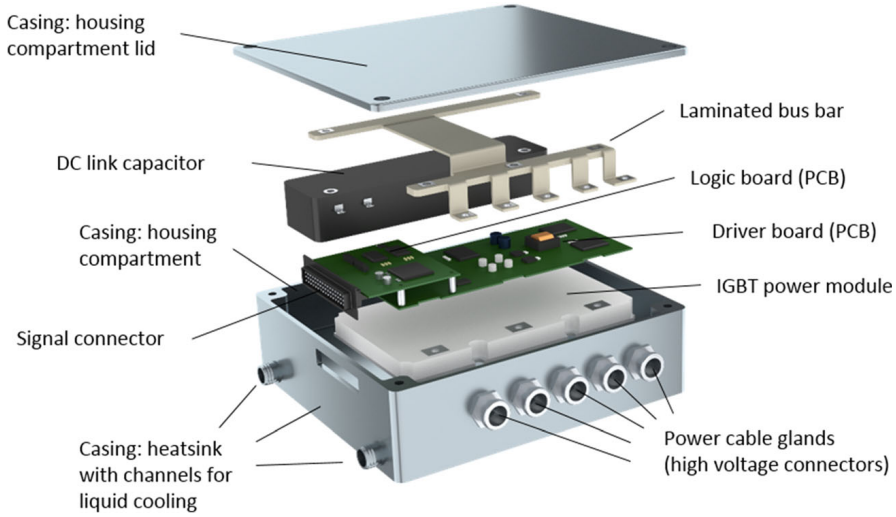


Figure 1.29: Liquid cooling of power electronic converter.

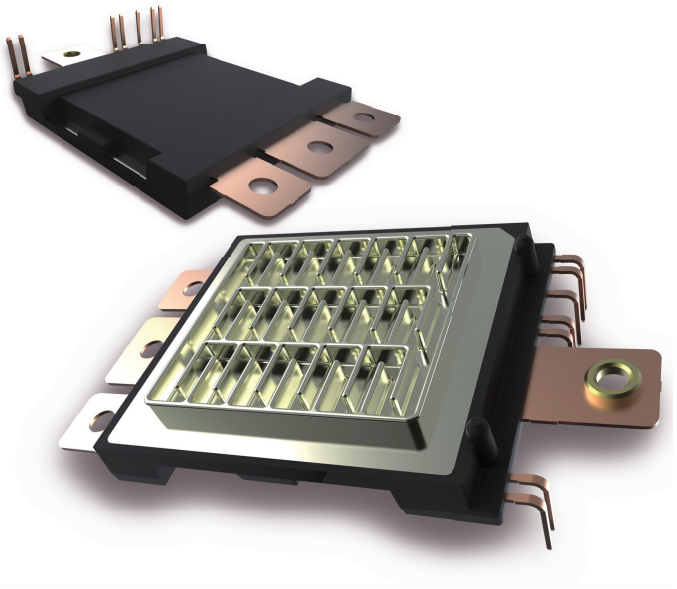
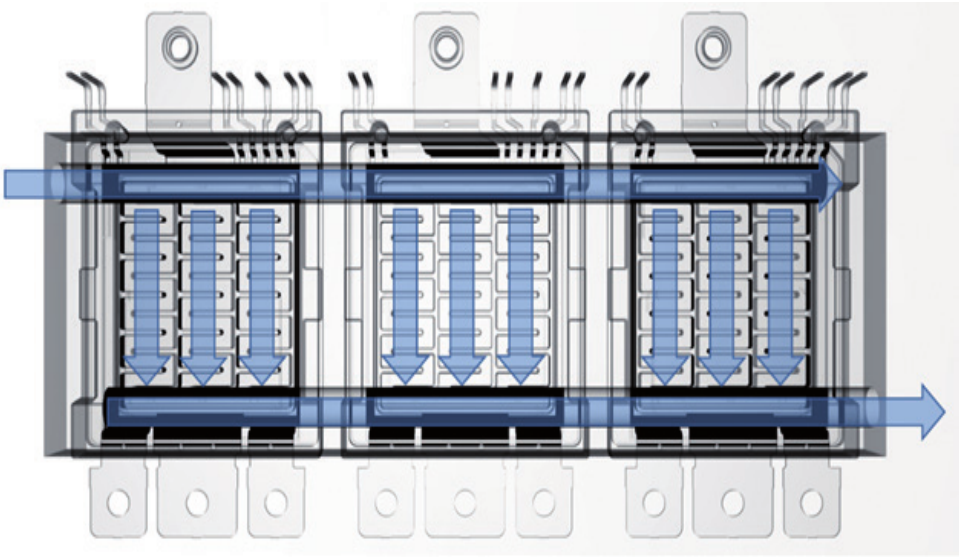
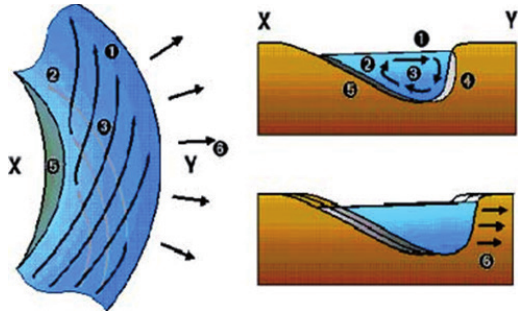


Figure 1.30: DCM™1000 power module for Next Generation Automotive Traction inverter based on Swirl Effect by Danfoss® [54].



(a)



(b)

Figure 1.31: (a) Parallel flow of the coolant, (b) Swirl effect in river

Chapter 2

Controlled Shoot Through (CST) based loss modeling considering zener impedance and self-heating of MOSFET

Great dreams of great dreamers are always transcended.

– Dr. A. P. J. Abdul Kalam

Active thermal control is an important method to extend the life of the power electronic converter, as explained in Chapter 1. The controlled shoot-through technique has many advantages like precise junction temperature using controlled shoot-through current, online measurement of on-state resistance $R_{ds_{on}}$ and using a power electronic converter as a heater [36]. In [36], the shoot-through pulse generated using a Zener diode in series with the gate driver as shown in Figure 2.1 [36, 62].

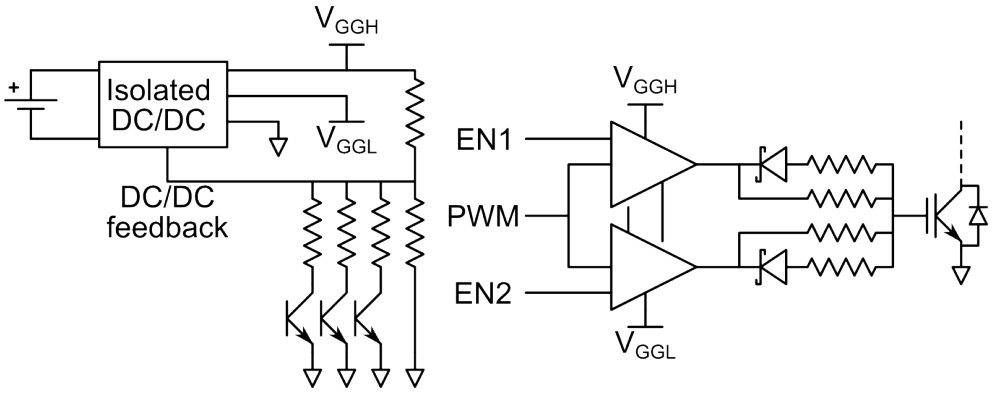


Figure 2.1: Hardware architecture of two-level gate driver [22].

To vary the gate voltage (also named as shoot-through voltage), the Zener diode is used. Let's take an example: Maximum gate voltage is 15V, to generate 8V shoot-through voltage the 5V zener diode is used in series (15 V-5 V=8 V). To achieve different shoot-through voltages, each time zener diode needs to be changed manually. Generating precise shoot-through voltage is difficult with this method.

The purpose of this chapter is to analyze the effect of a series zener diode on the controlled short circuit current and changes in the loss model. The self-heating of MOSFET also has an effect on the shape of the current. At the end of the chapter, the loss model is developed by considering self-heating the MOSFET. The inflection point indicates the start of the self-heating; therefore, details of it are also discussed.

2.0.1 Transient impedance of series Zener diode

The "transient impedance" of the Zener diode is defined as the instantaneous ratio of Voltage across the Zener diode divided by current through the diode (V_z/I_z). The unit of the ratio is Ohm (Ω).

The transient impedance in series with the gate driver can alter the shape of the gate voltage (V_{gs}) and result in a change in the drain current (I_d). Therefore, the direct loss model can not be used as specified in section 1.1. This is because of the series Zener diode's transient (dynamic) impedance. The transient impedance of the

series Zener diode decreases with an increase in the Zener current till a specific Zener voltage. The Figure 2.2 shows Zener transient impedance with different Zener voltages. The transient impedance of a 3 V Zener diode is relatively high. In contrast, the transient impedance of a 7.5 V Zener diode is the lowest [63].

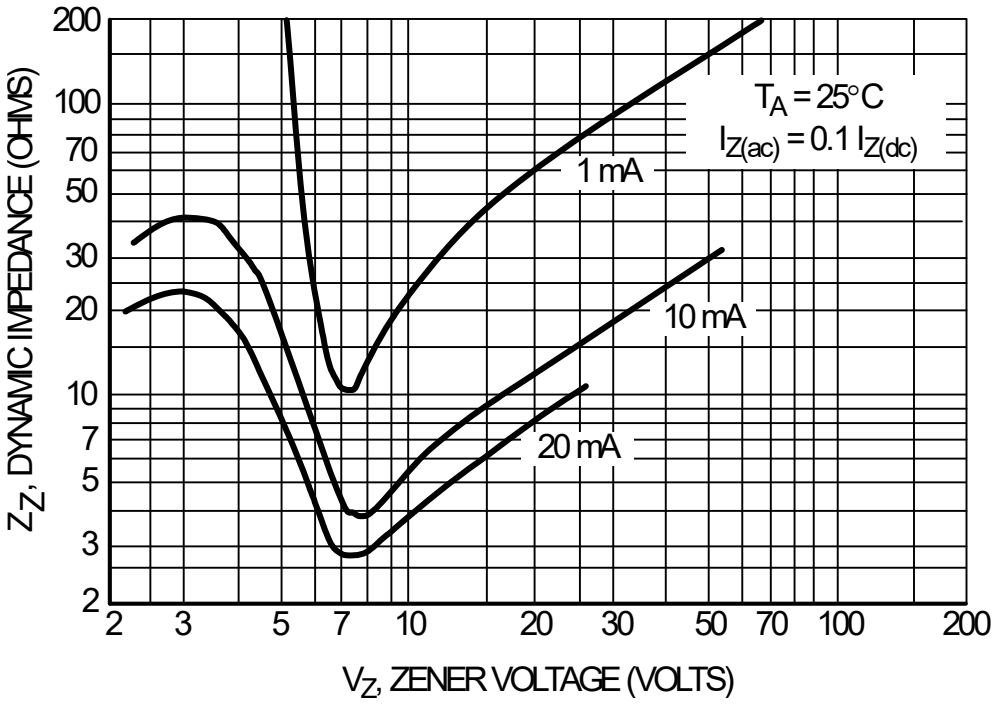


Figure 2.2: Transient impedance of Zener diode with different Zener voltages.

Let us consider V_z as the knee voltage, and V_{zk} is the rated voltage. The current at those respective voltages are I_z and I_{zk} operating and regions are shown in Figure 2.3. The transient impedance (Z_z) between these two points is given as,

$$Z_z = \frac{\Delta V}{\Delta I} \tag{2.1}$$

The transient impedance in terms of knee voltage and rated voltage is given as,

$$Z_z = \frac{V_z - V_{zk}}{I_z - I_{zk}} \tag{2.2}$$

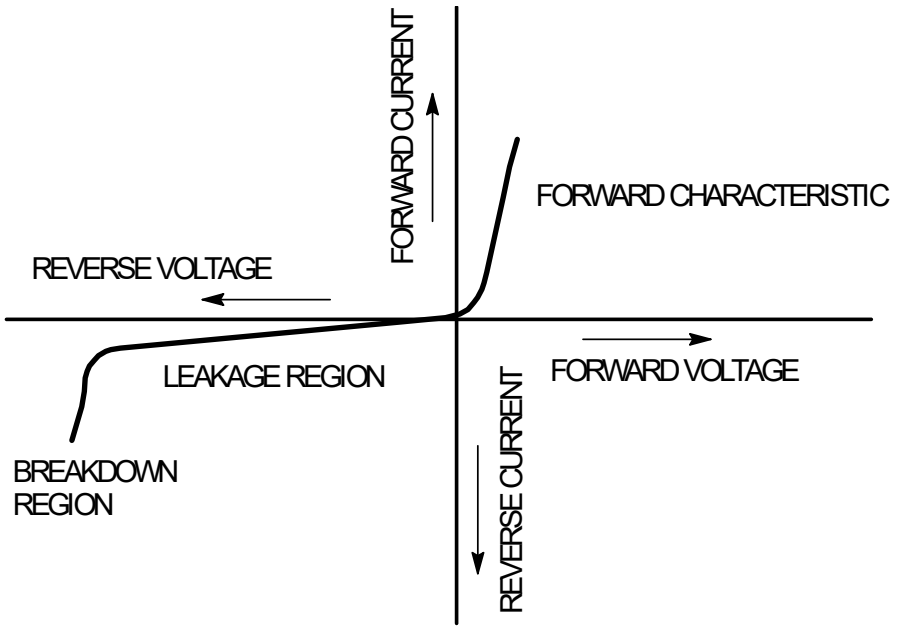


Figure 2.3: V-I characteristics of Zener diode.

Transient impedance of Zener diode and altered MOSFET transfer characteristics

The gate capacitance plays a vital role in the turn-on of the MOSFET. Drain current starts when$V_{gs} > V_{th}$. The drain current reaches its peak, and the drain to source voltage starts to drop. During the miller plateau, the drain current rises, and the drain-to-source voltage drops to on-state voltage. The gate capacitance Vs. gate voltage is shown in Figure 2.7 and Figure 2.4.

The charging time of a gate capacitance depends on gate current,

$$I_g = \frac{V_{gs}}{R_{path}} e^{\frac{-t}{\tau_{path}}} \tag{2.3}$$

Where I_g is gate sourcing current, R_{path} is the impedance of the path from the gate driver output pin (including internal gate resistance of the gate of the MOSFET), and τ_{path} is the time constant of the path $R_{path}C_{gs,gd,ds}$.

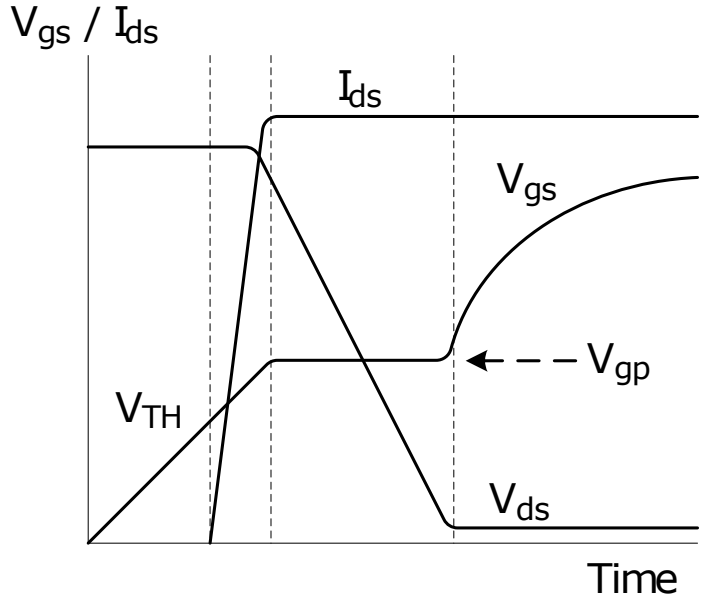


Figure 2.4: Turn-on transient of the MOSFET

From Equation 2.3, the gate-to-source voltage depends on the gate-sourcing current. Therefore, the impedance between the gate driver IC and the gate of the MOSFET affect the gate sourcing current. To achieve the third level (shoot-through voltage), the series Zener diode is used as shown in Figure 2.1 [36, 62] and discussed shortly in the introduction of this chapter. The resistors exhibit a linear relationship between voltage and current. However, the transient impedance of the Zener diode alters the shape of gate current.

Zener diode effect on the switching speed of the MOSFET

The circuit diagram and simulation for the analysis of the effect of Zener diode on the switching speed done as shown in Figure 2.5 and Figure 2.6 respectively. The rise time in the case of the series Zener diode is approx. 0.25 µs. However, without a series zener diode, the rise time is approx 0.03 µs. It is also interesting to know that the gate voltage does not reach its peak (4.88 V) due to the impedance of the zener

diode. The results are summarized in Table 2.1. The Zener impedance effect on the drain current is discussed in the next paragraphs.

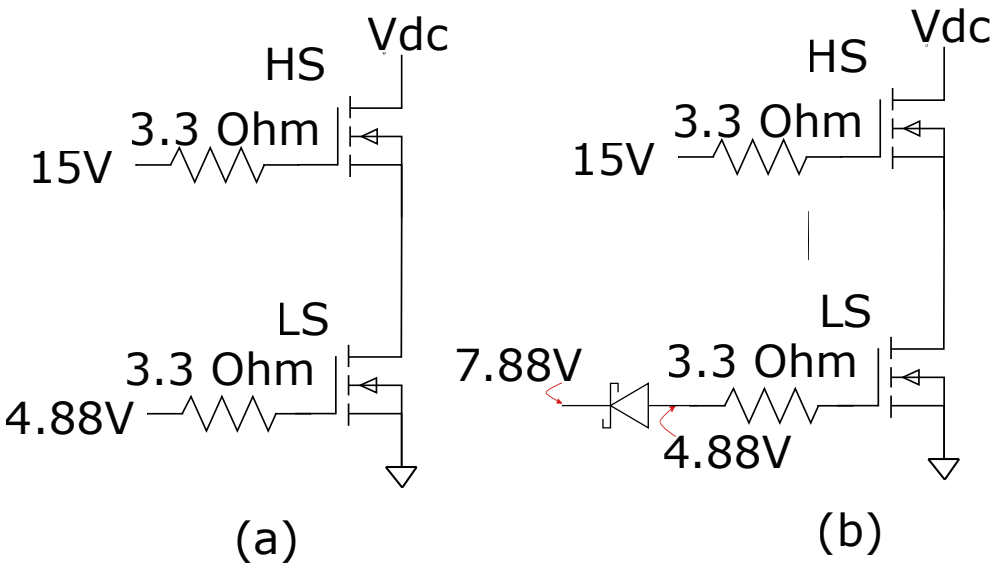


Figure 2.5: Circuit diagram to evaluate switching speed with Zener diode in series(Vzener=3V, Manufacturer part number: DIODES Incorporates® BZX84C3V0-7-F), and Wolfspeed® C2M0080120D.

Item	Case a: Without zener diode	Case b: With Zener diode	Remark
V_{gs} peak	4 V	4.88 V	-
I_g	0.12 A	0.33 A	Higher I_g in case b
Idrain-st-peak	0.8 A	2.8 A	Higher I_{st} in case b
I_{st}	0.2 µs	0.03 µs	Fast turn on in case b
I_{st} fall time time	0.15 µs	0.04 µs	fast turn off in case b

Table 2.1: Summary of simulation as shown in Figure 2.6 at F_s= 10 kHz.

The transient impedance (Z_z) of the Zener diode is not constant and varies depending on Zener voltage V_z as shown in Figure 2.2. From Equation 2.3, the gate

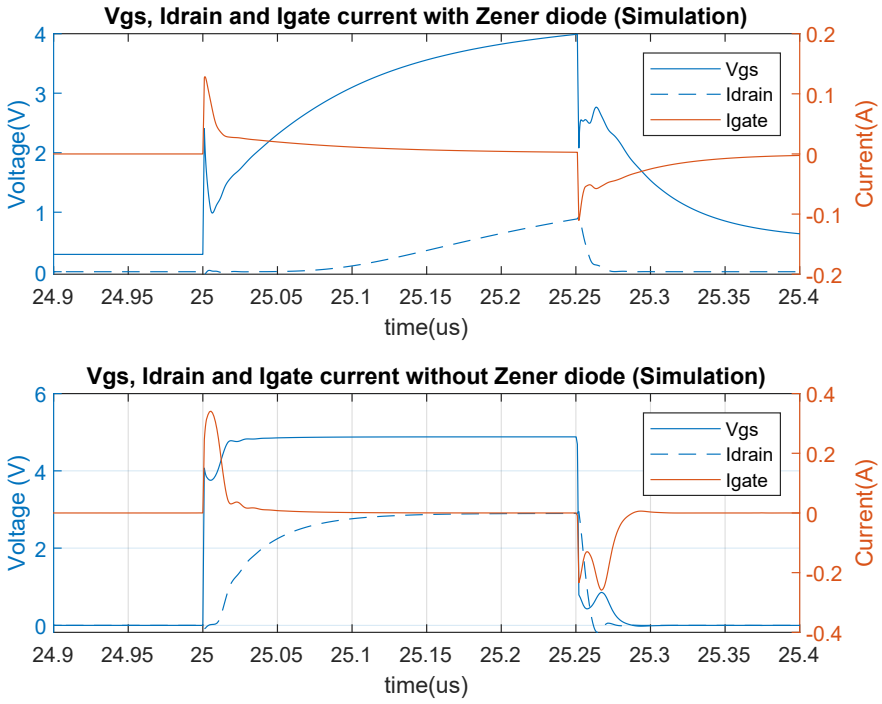


Figure 2.6: Zener diode effect on the switching speed of the MOSFET (Fs=10kHz,Rg=3.3 ohm)

sourcing current is affected by the transient impedance of the Zener diode. Due to gate voltage dependability on gate current, the shape of the gate voltage V_{gs} also alters. The drain current is a function of the gate voltage. Therefore, the transient impedance of the series Zener diode eventually alters the drain current. Results for the transient impedance of series Zener diodes are shown in Figure 2.9. The experimental results for controlled shoot-through using series Zener diodes are post-processed in MATLAB. The script is written for the processing given in Appendix B.1.

The Zener diode's transient impedance restricts the gate current, altering the shape of the CST pulse. As a result, it is critical to determine the highest allowed transient impedance of the Zener diode that does not disrupt the shape of the CST pulse.

The circuit diagram from the calculation of the transient impedance of the Zener diode is shown in Figure 2.8. The gate sourcing current (I_g) is calculated as,

$$I_g = \frac{V_{gs}}{R_{G_{st}}} \tag{2.4}$$

The transient impedance of the Zener diode (D_{zener}) is calculated from the gate sourcing current as,

$$Z_z = \frac{V_{D_{zener}}}{I_g} \tag{2.5}$$

From Figure 2.9, the transient impedance of a Zener diode alters the shape of the gate current. This results in a change in the gate voltage. The drain current shape is affected by the change in the gate voltage.

The simulation results with and without series Zener diode for Wolfspeed®C2M0080120D are plotted in Figure 2.6. The shoot-through current (I_{st}) shape for series Zener diode does not match WITH and WITHOUT Zener diode case.

2.0.2 On-state resistance (Rds_{on}) dependency on temperature

Various models of the MOSFETs are presented throughout its evolution and development. The Shichman-Hodges MOSFET model is known to be basic and easy for analytical analysis. This research is based on a controlled shoot-through technique proposed in [36]. The inventor of the CST technique [36] used the Shichman-Hodges

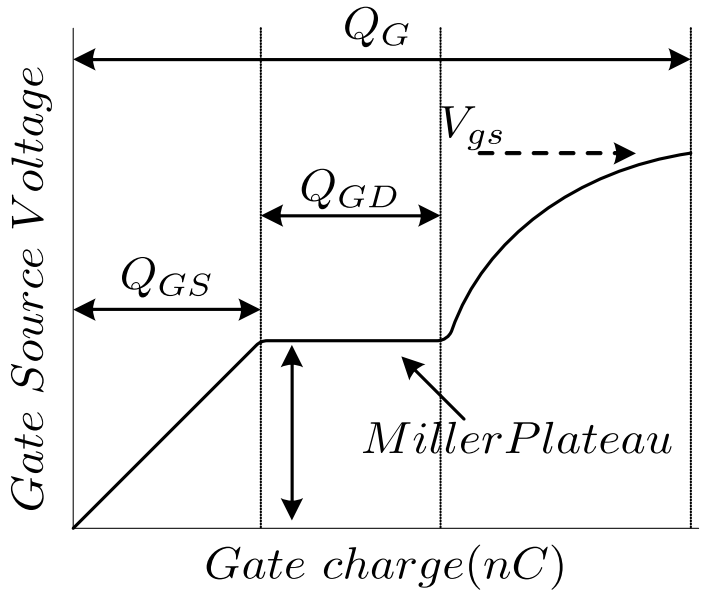


Figure 2.7: Charging of gate charges including miller plateau.

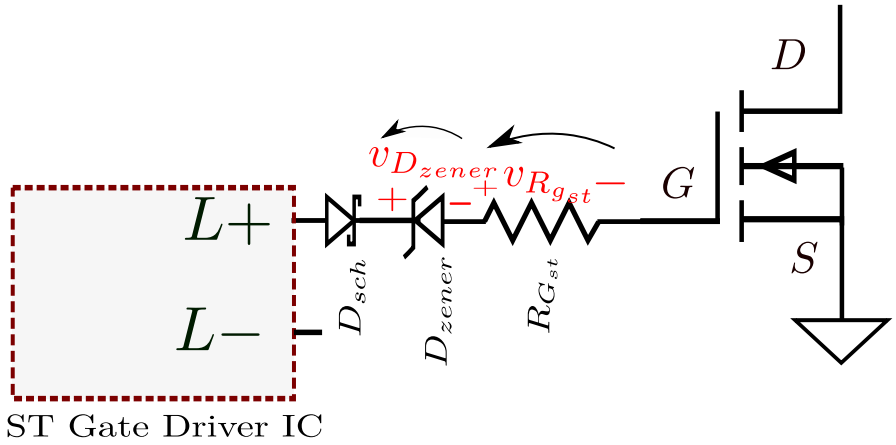


Figure 2.8: Circuit diagram for measurement of transient impedance of the Zener diode D_{zener}. L+ is sourcing path and L- is sinking path.

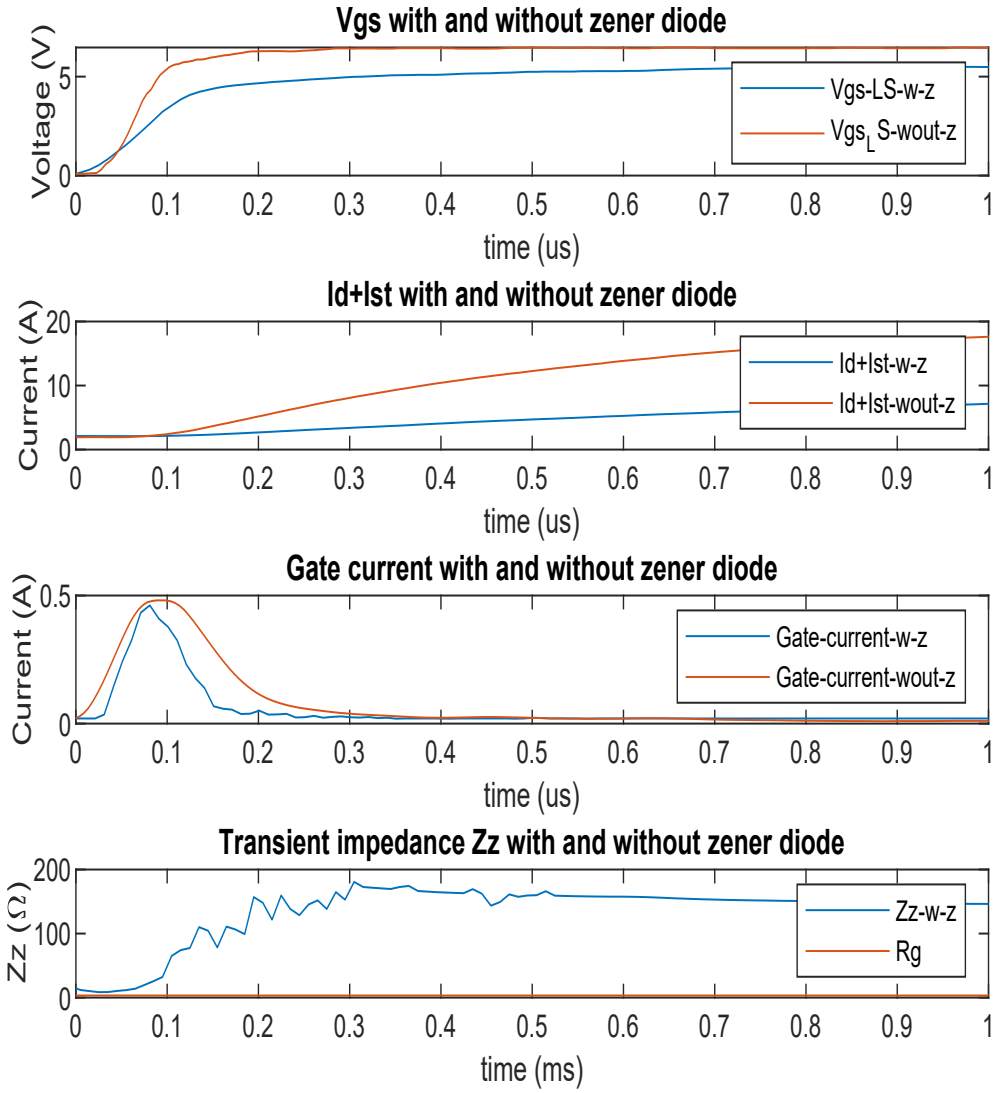


Figure 2.9: The V_{gs} shape changes due to change in the gate current. Red trace without Zener diode and Blue trace is Zener diode in series with gate driver. The change in gate current is due to transient impedance of Zener diode ranging from 10- 180 Ω. The change in gate results in change in the drain current. Test conducted with switching frequency $f_{sw} = 1\,\text{kHz}$.

MOSFET model to develop the loss models. Therefore in this thesis Shichman-Hodges based loss models are considered for the loss modeling. However, a separate study can be conducted to analyze the CST models considering more complex models.

The drain current in saturation region from Shichman-Hodges equation is given by,

$$Id_{(T_j)} = \frac{\mu_{(T_j)} C_{ox}}{2} \frac{W}{L} \left(V_{gs} - V_{th}(T_j) \right)^2 \tag{2.6}$$

The temperature dependencies of electron mobility μ and V_{th} alter the shape of the controlled shoot-through current and need to be analyzed. The silicon oxide degrades due to repetitive temperature [64], effects on the body diode [65] are not considered in the analysis.

One of the most important temperature-dependent MOSFET parameters is carrier mobility. As temperature rises, phonon density and scattering increase [66]. Thus, at higher temperatures, lattice scattering reduces the carrier mobility.

The temperature dependency of carrier mobility is given as,

$$\mu_{(T_j)} = \mu_{(T_r)} \left(\frac{T_j}{T_r} \right)^{k\mu} \tag{2.7}$$

Where T is absolute temperature, T_r is room temperature, $k\mu$ is fitting constant, usually 1.5, and $\mu_{(T_r)}$ is carrier mobility at room temperature (300 K) i.e. $0.14\,\mathrm{m}^2/\mathrm{Vs}$ [67].

From Figure 2.10, up-to 40% decrease in mobility carrier is observed at 373 K. Therefore, the decrease in the drain current happens.

The temperature also affects the threshold voltage of the MOSFET. The temperature dependency of carrier mobility and threshold voltage affects the transconductance and, eventually, on-state resistance. From Equation 2.6, the drain current increases with a decrease in temperature. Nevertheless, temperature dependency effects on carrier mobility dominate over threshold voltage decrease effects (usually, MOSFETs operate above room temperature), decreasing the drain current. This increases

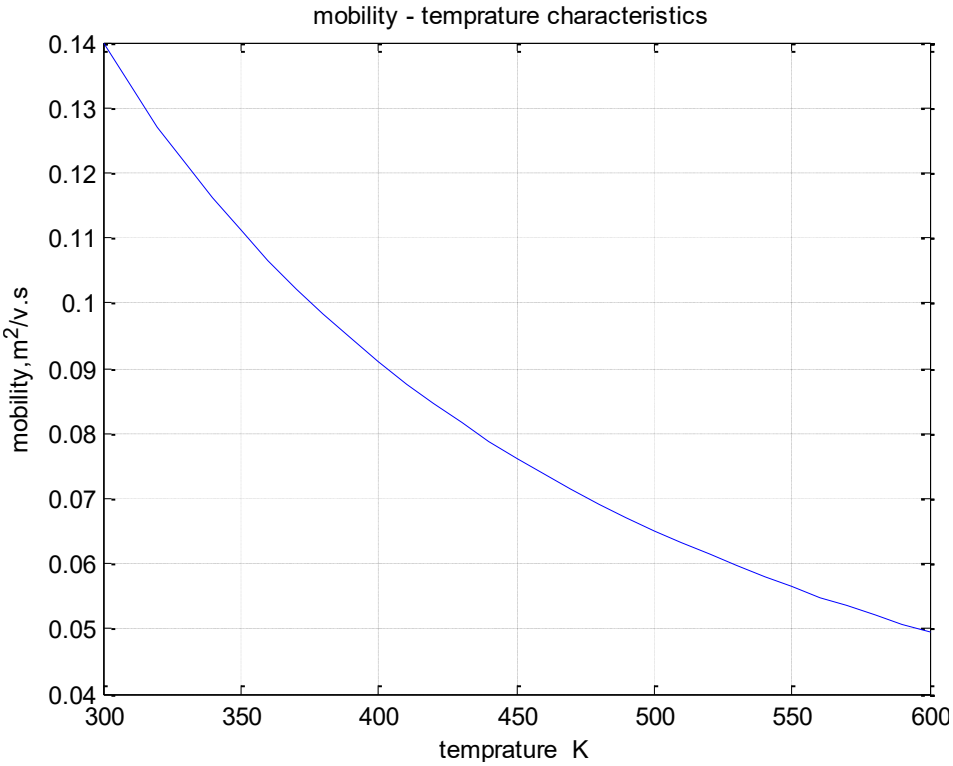


Figure 2.10: Mobility carrier decreases with increase in temperature.

on-state resistance, causing positive thermal feedback (term “positive feedback” used for an increase in on-state resistance).

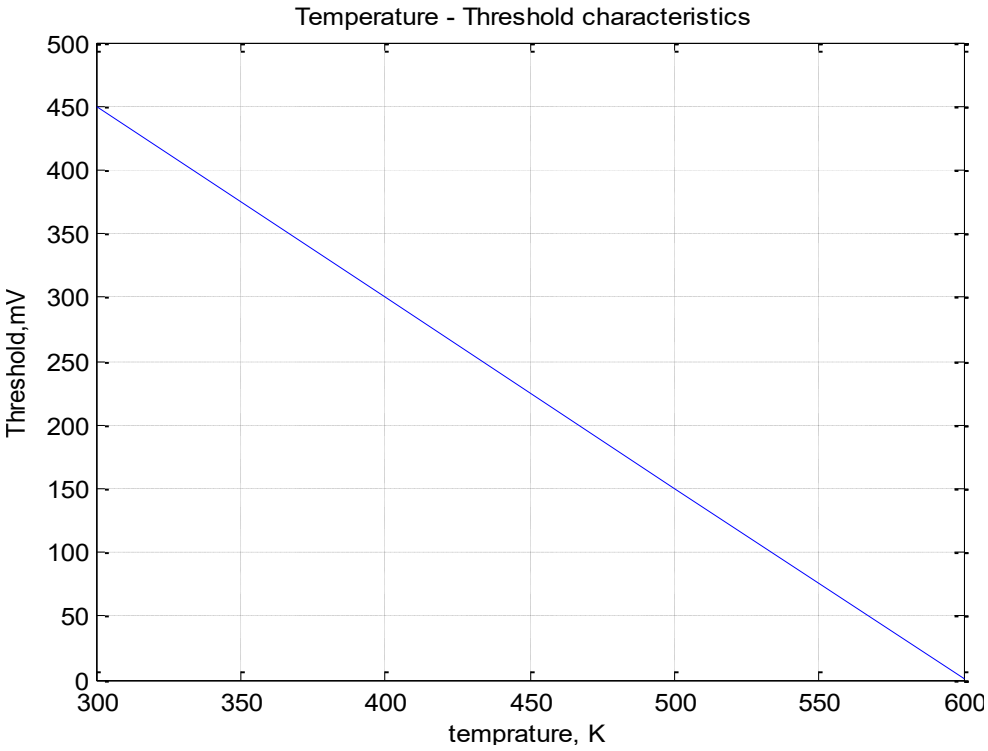


Figure 2.11: Threshold voltage linearly decrease with increase in temperature.

The threshold voltage (V_{th}) is given as,

$$V_{th} = V_{TO} + \gamma(\sqrt{|-2\phi_F + V_{SB}|}) - \sqrt{|-2\phi_F|} \tag{2.8}$$

Where body effect coefficient γ is,

$$\gamma = \frac{\sqrt{2qN_A\varepsilon_{si}}}{C_{ox}} \tag{2.9}$$

With increased temperature, intrinsic carrier concentration (N_A) decreases whereas Fermi potential ϕ_F increases. It results in a decrease in threshold voltage.

From [37], the on-state resistance is given as,

$$R_{ds_{on}} = \frac{V_{ds_{on}}}{i_d} \approxeq \frac{V_{gs} - V_{th}}{2i_{d,sat}} \tag{2.10}$$

by substituting values of $i_{d,sat}$ and V_{th} by referring equation 2.6 , 2.7, and 2.8 in equation 2.10,

$$R_{ds_{on}} = \frac{V_{gs} - V_{TO} + \gamma(\sqrt{|-2\phi_F + V_{SB}|}) - \sqrt{|-2\phi_F|}}{2\frac{\mu_{(T_j)}C_{ox}}{2}\frac{W}{L}\left(V_{gs} - V_{th}(T_j)\right)^2} \tag{2.11}$$

Numerator and denominator has $V_{gs} - V_{th}(T_j)$ common term, therefore on-state resistance as a function of temperature dependent mobility carrier and threshold voltage is given as,

$$R_{ds_{on}} \;\; f(\mu_{(T_j)}, V_{th}(T_j) = \frac{1}{\mu_{(T_j)}C_{ox}\frac{W}{L}\left(V_{gs} - V_{th}(T_j)\right)} \tag{2.12}$$

From Equation 2.12, it is concluded that the on-state resistance is a function of temperature-dependent parameters like mobility carrier and threshold voltage. Here the parameters C_{ox}, channel width, and length are considered constant. An increase in temperature causes a decrease in drain current, whereas a lowered threshold voltage causes an increase in drain current.

By considering V_{th} is constant over temperature change, the relation between $R_{ds_{on}}$ and $\mu_{(T_j)}$ becomes,

$$R_{ds_{on}} \propto \frac{1}{\mu_{(T_j)}} \tag{2.13}$$

From Equation 2.13, it can be stated that with an increase in temperature, the electron mobility carrier decreases and resulting in an increase in on-state resistance [68–70].

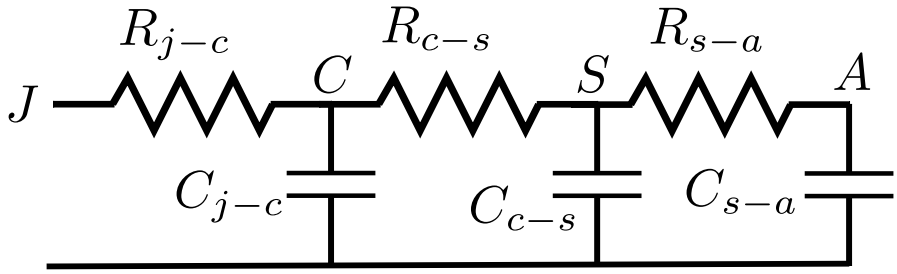


Figure 2.12: Equivalent R-C thermal model of MOSFET, heat-sink and ambient.

Thermal runaway due to local hot-spot

The increase in junction temperature causes an increase in on-state resistance, resulting in a decrease in drain current. This also helps in paralleling power MOSFETs. The high current carrying MOSFET heats up, causing an increase in on-state resistance. Therefore, current flows through a relatively colder MOSFET, resulting in a natural balancing of current. The self-heating device can also damage itself due to excessive junction temperature. The manufacturer specifies the maximum junction temperature. This is important in controlled shoot-through technique implementation. The dissipated power should not exceed the absolute maximum rating $T_j(max)$.

The maximum junction temperature is given as,

$$T_j(max) = T_a + (P_{sw} + P_{cst,max})(R_{j-c} + R_{c-s} + R_{s-a}) \tag{2.14}$$

Where P_{sw} is switching loss, $P_{cst,max}$ is the maximum power loss generated due to controlled shoot-through, R_{j-c} is thermal resistance from junction to case, R_{c-s} is thermal resistance from case to heat sink surface, and R_{s-a} is thermal resistance from heat sink surface to ambient, T_a is ambient temperature.

Therefore, the maximum allowable controlled shoot-through current in order to avoid thermal runaway is given as,

$$P_{cst,max} = \frac{T_j(max) - T_a}{(R_{j-c} + R_{c-s} + R_{s-a})} \tag{2.15}$$

The $P_{cst,max}$ is important to decide shoot-through time period and shoot-through voltage.

External cooling effect on self-heating of MOSFET

The power semiconductor device's temperature is an essential parameter for the life-time of the overall system. With an increase in temperature, the life of the power devices decreases. Various cooling methods are available for the power electronic converters like liquid, forced, and chip level cooling as reported in Chapter 1.

The thermal time constant (τ_θ) for MOSFET by referring Figure 2.12 is given as,

$$\tau_\theta = \tau_{j-c} + \tau_{c-s} + \tau_{s-a} \tag{2.16}$$

$$\tau_{\theta(c-a)} = R_{j-c} \cdot C_{j-c} + R_{-s} \cdot C_{c-s} + R_{s-a} \cdot C_{s-a} \tag{2.17}$$

The dynamic junction temperature of MOSFET temperature rises with the rise in current, which lasts in the range of µs. In contrast, the thermal time constant of the cooling arrangement varies from seconds to minutes depending on thermal impedance and capacitance. The higher time constant of the cooling system at the body case level will not have any effect on the dynamic junction temperature of the MOSFET ($\tau_{\theta(c-a)} \ggg \tau_{\theta(j)}$). The chip level cooling system is proposed in the literature [57]. Assuming all instantaneously generated heat is dissipated in the junction-level cooling system, there will not be a self-heating effect. This will result in no change in the on-state resistance of MOSFET as shown in Figure 4.1. However, in reality, it is impossible to instantly remove heat generated at die without causing self-heating.

Material effect on self-heating

Heat buildup in the channel at high power levels is called self-heating. Device scaling, high current densities, and using materials with low thermal conductivity all contribute to self-heating in semiconductor devices. The heat conductivity of materials like SiO_2 and $SiGe$ is much poorer than that of Si [71]. The thermal conductivity of

SiO_2 is 1.4 $Wm^{-1}K^{-1}$, whereas Si is 148 $Wm^{-1}K^{-1}$. Advanced semiconductor devices may exhibit increased self-heating due to the high-gate dielectric's poor thermal conductivity [72].

2.1 Inflection Point: Transition from negative thermal feedback to positive thermal feedback- The start of self-heating

The inflection point is vital in defining the loss model for the controlled short-circuit technique. The inflection point states about change in the **N**egative **T**emperature **C**oefficient (NTC) to **P**ositive **T**emperature **C**oefficient (PTC) of the MOSFET. The MOSFET has a Positive Temperature Coefficient; as a result, with a rise in junction temperature, the on-state resistance increases. In other words, when temperatures rise, drain currents decrease. This is critical when MOSFETs are operating in parallel. With a suitable thermal channel between devices, the positive temperature coefficient decreases current in the hottest device while forcing more current to flow in the cooler device, preventing thermal runaway [73]. If the controlled shoot-though continues to operate in negate temperature coefficient region, the controlled short circuit can increase exponentially and damage the device as shown in Figure 2.13. The pink trace shows an uncontrolled short circuit due to a local hotspot. Therefore knowing the inflection point, negative temperature coefficient and positive temperature coefficient area is essential.

The temperature gradient is minimized, and hot spots are avoided by increasing the resistivity of such MOSFETs and causing current to flow in cooler MOSFETs. This fundamental physical principle enables the parallel array of cells to work correctly.

At a certain V_{gs}, all three temperature curves will meet at some point, as shown in Figure 2.13. This is called the "inflection point" [73, 74]. In more explanatory words, it can be explained as a transition from negative thermal feedback to positive thermal feedback that happens at a point. This point is called "inflection point". The inflec-

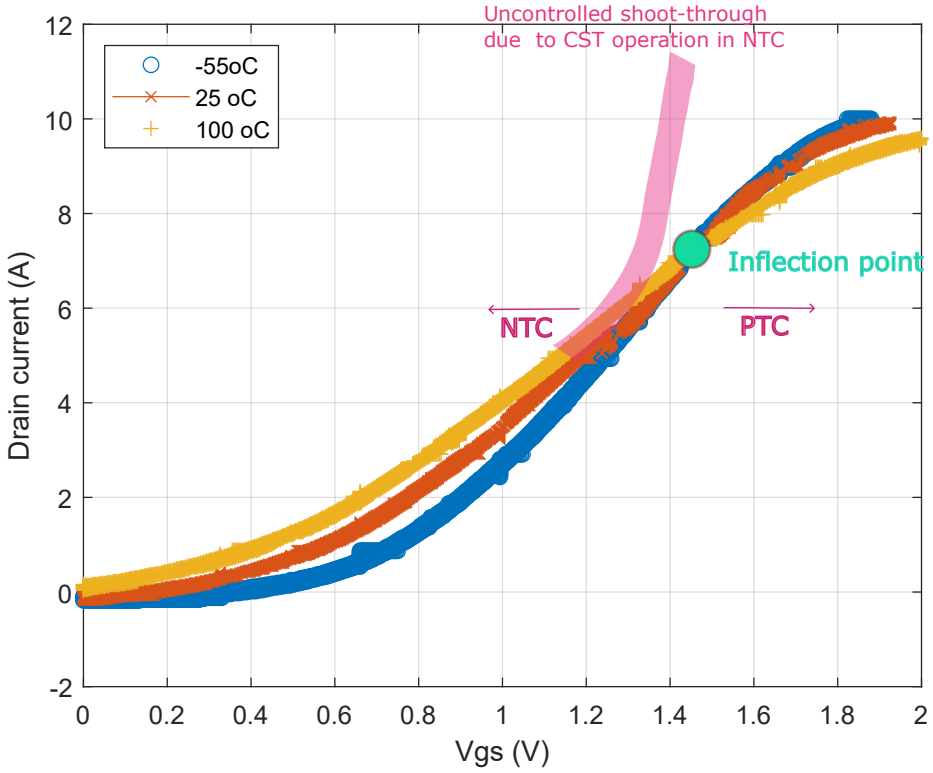


Figure 2.13: Typical representation of inflection point separating negative thermal feedback region and positive thermal feedback region $V_{ds} \geq 10$ V [73] .

tion point is also referred to as "Temperature Compensation Point (TCP)" [11]. This point is thermally stable. Therefore, it separates the Negative Temperature Coefficient (NTC) and Positive Temperature Coefficient (PTC) of the power device [11, 75]. The transfer characteristics meet at a TCP point as shown in Figure 2.13.

The $R_{ds_{on}}$ rise as junction temperature rises for a V_{gs} above the inflection point [73]. Therefore, MOSFETs carrying higher currents become more resistive, and current is shared with cells carrying lower currents. This MOSFET feature ensures that current is distributed uniformly across all devices.

The MOSFET behaves more like a bipolar transistor below the inflection point. A cell with a higher current than the surrounding cells will continue to take more current as the device heats up. Thermal runaway can occur if the device continues in this transition area for an extended period of time. To ensure proper device operation, the load switch should be operated with a V_{gs} above the inflection point [73].

The controlled shoot-through current shape changes due to self-heating. Predicting when positive thermal feedback will come into play will be beneficial. An inflection point is related to $R_{ds_{on}}$. The $R_{ds_{on}}$ is lower when the junction temperature is lower. The $R_{ds_{on}}$ increases with an increase in junction temperature.

Due to the negative temperature coefficient (NTC) feature, which tends to focalize current and create local hot spots, operating at low gate voltage (linear region of MOSFET) might result in secondary failure and thermal runaway [76–78].

At inflection point the change in the drain current is zero. Therefore the Equation 2.6 becomes,

$$\frac{\mathrm{d}\left(Id_{(T_j)}\right)}{\mathrm{d}T_j} = \frac{\mathrm{d}\left(\mu_{(T_j)}\zeta\left(V_{gs}-V_{th}(T_j)\right)^2\right)}{\mathrm{d}T_j} \tag{2.18}$$

Here $\zeta = \frac{C_{ox}}{2}\frac{W}{L}$, where A is constant. The at inflection point i.e. TPC $\frac{\mathrm{d}\left(Id_{(T_j)}\right)}{\mathrm{d}T_j}$=0. Therefore, Equation 2.18 becomes,

$$0 = \frac{\mathrm{d}\mu_{(T_j)}}{\mathrm{d}T} + 2(V_{gs}-V_{th}(T_j))\frac{\mathrm{d}V_{th}(T_j)}{\mathrm{d}T_j} \tag{2.19}$$

At higher temperatures, the mobility carrier is dominated over the threshold voltage. Therefore, inflection point dependency on the mobility carrier is given as,

$$\frac{\mathrm{d}\mu_{(T_j)}}{\mathrm{d}T} = -2(V_{gs} - V_{th}(T_j))\frac{\mathrm{d}V_{th}(T_j)}{\mathrm{d}T_j} \tag{2.20}$$

From Equation 2.20, a decrease in mobility carrier point can be stated, and at the same point, self-heating of the device starts.

2.2 Controlled shoot-through loss models under different condition depending on series Zener diode and self-heating

Three types of different loss models are considered depending on whether the series Zener diode (3 V and 7.5 V) is used along with the gate driver or not. The next model in which self-heating of the MOSFET is considered. The following loss models are considered:

- Ideal loss model.
- Loss model for Zener diode in series (between gate driver and gate of MOSFET) and NO self-heating.
- Loss model considering self-heating and NO Zener diode in series.

2.2.1 Ideal loss model for controlled shoot-through technique

As explained in section 1.1, in the ideal controlled shoot-through condition, the drain current should follow gate voltage (square-wave in shape [35, 36]. Under NO Zener diode in series and considering NO self-heating, the CST current shape is a square wave as shown in Figure 2.16.

The direct model for losses under these conditions is given as [35],

$$Est,H = (V_{dc} - V_o)I_{st}t_{st} \tag{2.21}$$

$$Est,L = V_o I_{st} t_{st} \tag{2.22}$$

Where Est,H is shoot-through loss in high side MOSFET and Est,L is shoot-through loss in low side MOSFET.

The loss model for real applications can be considered by deducting switching losses from the ideal loss mode. The energy lost during a shoot-through (ST) event is given as [35, 36] (Green area in Figure 1.21),

$$E_s t = \int_0^{t_{st}} V_{dc} I_{st} dt \tag{2.23}$$

$$Est = V_{dc} I_{st} t_{st} \left[1 - \frac{\tau}{t_{st}} (1 - e^{\frac{-t_{st}}{\tau}}) \right] \tag{2.24}$$

2.2.2 Loss model for Zener diode in series and considering NO self-heating

The transient impedance offered by the series Zener diode affects the gate sourcing current and results in a change in the gate to source voltage build-up as shown in Figure 2.2 and Figure 2.9. The following sub-sections give mathematical modeling for the altered shape of the CST current.

Due to the high transient impedance of 3 V series Zener diode, the gate of the MOSFET does not charge completely. As shown in Figure 2.2, the transient impedance with a lower Zener voltage has a higher transient impedance. Therefore, the drain current shape is different for 3 V and 7.5 V series Zener diode as explained in Sub-section 4.1.

Due to the transient impedance of 3 V Zener diode, the shoot-through current becomes triangular in shape as shown in Figure 2.14.

The loss model for 3 V series Zener diode is given in Equation 2.25. The shape of the controlled shoot-through current is triangular. Therefore, the area of the triangle is given as,

$$E_{st-LS_{3VZener}} = \frac{1}{2} t_{st} I_{st'} V_{dc} \tag{2.25}$$

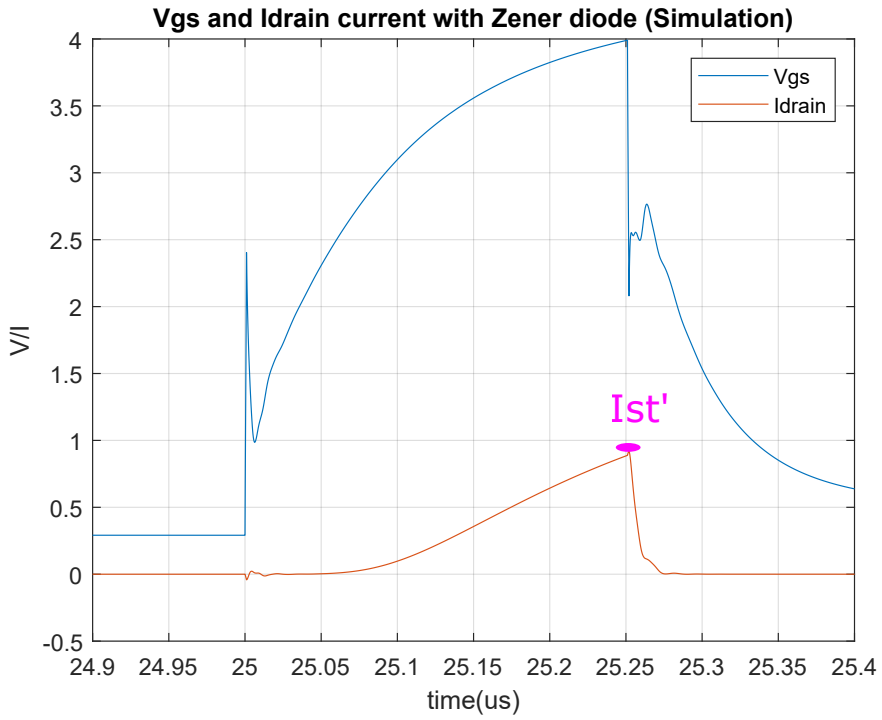


Figure 2.14: Shoot-through current (Ist) with 3V Zener diode in series. Wolfspeed® C2M0080120D, V_{dc}= 100 V.

2.2.3 Loss model by considering self-heating

The Negative Temperature Coefficient and Positive Temperature Coefficient alter the transfer characteristics as shown in Figure 2.13. Due to the absence of transient impedance of the Zener diode, the gate sourcing current charges the gate of the MOSFET, resulting in drain current following the almost square-wave (ideally) as the gate to source voltage (V_{gs}).

The current shape follows a half-parabolic arch path from 0 to the inflection point (t_1). From the inflection point, the self-heating of MOSFET offers higher on-state resistance ($R_{ds_{on}}$). The instantaneous loss is not constant. This results in a change in half the parabolic arch shape in the straight line path of the drain current. From t_1 to

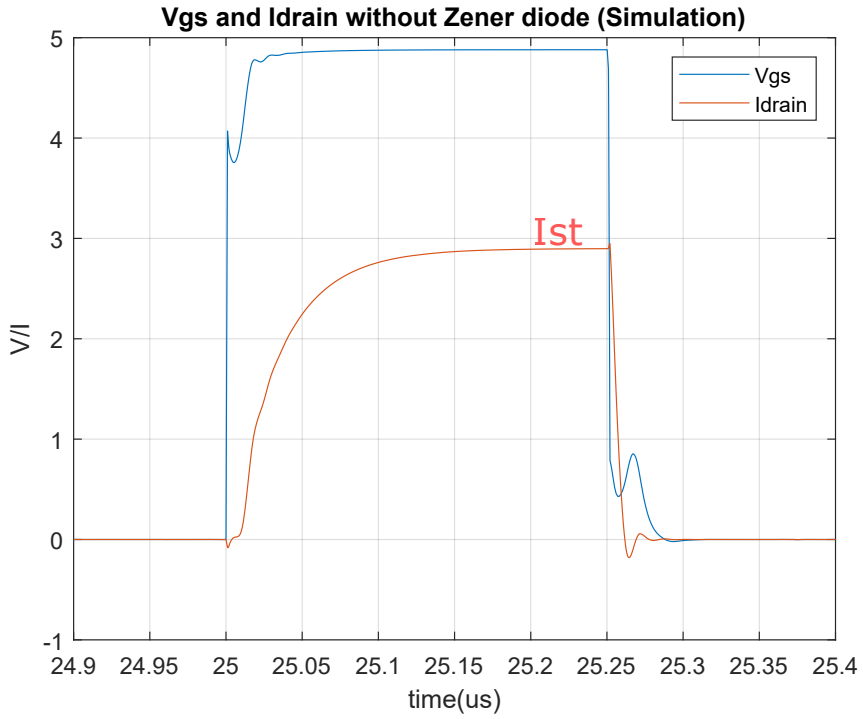


Figure 2.15: Shoot-through current (I_{st}) No Zener diode in series. Wolfspeed® C2M0080120D, V_{dc}= 100 V.

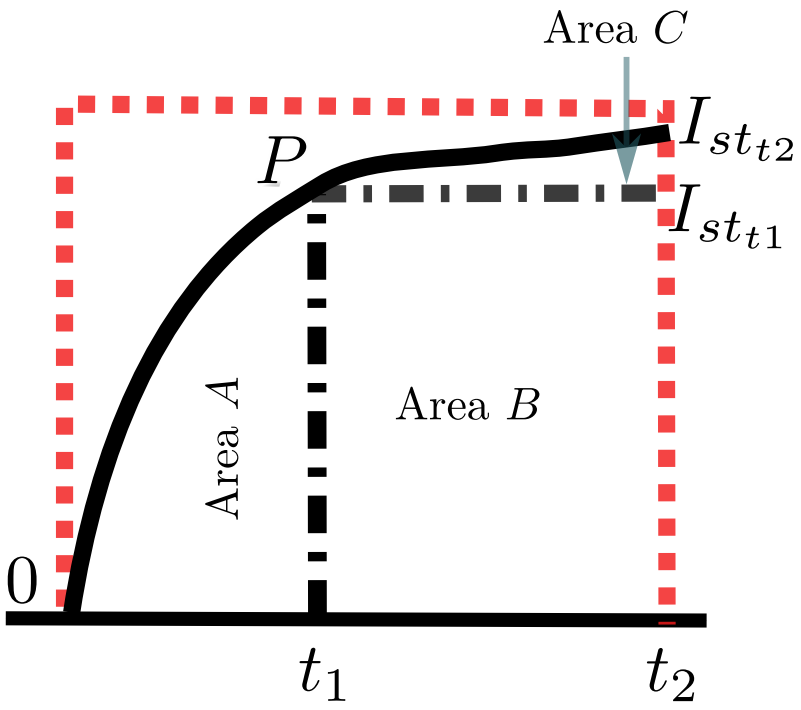


Figure 2.16: CST current shape without Zener diode in series. Point *P* is inflection point. The area A, B and C are shown to define the loss model. The RED trace shows ideal shoot-through current and BLACK trace shows shoot-through current due to self-heating.

t_2, the current shape is a constant slope. Therefore, the area calculated for the loss model is shown in Figure 2.16.

Energy lost for area A is given as Equation 2.24 [36],

$$E_A = Est = V_{dc} I_{t_1} t_1 \left[1 - \frac{\tau}{t_1}(1 - e^{\frac{-t_1}{\tau}}) \right] \tag{2.26}$$

The area energy loss under Area B is given as,

$$E_B = (t_2 - t_1) I_{st_{t1}} V_{dc} \tag{2.27}$$

Similarly, the energy loss under Area C calculated as,

$$E_C = \frac{1}{2}(t_2 - t_1)(I_{st_{t2}} - I_{st_{t1}}) V_{dc} \tag{2.28}$$

From Equation 2.26, 2.27, and 2.28 the energy lost considering self-heating is given as,

$$E_{st-self\ heating} = E_A + E_B + E_C \tag{2.29}$$

$$E_{st-self\ heating} = \underbrace{V_{dc} I_{st} t_1 \left[1 - \frac{\tau}{t_1}(1 - e^{\frac{-t_1}{\tau}}) \right]}_{\text{Area A}} + \underbrace{\Big(t_2 - t_1\Big) I_{t_1} V_{dc}}_{\text{Area B}} + \underbrace{\frac{1}{2}\Big(t_2 - t_1\Big) I_{t_2} V_{dc}}_{\text{Area C}} \tag{2.30}$$

The loss models are explained in section 1.1 as a direct model, a model by considering nonlinear effects, and an inverse model [36]. The loss model considering self-heating is given in Equation 2.30. For high V_{DS}, the shoot-through current causes self-heating during controlled shoot-through duration. Therefore, the self-heating must be calculated considering different areas specified in Figure 2.16. Whereas, with low shoot-through current, due to the absence of self-heating phenomenon, the shoot-through current shape and respective loss models are explained in Subsection 2.2.1.

2.3 Summary

After explaining the state of the art on active thermal control, chapter 2 dives in-depth on the controlled shoot-through method and loss models. The traditional method to achieve third-level voltage was to connect a series zener diode as shown in Figure 2.1. It is not possible to change the third-level voltage during the operation of the converter. Therefore new gate driver is proposed in this thesis. However, it is worth noticing that the cost of implementation by using a zener diode is much less than the proposed gate driver in the thesis. Therefore analyzing the effect of zener diode on the loss models brings industrial value to the technique. The loss models by using proposed gate drivers and conventional gate drivers with series zener diode are compared.

Due to high junction temperature during controlled shoot-through duration, the self-heating also affects the loss model. Therefore the loss model by considering self-heating is derived in Equation 2.30.

Chapter 3

Development of Three-level Two-degree-of-freedom Active Gate Driver (TL-2DoF-AGD)[1]

Nature is our kindest friend and best critic in experimental science if we only allow her intimations to fall unbiased on our minds.

– Michael Faraday

The controlled shoot-through (CST) is a half-bridge working in the controlled short-circuit condition. Following MOSFET nomenclature, CST is a modulation technique that involves a specific gate driver to force the device into a saturation region. Working in saturation is typical for switching devices since this region is traversed only in transients from on-state to off-state and vice versa. Forcing this operating mode in other moments enables accurate control of additive device loss without remarkable effects on the output waveforms [35].

[1] The three-level two-degree-of-freedom active gate driver (TL-2DoF-AGD) is developed under research project PSEudo-COgeneration for Battery heating on electric and hybrid Boats (*PSECOB*[2]) funded by OIS-AIR InnovAIR Platform, 2019 [39]. URL: https://www.oisair.net/.

Despite the actual disadvantage of increasing device power loss in normal operation, the controlled shoot-through technique enables some features that can be interesting in transient modes. First, it transforms the power switch into a source of heat, with applications in device characterization [79] and for pre-heating in cold-start scenarios [38].

In addition, the CST current is, for all intents and purposes, a saturation current; measuring it after an appropriate calibration procedure improves the applicability of this quantity as a TSEP, thus widening its use.

This chapter explains the complete design and implementation of a three-level two-degree-of-freedom active gate driver (TL-2DoF-AGD). This gate driver can generate a suitable gate voltage pattern for controlled shoot-through. Differently from existing implementations, the additional (third) gate voltage level can be controlled in real-time; hence two-degrees of freedom are available for control, i.e., CST pulse duration (t_{st}) and CST pulse amplitude (V_{st}). The TL-2DoF-AGD operation is hence validated and bench-marked with different loss models.

3.1 Design of Three-level Two Degree of Freedom Active Gate Driver (TL-2DoF-AGD)

In this section, the design and architecture of the gate driver are discussed. The selection of gate resistor wattage, analog reference voltage generation, non-linearity in the optocouplers, and load modeling for gate capacitances are discussed in this section.

The maximum sourcing current of SI8271 gate driver IC at T_a=20 Deg C ambient temperature is 1.7 A [85]. Therefore the losses that occurred in the gate resistor are given as P_{loss,R_g},

$$P_{loss,R_g} = I_{src}^2 \cdot R_g \tag{3.1}$$

I_{src} is sourcing current and R_g is gate resistor.

$$P_{loss,R_g} = 1.6^2 \cdot 3 = 11.22 watt \tag{3.2}$$

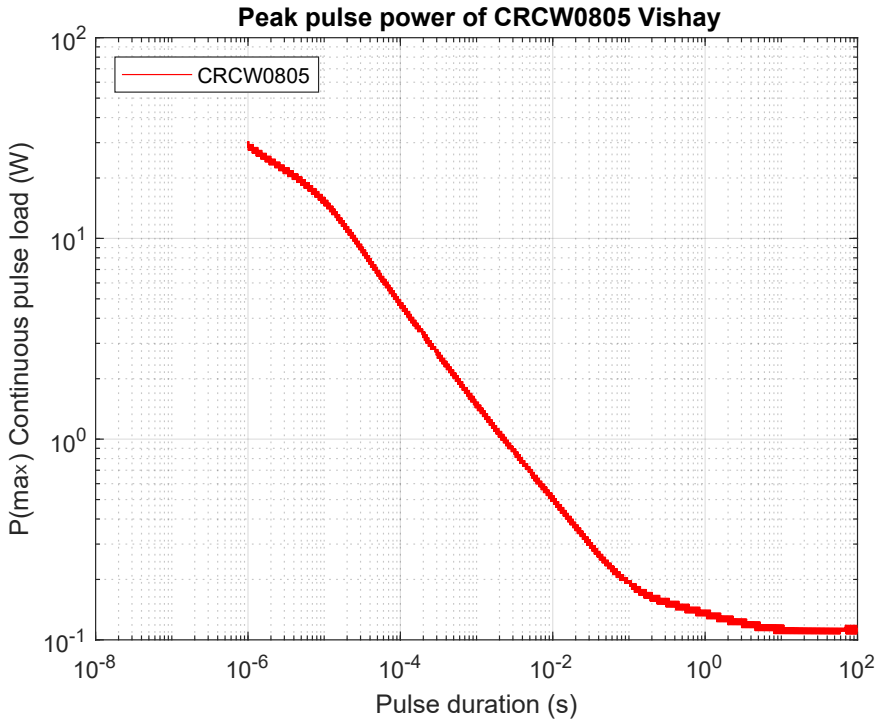


Figure 3.1: Selection of gate resistor power rating based on repetitive pulse power graph from manufacturer for CRCW0805 Vishay® [80].

The dropout voltage across LDO causes saturation of output voltage as shown in Figure 3.2. The input voltage should be higher than the output voltage (at-least dropout voltage should be considered). The nonlinearity in the output of the optocoupler was observed during the development of the gate driver, as shown in Figure 3.3. The discussion on the non-linearity of opto-electronics is out of the scope of this research work. But care should be taken while selecting an optocoupler for the reference shoot-through voltage generation (RC) stage.

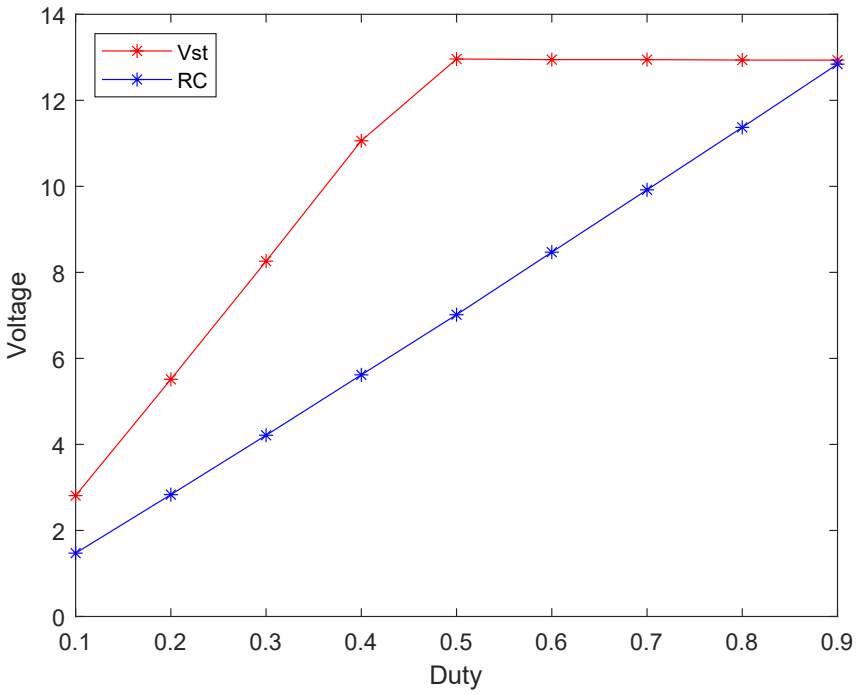


Figure 3.2: RC filter stage to generate reference voltage to PWM controlled LDO stage. Blue line represents output of RC filter and Red line represents output of PWM controlled LDO.

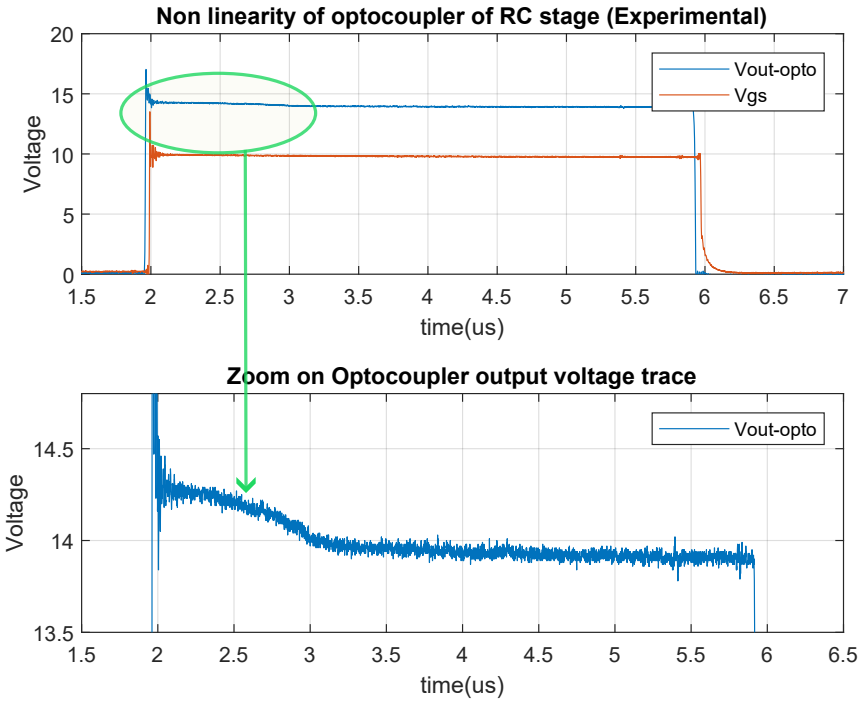


Figure 3.3: Non-linearity of output voltage of optocoupler ACPL-4800-000E Broadcom® [81].

Load model

The peculiarity of a gate driver supply resides in the load that, differently from the other most common cases, is mainly capacitive. Turning on the MOSFET involves the charging of the gate capacitances. The gate voltage pulses are required to turn on the MOSFET. The gate driver load i_o can thus be modeled as a pulsed current generator with period T_s (equal to the switching one) and with two different values: I_h during the charging phase, I_ℓ otherwise:

$$i_o(t) = \begin{cases} I_h & \text{if} \quad \text{mod}\,(t, T_s) \leq cT_s \text{ (phase 1)} \\ I_\ell & \text{otherwise (phase 2).} \end{cases} \tag{3.3}$$

The parameter c represents the relative duration of the charge phase. This is a crude simplification since the effective shape of the current is exponential, but it simplifies the computation without excessive errors.

This load is not driven by the gate driver supply directly, but it is filtered by a shunt capacitor C_o, which is used to reduce the current ripple seen from the converter. The capacitor C_o, combined with the equivalent series resistance of the power supply R_s, creates a low-pass filter. This section aims to identify under which conditions the load seen from the power supply can be regarded as a constant current source, with all the current ripple withstood by C_o.

Two models are given: one is based on the approximation of the constant current from the supply i_s, and the other is exact and based on the equivalent circuit of gate capacitance as shown in Figure 3.4. In reality, the C_{out} is the decoupling capacitor of the dynamic third-level gate-driving IC. The I_o is the gate charging current of the MOSFET, and V_o is voltage built up across the gate-source due to gate charging.

Isolated DC-DC converter characterization

The third-level dynamic gate voltage can not be generated with the help of the bootstrap gate driving circuit topology due to the need for charging of the bootstrap capacitor C_{boot}. Therefore, the dedicated DC-DC power supply is essential for producing

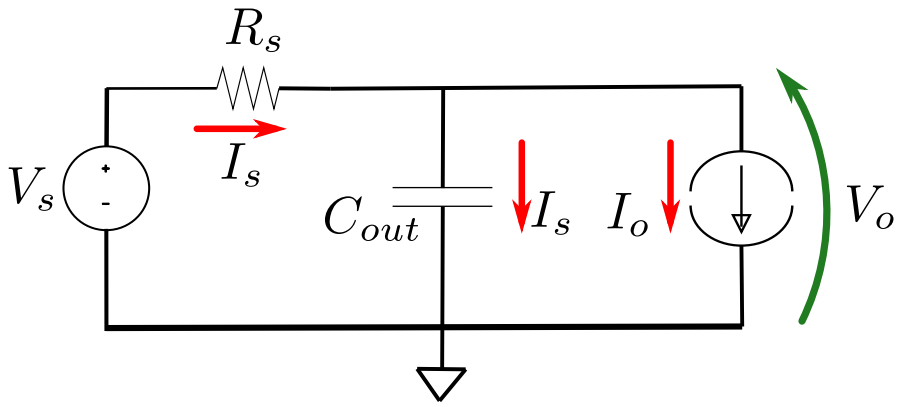


Figure 3.4: Equivalent circuit of load current required to charge the gate of the MOSFET.

third-level dynamic gate voltage. The floating point in the half-bridge requires an isolated DC-DC power supply [82]. The accuracy of gate voltage is vital to determine the exact shoot-through voltage as expected. Therefore, the experimental measurement data must match the linear model shown in Figure 3.5. The power supply is an isolated DC-DC power supply used by RECOM RP-2415D [82].

The experimental data compared with the linear model of uncontrolled isolated DC-DC power supply [82]. The results are post-processed in MATLAB, and the script is available in Appendix B.3.

3.2 Third-level dynamic gate voltage generation

Traditional two-level gate driver has two stage(0 or Negative voltage) and high (V_{gs}). The term "third-level voltage" indicates variable gate voltage between OFF and ON voltage. To achieve fixed gate voltages and variable gate voltages, dedicated gate driver ICs are required.

The parallel connection of gate driver ICs is shown in Figure 3.9. The Schottky diodes are essential to avoid clamping of two different gate voltages (traditional gate voltage of 15V and ST gate voltage) as shown in Figure 3.8. An additional gate driver

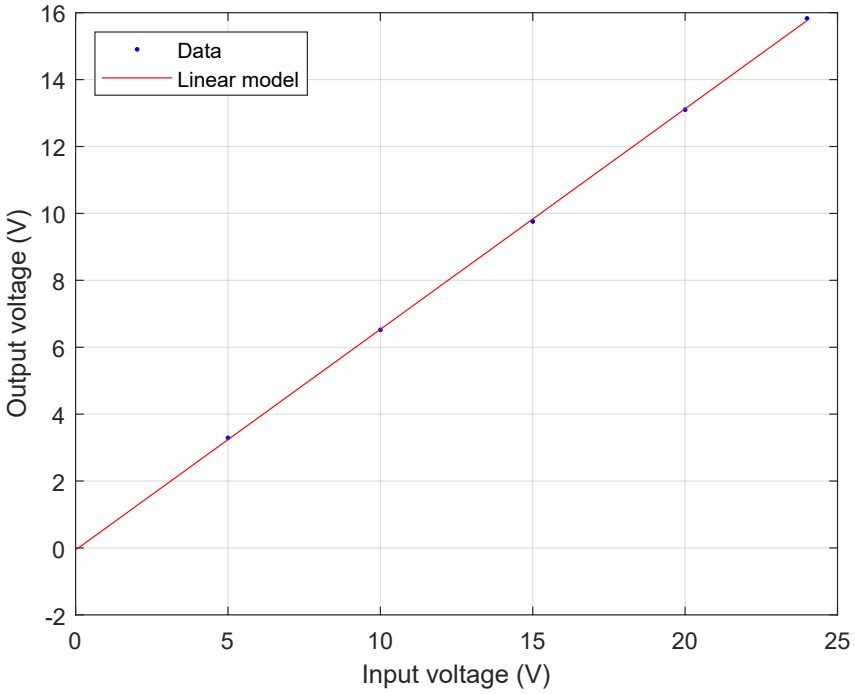


Figure 3.5: Characterization of isolated DC-DC converter (RECOM RP-2415D) for the TL-2DoF-AGD.

IC is required to sink the gate charge (sink MOSFET) as shown in Figure 3.8. Omitting sinking gate driver IC will create a short circuit path through the pull-low path of the complementary gate driver IC (sinking gate driver IC), i.e., H+ of "Traditional Gate Driver IC" short-circuited via H- of "ST Gate Driver IC". Therefore, the low path of the "Traditional Gate Driver IC" and the "Shoot-Through Gate Driver IC" are kept floating. The sink path is provided through a small signal MOSFET (also called "Sink MOSFET") with a dedicated gate driver IC called the "Sinking Gate Driver IC".

The Under Voltage Lockout (UVLO) feature of the gate driver IC shuts down the output voltage when the supply voltage (in this case, dynamic gate voltage) is below some specified value. It depends on the manufacturer, and in the datasheet, it's mentioned as a V_{UVLO}. The SiC MOSFETs have a lower threshold voltage than Si MOSFETs and IGBTs [83, 84]. Few gate driver ICs have V_{UVLO} lower than threshold voltage v_{th} of SiC MOSFETs [85, 86]. To overcome this problem, the Zener diode (D_{zener}) can be attached in series to the output voltage of the gate driver IC as depicted in Figure 3.8. This impacts the shape of the controlled shoot-through current due to the Zener diode's transient impedance (Z_z). This is discussed in section 2.2.

A PWM-controlled LDO is used in the TL-2DoF-AGD to generate the third-level gate voltage. PWM-based LPF-filtered DAC creates the reference voltage $V_{st_{ref}}$ for the PWM-controlled LDO. The *RC* filter converts the PWM duty into a variable analog output voltage known as $V_{st_{ref}}$. The reference voltage varies from 0 to $V_{st,max}$. The PWM-controlled LDO, as illustrated in Figure 3.6, is used to vary the shoot-through voltage V_{st} by varying $V_{st_{ref}}$. The $V_{st_{ref}}$ is the varying duty cycle of the control signal. As the floating ground is needed for the HS MOSFET, an optocoupler isolates the control and power sections as depicted in Figure 3.9.

Let V_{ref} be the reference input voltage to the error amplifier, V_{out} is the output voltage required ("shoot-through voltage (V_{st})" or "dynamic third level gate voltage"), R_h is high side resistance, R_l is Low side resistance.

The output of LDO given as,

$$V_{out} = V_{st} = V_{st_{ref}} \left(1 + \frac{R_l}{R_h + R_l}\right) \tag{3.4}$$

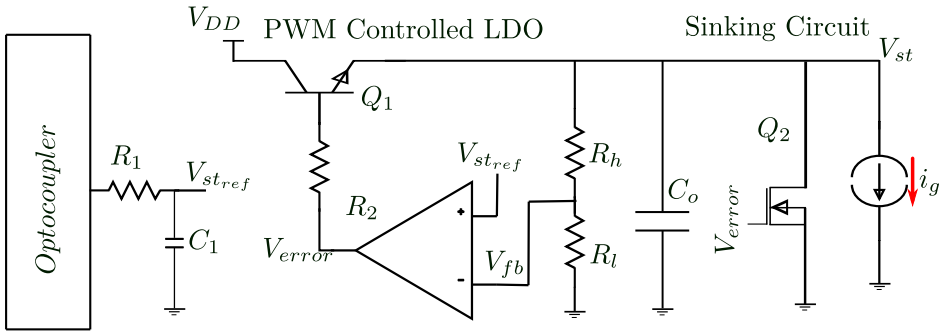


Figure 3.6: Low dropout regular (LDO) for third-level dynamic gate voltage generation and sinking MOSFET for higher slew rate during fall time.

Figure 3.8 and Figure 3.9 show the architecture of the level two-degree-of-freedom architecture. The shoot-through gate driver IC and the traditional gate driver IC are connected in parallel. The gate resistances of the traditional and shoot-through gate driver ICs are represented by R_G and $R_{G_{st}}$, respectively. The Schottky diodes D_{sch_1} and D_{sch_2} prohibit the clamping of V_{gs} with V_{st}.

The gate driver IC (SI8271) operates in a push-pull mode [85]. As a result, if two gate driver ICs are connected in parallel, the sourcing current (I_g and $I_{g_{st}}$) of one is short-circuited by the sinking path of the other. Therefore, a distinct sinking route is necessary. The sinking routes of both the traditional gate driver IC and the shoot-through gate driver IC are maintained sinking paths in floating condition. As illustrated in Figure 3.8, the V_{gs} is applied, charging the MOSFET's gate with I_g and sinking in the route of I_{sink}.

Similarly, V_{st} serves as a shoot-through voltage, and $I_{g_{st}}$ charges the MOSFET gate and sinks in the I_{sink} route. When V_{gs} or V_{st} is applied to the sinking route, it enters high impedance mode (HiZ).

3.3 Maximum and minimum LDO output voltage

In order to generate a reference voltage for the LDO, the control signal from the microcontroller unit (MCU) is converted into an analog signal (Digital to Analog- DAC)

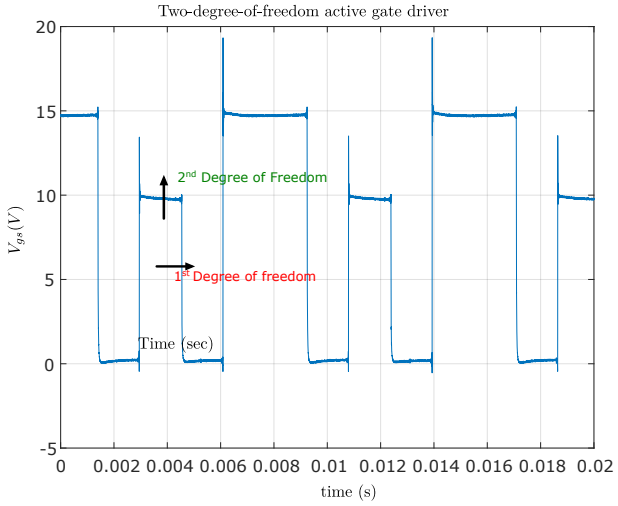


Figure 3.7: Output of Three-level two-degree-of-freedom Active Gate Driver (TL-2Do-AGD).

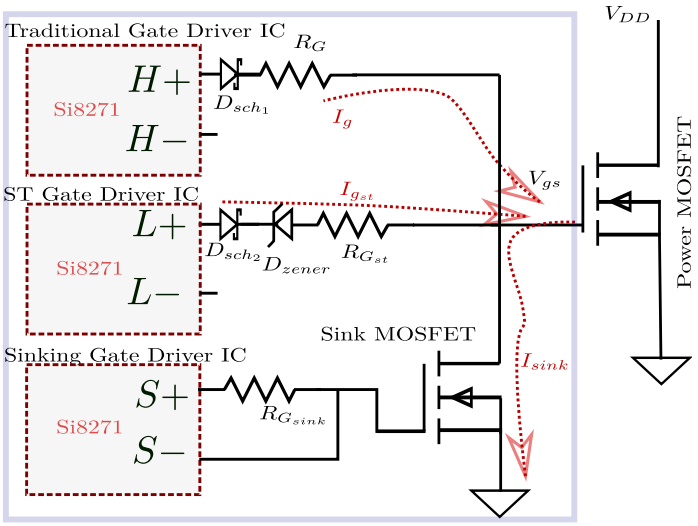


Figure 3.8: Block diagram of TL-2DoF-AGD: Three gate driver ICs (SI8271) in parallel for traditional, shoot-through and gate turn-off operation.

Input	V_{DD} for GD	V_{st} for ST GD	EN for GD	EN for ST GD	Output
PWM	Power ON	Power ON	High	Low	V_{gs}
PWM ST	Power ON	Power ON	High	Low	$\emptyset$
PWM ST	Power ON	Power ON	Low	High	V_{st}
PWM	Power ON	Power ON	Low	High	$\emptyset$
PWM	Power ON	Power ON	Low	Low	$\emptyset$
PWM	Power ON	Power ON	High	High	V_{gs}

Table 3.1: Truth table for output combination of PWM, PWM ST and EN signals. V_{gs}: gate to source voltage, V_{st}: shoot-through voltage, $\emptyset$: Pull low. GD stands for "Traditional gate driver IC", ST GD stands for "Shoot-through gate driver IC".

using a RC filter. The maximum and minimum output voltage of PWM-controlled LDO is set by reference shoot-through voltage $V_{st_{ref}}$ or by setting $V_{out} = V_{ref}$ if $R_h = 0$ or $R_l = \infty$. The dropout voltage required to operate the low-dropout regulator is also important. By considering the dropout voltage of LDO, the output voltage (shoo-through voltage V_{st}) is given as,

$$V_{st} = V_{DD} - V_{ce} \tag{3.5}$$

The gate driver IC has internal voltage drop [85]. Therefore, the output voltage of third-level voltage generation is given as,

$$V_{st} = V_{DD} - V_r \tag{3.6}$$

Where, V_r is internal drop across MOSFET gate driver IC.

From Equation 3.5 and Equation 3.6, the total voltage drop observed in the third-level voltage generation is,

$$V_{st} = V_{DD} - V_{ce} - V_r \tag{3.7}$$

The minimum and maximum third-level voltage generated from PWM controlled LDO is given as,

$$V_{st} = V_{out} = \begin{cases} V_{out}^{\max} = V_{DD} - V_{ce} - V_r & \text{maximum output voltage} \\ V_{out}^{\min} = 0 & \text{minimum output voltage} \end{cases} \tag{3.8}$$

The accuracy in third-level dynamic gate voltage generation is an critical due to sensitivity of drain current with respect to the gate voltage.

3.4 Optimization of LDO

The slew rate of the third voltage generation determines the bandwidth of the gate driver. Therefore, the faster rise and fall of the third voltage is important. The $\sigma_{V(r)}$ is the slew rate of voltage during rise time, and $\sigma_{V(f)}$ is the slew rate of voltage during

fall time. The C_{out} is the output capacitor, and I_{sink} is the gate sinking current. From Figure 3.6 I_{sink} is defined as,

$$-I_{sink} = C_{out}\frac{dV_{out}}{dt} \tag{3.9}$$

$$\sigma_{V(f)} = -\frac{I_{sink}}{C_{out}} \tag{3.10}$$

From Equation 3.10, the slew rate during fall time (σ_f) depends on sinking current I_{sink}. Therefore, the sinking circuit is proposed to increase the slew as shown in Figure 3.6.

The gate driver efficiency is vital for system efficiency and industrial feasibility. The third voltage generation state is low dropout regulator (LDO); therefore, the LDO Efficiency (η_{LDO}) is given as,

$$\eta_{LDO} = \frac{V_{out}}{V_{in}} \tag{3.11}$$

The minimum voltage necessary for the shoot-through is around ≈ 3 V for SiC MOSFET [86]. From Equation 3.11, the gate driver's efficiency depends on the LDO's efficiency. LDO has a higher loss share in the gate driver than other components. For the gate voltage of 3.3 V, the efficiency becomes $3.3\,\mathrm{V}/15\,\mathrm{V}$ becomes 22%. For higher gate voltage, the efficiency is higher 10 V efficiency becomes 10 V/15 V= 66.67%).

The gate driver IC's Under Voltage Lock Down (UVLO) function prevents driving the MOSFET's gate with $V_{st} < V_{UVLO}$. As a result, the Zener diode may be used in conjunction with the Gate Driver IC to obtain $V_{st} < V_{UVLO}$ output of the gate driver IC, where Vz is Zener voltage, and V_{st} is shoot-through voltage to driver gate and generate controlled shoot-through.

The shoot-through voltage after the Zener diode is given as,

$$V_{st} = V_{out} - V_z \tag{3.12}$$

The saturation of the LDO prevents V_{st} from reaching the voltage provided by the power supply, i.e., V_{cc}, due to the dropout voltage necessary for optimal LDO functioning. Since components such as resistors, capacitors, and so on are not equal even

when manufactured in identical batches, the difference in the shoot-through voltage (third-level voltage) of HS and LS gate drivers may vary. This issue might be solved by adjusting reference voltage ($V_{st_{ref}}$) for each gate driver. Due to the lower threshold voltage of SiC MOSFETs, a shoot-through voltage in the 3 V range is anticipated. With this reduced voltage, however, the gate driver IC enters a voltage lockout condition (UVLO). As a result, the Zener diode generates a shoot-through voltage lower than the UVLO of the gate driver IC [36].

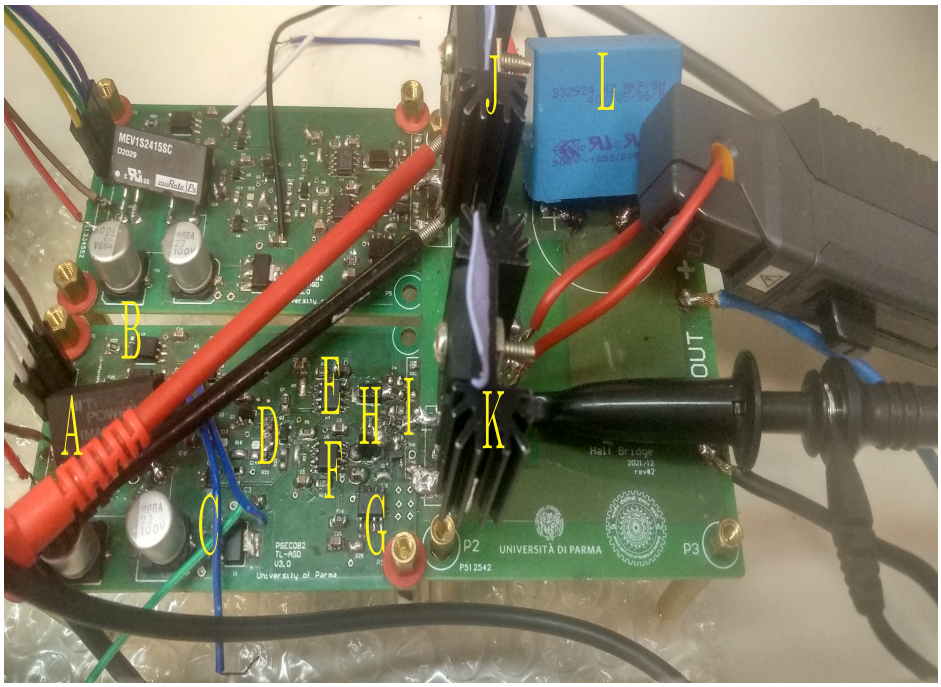


Figure 3.9: Three level two-degree-of-freedom active gate driver (TL-2DoF-AGD). A: Isolated DC-DC power supply (24V - 15V), B: Optocouplers, C: LDO for 5V logic (15V-5V), D: Third-level voltage generation stage, E: Fixed gate voltage IC (15V), F: ST gate voltage IC, G: Gate driving IC for gate charge sinking small signal MOSFET, H: Schottky diodes, I: Gate resistors, J: High side MOSFET, K: Low side MOSFET (DUT), L: DC-link capacitor

3.5 Architecture of Three-level Two Degree of Freedom Active Gate Driver (TL-2DoF-AGD)

The architecture and control logic for the active gate driver is shown in Figure 3.10 and Figure 3.10, respectively. Section 3.1 discusses the design of various stages of the gate driver. To control the gate driver, the enable (EN), PWM (for conventional operation), PWM-ST (for shoot-through operation), PWM-$V_{st,ref}$ for PWM controlled LDO to generate third-level (shoot-through) voltage. When the high side MOSFET is in the saturation region, the LS MOSFET is in a linear region but with lower gate voltage. In this case, due to the higher on-state resistance of LS MOSFET, the heating on the LS happened in a controlled way. The diode D_{sch1} and D_{sch2} are required to avoid clamping of output voltages of conventional and shoot-through gate driver ICs. A separate gate driver IC is used to sink the gate current. This can also be done by using an optocoupler.

3.6 Worst case analysis (WCA)

The shoot-through voltage is vital in the controlled shoot-through technique. The excessive gate voltage can damage the power device (provided that the shoot-through duration exceeds the allowable short circuit duration or maximum junction temperature). Therefore knowing about the tolerances effect on the shoot-through voltage becomes very important.

The worst-case analysis for PWM controlled stage is done in the subsection. The $\pm$ 10% tolerances of capacitors and resistors are considered for the simulation. For the circuit diagram, as shown in Figure 3.12, the ideal output voltage is 4.5 V. With $\pm$ 10% the shoot-though voltage (V_{st}) varies from 4.90 V to 4 V. The lower shoot-through voltage will not damage the power MOSFET, but the high shoo-through voltage may damage it.

$$V_{st} = V_{ref}\frac{R_2 + R_1}{R_2} = 3V \cdot \frac{1k + 2k}{2k} = 4.5V \tag{3.13}$$

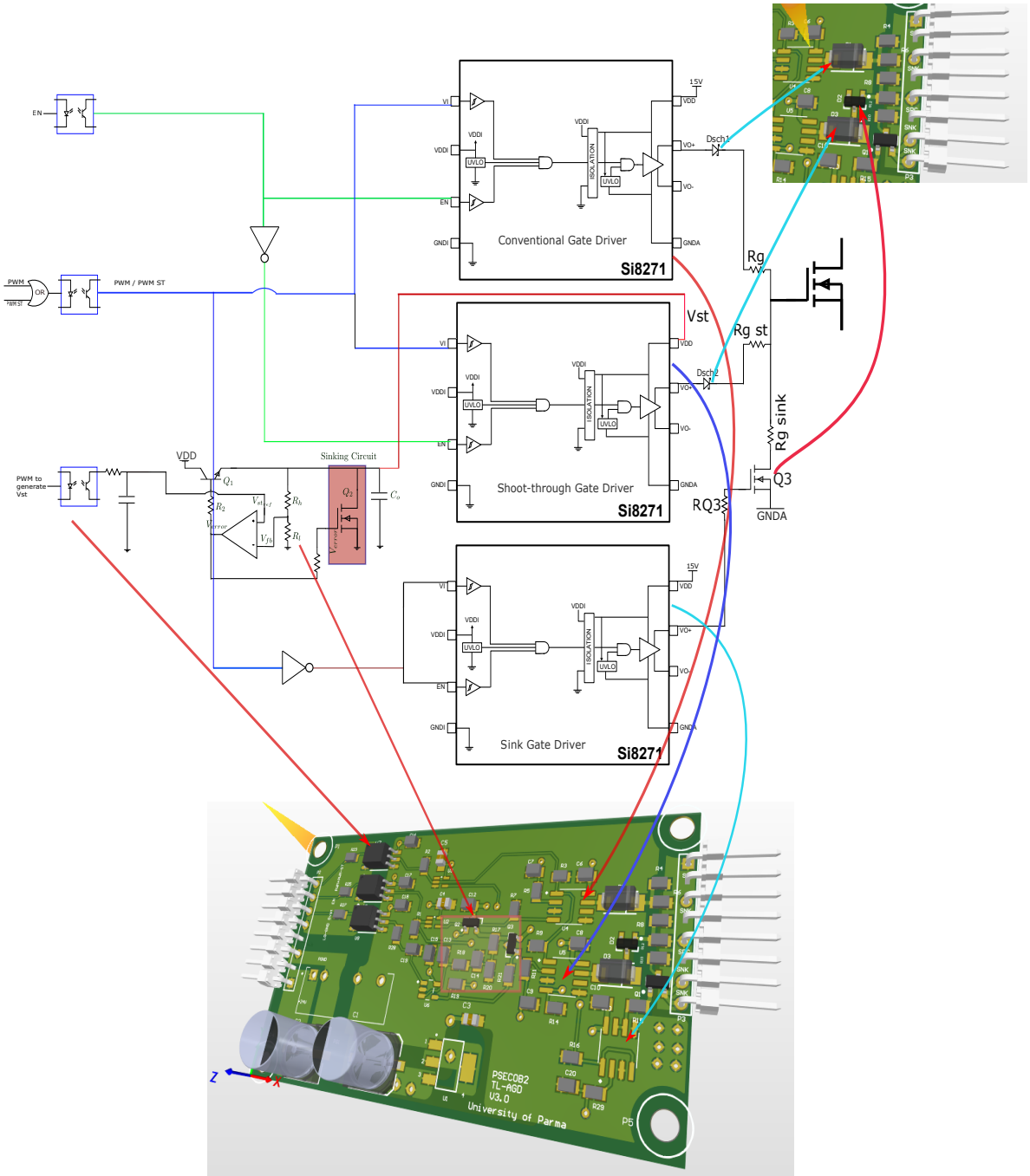


Figure 3.10: Architecture of Three-level two-degree-of-freedom Active Gate Driver (TL-2DoF-AGD).

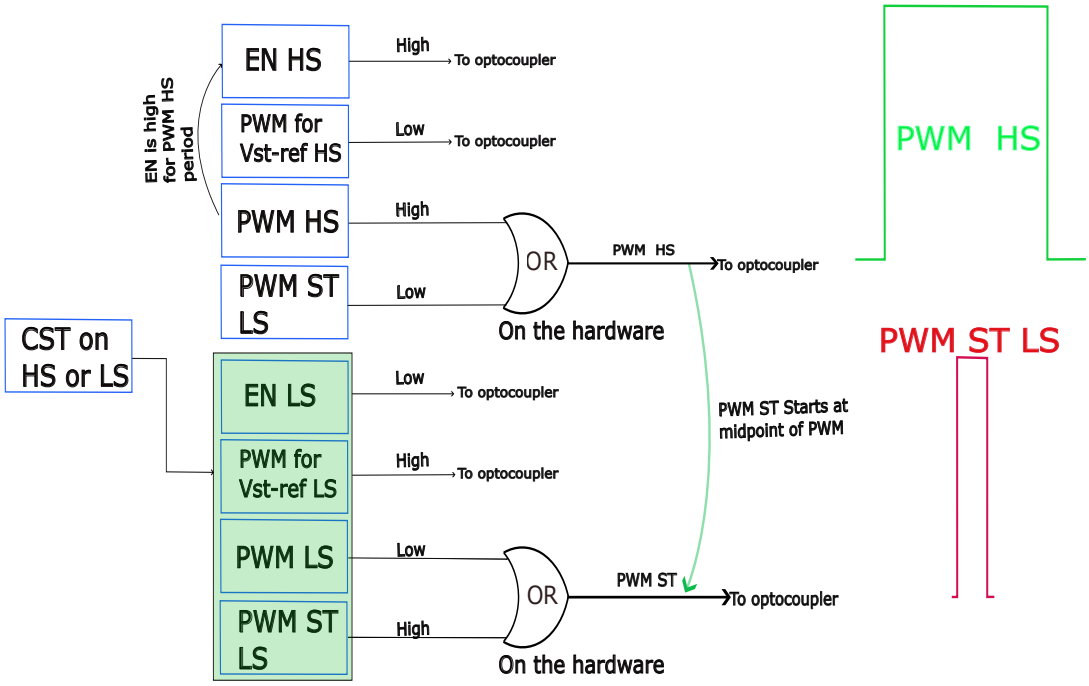
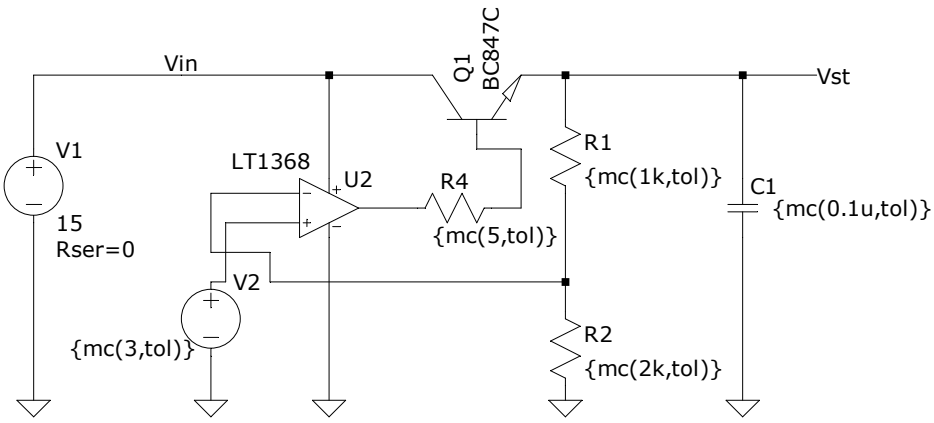


Figure 3.11: Control signals for the gate driver




```
.param tol=0.1
.function wc(nom,tol) if(rum==1, nom, if(flat(1)>0,nom*(1+tol),nom*(1-tol)))
.step param run 1 100 10
.tran 10m
```

Figure 3.12: Circuit diagram for worst case analysis for shoot-through voltage generation stage. Component tolerances $\pm$ 10%.

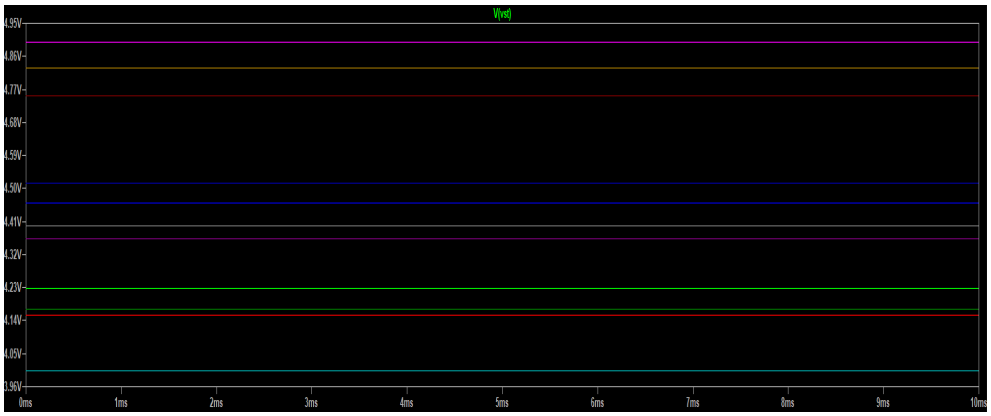


Figure 3.13: Results for worst case analysis with $\pm$10% tolerances in the resistors (R1, R2, R4) and capacitor (C1).

3.7 Small signal model and stability analysis

The simulation circuit for the stability analysis of the third-level dynamic gate voltage generation stage is shown in Figure 3.15. The stability analysis of the third-level dynamic gate voltage generation stage is important to know the switching frequency of the third-level gate voltage. The small signal model of the third-level dynamic gate voltage generation stage (also termed as "PWM controlled LDO stage") is shown in Figure 3.14. The small signal model of the third-level dynamic gate voltage generation stage, the transfer function (TF), is written as,

$$TF = \frac{V_{out}}{V_{in}} \tag{3.14}$$

Where V_{out} and V_{in} are output and input voltages of the third-level voltage generation stage. The V_{out}= V_{st} and $V_{st_{ref}}$ is reference voltage to the PWM-controlled LDO The output voltage is third-level dynamic gate voltage (i.e., shoot-through voltage) and the input voltage is the reference voltage from the RC filter (Digital to Analog converter).

Therefore the Equation 3.14 becomes,

$$TF = \frac{V_{st}}{V_{st_{ref}}} \tag{3.15}$$

The transfer function becomes,

$$TF = \frac{G(s)}{1+G(s)H(s)} \tag{3.16}$$

From Figure 3.16, the transfer function becomes,

$$TF = \frac{R_z + R_c + \frac{1}{Cs}}{1 + \left(\frac{R_l}{R_h+R_l}\right) \cdot \left(R_z + R_c + \frac{1}{Cs}\right)} \tag{3.17}$$

The pole-zero analysis of Equation 3.17 is shown in Figure 3.17.

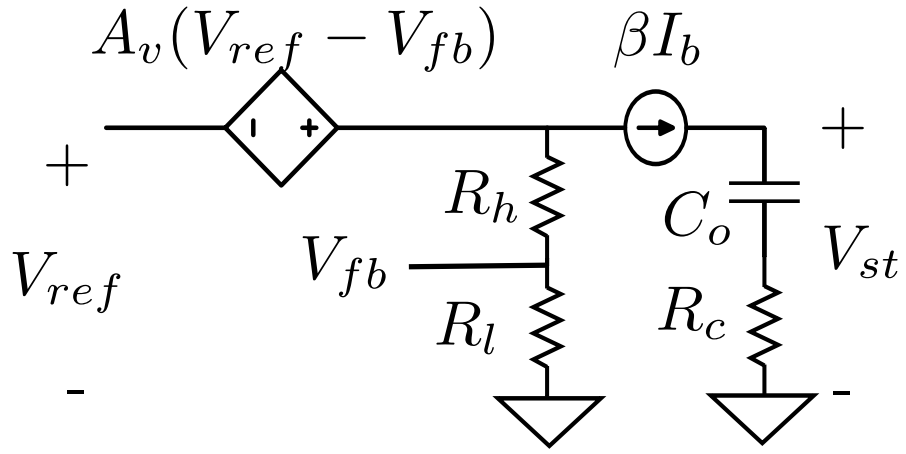


Figure 3.14: Small signal model of dynamic third level gate voltage generation stage.

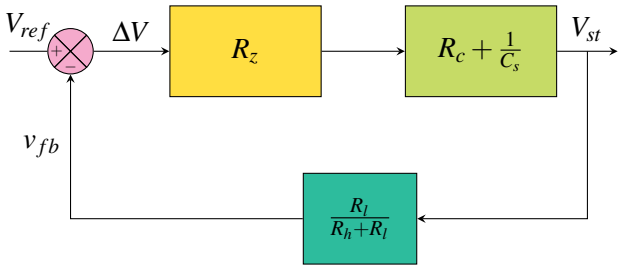


Figure 3.16: Block diagram of small signal model.

3.8 Parasitic turn-on (PTO) of MOSFET

In power electronics, low-side false turn-on is a common phenomenon, as shown in Figure 3.18. This is also known by various names as "$\frac{dv}{dt}$ induced turn-on", "spurious turn-on","unintentional turn-on", and "parasitic turn-on" is a common occurrence and shown in Figure 3.18. This false turn-on can potentially damage the MOSFET and affect the overall converter's reliability.

Any unexpected gate voltage during a controlled shoot-through can damage the

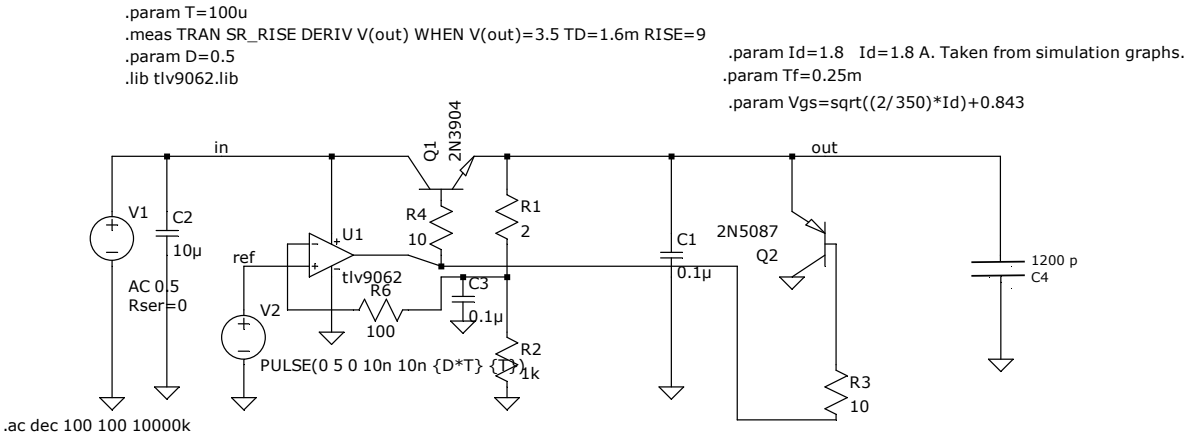


Figure 3.15: Stability analysis of third-level dynamic gate voltage generation stage.

power device. This subsection discussed the relation between gate resistance and induced false turn-on voltage. In the developed gate driver, the negative voltage rail is not used. However, in almost all SiC MOSFET-based converters, the negative power supply rail is used. Variable gate voltage with negative rail can be developed as a future work of this thesis.

Parasitic turn-on happens when the low-side switch's drain-to-source voltage rapidly rises and the high-side switch triggers. This rapid voltage rise creates a displacement current of $C \cdot \frac{dv}{dt}$ and affects the voltage across the Miller capacitance (C_{gd}), a parasitic capacitance that resides between the drain and the gate as shown in Figure 3.19. The displacement current causes the gate and source to create a voltage greater than V_{th}, which causes the rectifying switch to unintentionally turn on as shown in Figure 3.18.

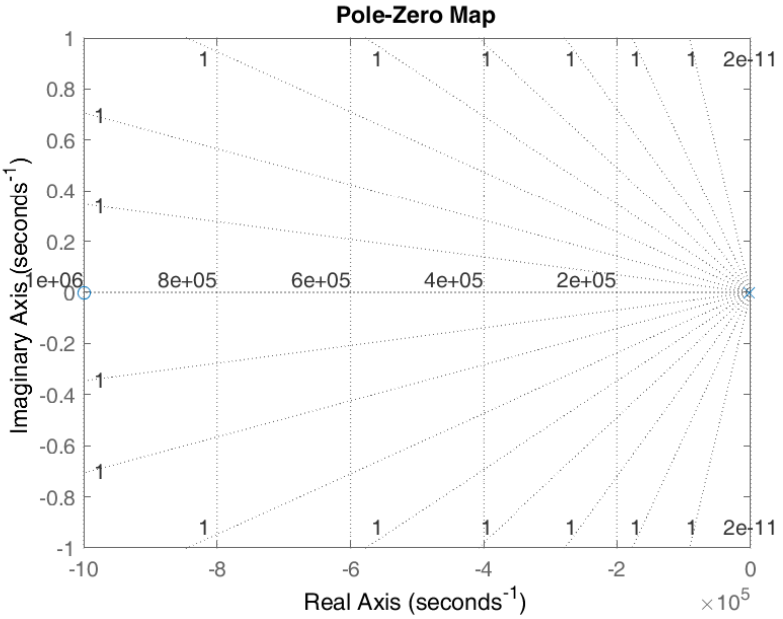


Figure 3.17: Pole zero analysis of third-level dynamic gate resistance generation stage.

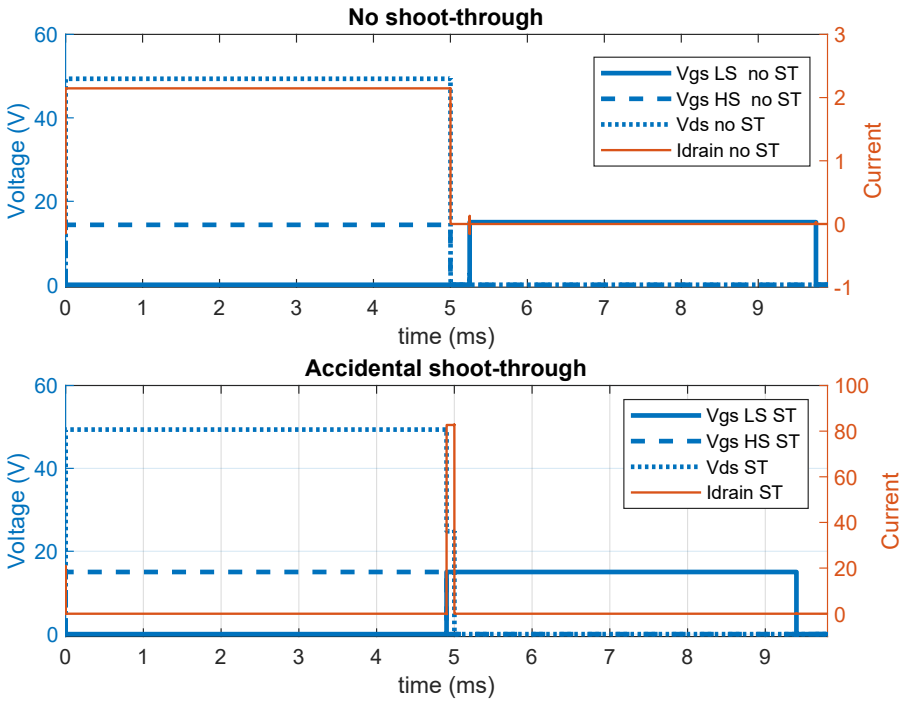


Figure 3.18: Accidental shoot-through of leg. ST: shoot-through, I_{drain}: Drain current.

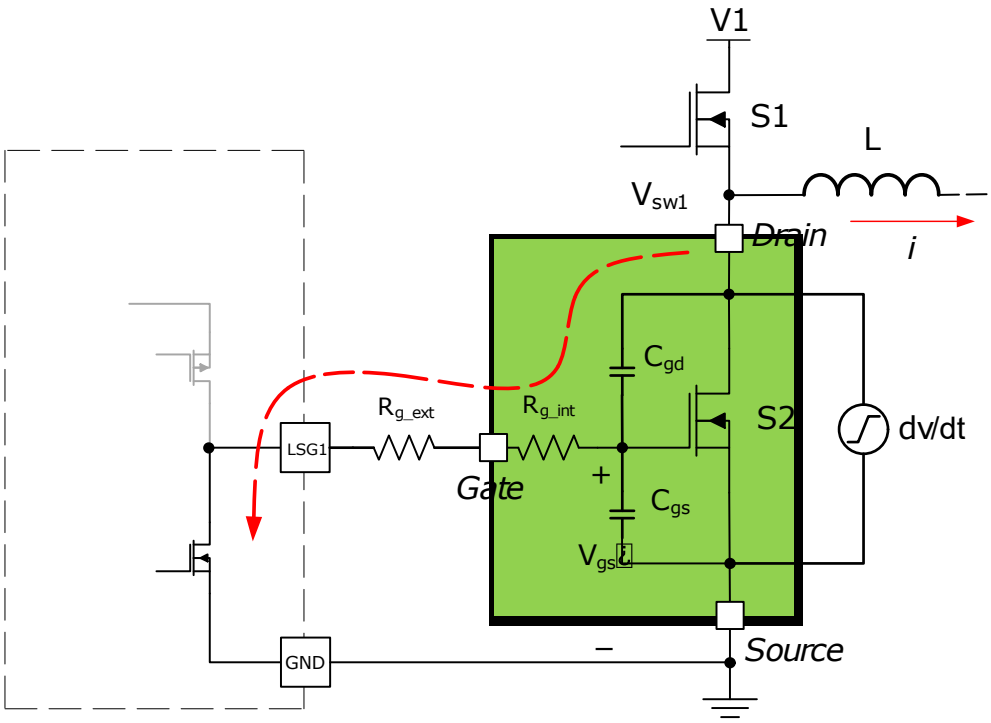


Figure 3.19: Charging of miller capacitance and inducted voltage higher than threshold voltage

It is crucial to accurately calculate the additive losses due to the controlled shoot-through technique. However, due to the self-turn-on phenomenon, the MOSFET can turn on during the commutation of the HS MOSFET. This results in additional uncontrolled losses.

When drain voltage is applied across the MOSFET, the drain gate current flows and is given as,

$$i = C_{gd}\frac{dv}{dt} \tag{3.18}$$

As a results the induced gate voltage is given as,

$$v_{gs} = R_g C_{gs}(1 - exp\left(\frac{-t}{(C_{gs}+C_{gs})R_g}\right) \tag{3.19}$$

From Equation 3.19, the gate resistance R_g is important for the voltage build-up for spurious turn-on. The effect of gate resistance on spurious turn-on voltage is shown in Figure 3.20. An increase in gate resistance up to 5 Ω results in a sharp increase in the inducted gate voltage. The SiC MOSFETs have a lower turn-on voltage. Therefore, gate resistance of 5 Ω can generate threshold voltage and result in uncontrolled shoot-through of the leg. From Figure 3.20, the spurious turn-on voltage also increases with an increase in gate resistance value.

3.9 Limitations of the proposed Three-level Two-degree-of-freedom Active Gate Driver (TL-2DoF-AGD)

The proposed TL-2DoF-AGD gives fine control over gate voltage by changing the PWM duty cycle as shown in Figure 3.10. However this gate driver also has limitations and summarized as below.

- **Voltage drop in the third-level gate voltage generation:** The third-level gate voltage (also called dynamic gate voltage generation) is generated using PWM-controlled LDO. The voltage drop in the LDO can not be avoided for the operation purpose. The voltage drop must be considered while selecting the gate voltage for the application.

- **Input-output voltage:** The input voltage to the third-level voltage generation stage should be higher than output.

- **Negative gate voltage:** The gate driver does not have the capability to give negative gate voltage during OFF conditions. However, it can be integrated into the future version of the gate driver.

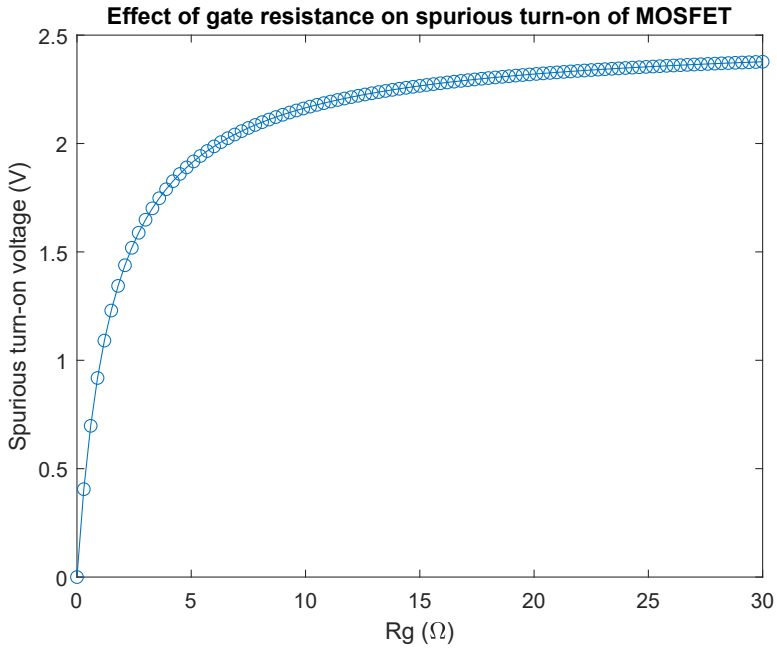


Figure 3.20: Spurious turn-on voltage with increase in gate resistance (R_g) (simulation).

3.10 Summary

Chapter 3 gives details about hardware implementation for TL-2DoF-AGD. The design parameters for the gate resistors, third-level gate voltage generation stage, nonlinearity in optocoupler, load model, isolated dc-dc gate driver power supply are discussed. The architecture of the proposed gate driver is shown in Figure 3.10. The worst case and stability analysis are also done. The gate driver exhibit limitations such as drop in the output voltage, non-availability of the negative gate voltage.

Chapter 4

Results

The progress and development of man are of immeasurable importance for humanity and are essentially dependent on invention.

– Nikola Tesla

In this chapter, the results for the controlled shoot-through technique with 3 V, 7.5 V series Zener diode and without Zener diode are discussed. The results are collected at case temperature T_c=80 °C. The results are collected at drain to source (V_{ds}) at 100 V and 300 V. The transfer characteristics are plotted for different V_{ds} and series Zener diodes.

The effects of a series Zener diode on a controlled shoot-through current are discussed in this chapter. The simulation and experimental results of the effect of self-heating on CST current shape are discussed. The optocouplers are used to get optical isolation (3.7 kV r.m.s.) between the control and power section as shown in Figure A.5 [87]. The PWM control signal is required to control the duty cycle of the reference voltage generation.

4.1 CST current due to transient impedance of Zener diode and self-heating

In a two-level active gate driver, the series Zener diode is used to vary the gate voltage as shown in appendix A.1 and A.2. The transient impedance of the series Zener diode alters the gate sourcing current as discussed in Subsection 2.0.1. Resulting in the change in the V_{gs} and drain current shape.

This also results in a change in the loss model. The effect of transient impedance of series Zener diode is seen by plotting transfer characteristics as shown in Figure 4.4. The 3 V Zener diode offers higher transient impedance as shown in Figure 2.2 and Figure 2.9. Therefore, the shape of the shoot-through current is parabolic. This affects the loss model of the controlled shoot-through technique as discussed in Chapter 2.

The 7.5 V Zener diode offers lower transient impedance than 3 V Zener diode. Therefore, the shoot-through current is almost a square wave, as shown in Figure 4.2 and Figure 4.3.

As discussed, the Zener diode's transient impedance alters the gate current's shape and eventually drain current of the MOSFET. The Three-level two-degree-of-freedom active gate driver (TL-2DoF-AGD) has PWM-controlled third-level voltage generation and can generate up to 3.2 V (operation below this voltage limited by UVLO of gate driver IC). Therefore, a series Zener diode is not required.

TL-2DoF-AGD allows shoot-through current to follow gate to source voltage V_{gs} path. The shape of the gate to source voltage is almost a square wave, and the shape of the shoot-through current is also almost a square wave, as shown in Figure 4.2 and Figure 4.3. The direct model is used due to the square wave of the shoot-through current. The most accurate losses can be estimated due to the applicability of the direct model.

With the increase in the drain to source voltage (V_{ds}), the shoot-through current increases resulting in a rise in the junction temperature (T_j). The rise in junction temperature causes a decrease in mobility carrier and hence an increase in the on-state resistance of MOSFET. The shape of the shoot-through current starts to invert

from the inflection point mentioned in Equation 2.20. The self-heating causes an increase in the on-state resistance of the MOSFET as explained in Equation 2.12. This results in a dynamic change in the shoot-through current.

Therefore, the self-heating effect on the shape of the shoot-through current is important for the accurate calculation of controlled shoot-through losses. The simulation for the analysis of the self-heating effect on drain current is done in SIMPLIS/SIMetrix® as shown in Figure 4.1. The advanced (referred to as Level-3) electro-thermal model of MOSFET IRPP65R045C7 by Infineon® is used for controlled shoot-through simulation. When junction temperature is tied to a constant temperature, the shoot-through current (blue dash line) is constant, as shown in Figure 4.1 (Die to Case thermal impedance will not allow it in the real application).

In Figure 4.1, the junction temperature T_j is not tied to a constant voltage source and is shown as a magma line. The dynamic high shoot-through current causes a decrease in mobility carrier. This results in an increase in the on-state resistance of the MOSFET (self-heating). This explains the change in the controlled shoot-through current shape.

The IRPP65R045C7 MOSFET L3 model in SIMPLIS/SIMetrix® is used to analyze self-heating on controlled shoot-through current. For experimental validation Wolfspeed® C2M0080120D is used.

By considering self-heating, the experimental results are shown in Figure 4.2. When the drain to source voltage V_{ds} is 100 V, the shoot-through current with a 3V zener diode is almost triangular (approximation). Similarly, 7.5 V series Zener diode case, the shoot-through current shape follows gate voltage. Without a series Zener diode (with TL-2DoF AGD), the drain current follows gate voltage.

For V_{ds} = 300 V, high controlled shoot-through current flows for 7.5 V series Zener diode case and without Zener diode case. The shape of the controlled shoot-through current does not follow the gate current shape (square). The CST current has a positive slope. This means the on-state resistance is higher than V_{ds} = 100 V case. This increase in on-state resistance of the MOSFET is defined as "self-heating".

The junction temperature when drain to source voltage is 100 V and 300 V is seen in Figure 4.5, and it's effect on transfer characteristics is shown in Figure 4.4. The

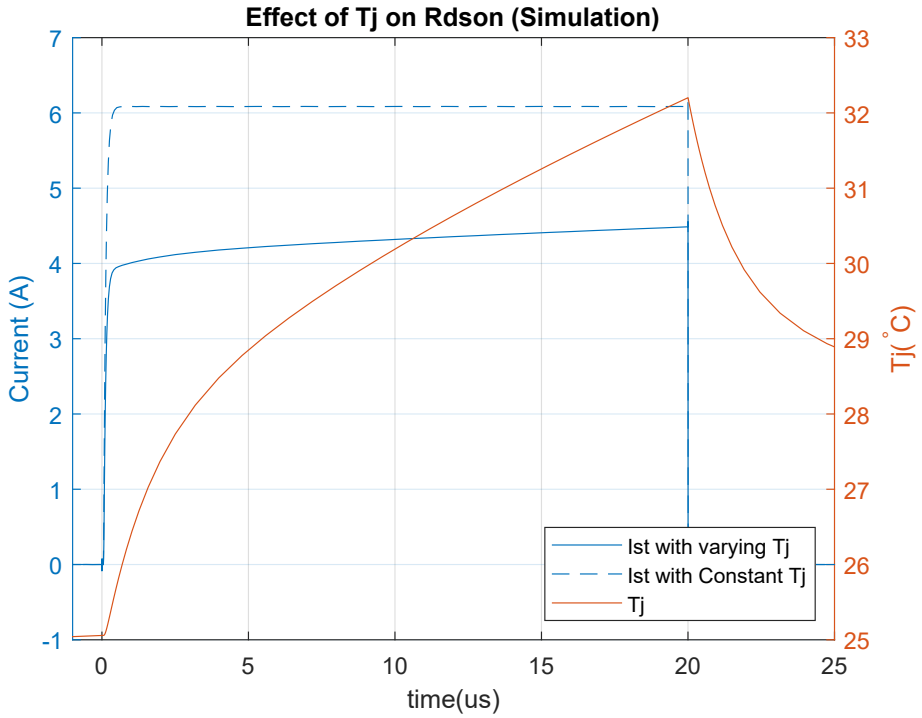


Figure 4.1: Electro-thermal simulation of IRPP65R045C7 MOSFET in SIMPLIS/SIMetrix®: $R_{ds_{on}}$ changes with junction temperature due to self-heating. Dashed blue line: T_j at constant temperature, Blue line: T_j changes due to shoot-through current, and magma line represent varying T_j due to shoot-through current. (Simulation)

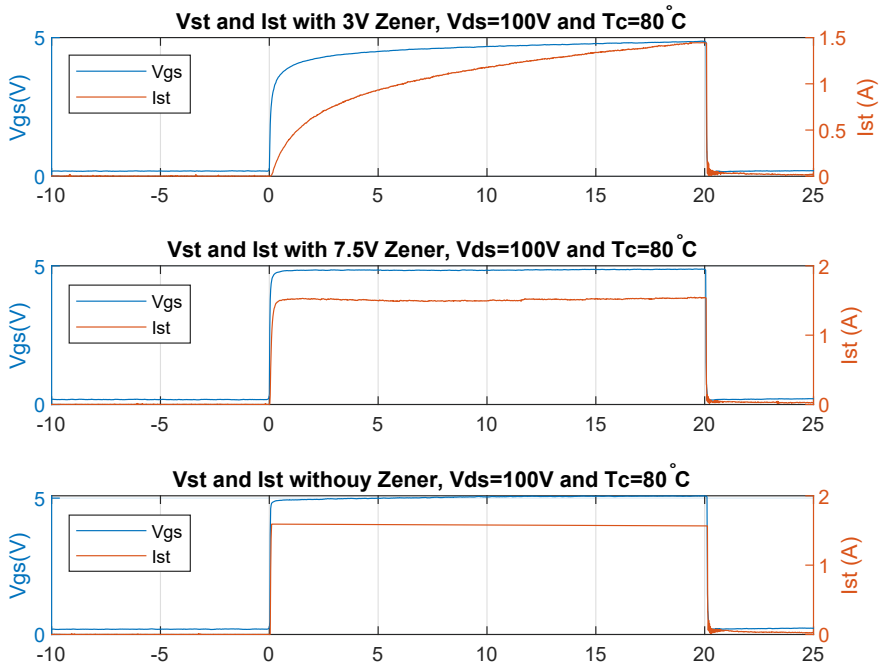


Figure 4.2: Controlled shoot-through current shape change due to presence of 3V and 7.5V series Zener diode (Experimental). Wolfspeed® C2M0080120D SiC MOSFET, Vds=100V, T_c=80 °C (Experimental). Results post-processed in MATLAB® and script is available in Appendix B.2.

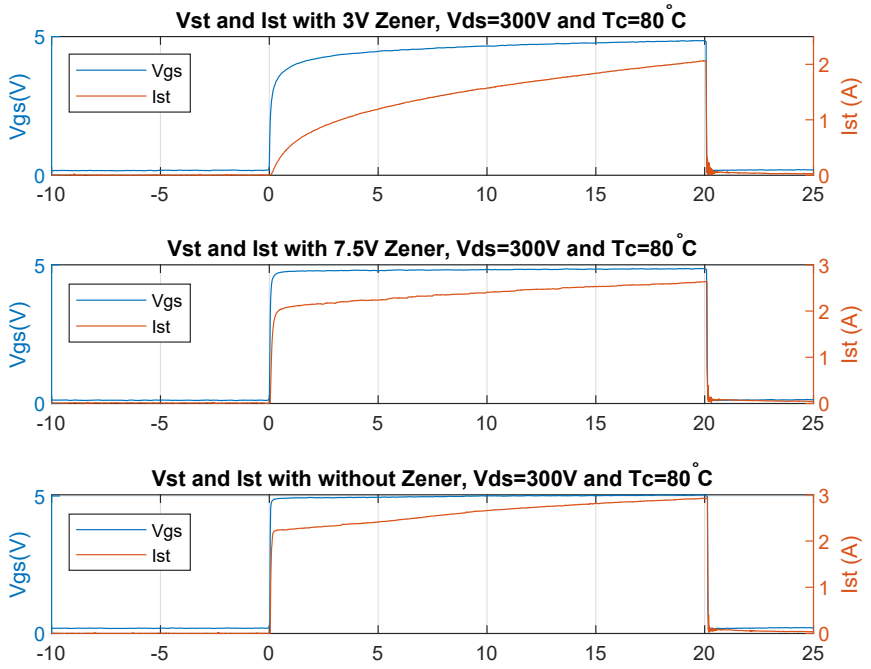


Figure 4.3: Controlled shoot-through current shape change due to presence of 3V and 7.5V series Zener diode (Experimental). Wolfspeed® C2M0080120D SiC MOSFET, Vds=300V, T_c=80 °C. Results post-processed in MATLAB® and script is available in Appendix B.2.

rise in junction temperature from 80 °C to 104 °C (as shown in Figure 4.5) cause self-heating of devices without Zener diode case and with 7.5 V Zener diode case. The junction temperature in 3 V series Zener diode case is lower in both cases (without Zener diode and 7.5 V Zener diode).

The experimental setup for testing TL-2DoF-AGD for a controlled shoot-through technique is shown in Figure 4.6 and Figure 4.7. The microcontroller unit (MCU) is used for the PWM logic generation. The control board has an OR GATE to combine PWM and PWM-ST (shoot-through) commands. MCU generates EN signal to enable gate signal, i.e., V_{gs}. The PWM signal (PWM-V_{st}) for reference shoot-through voltage is also generated.

These PWM, EN, and PWM-V_{st} are given to TL-2DoF-AGD. The control board and TL-2DoF are optically isolated using optocouplers. The low-side MOSFET is used as a device under test (DUT). The resistive load is used for the loading of the half-bridge.

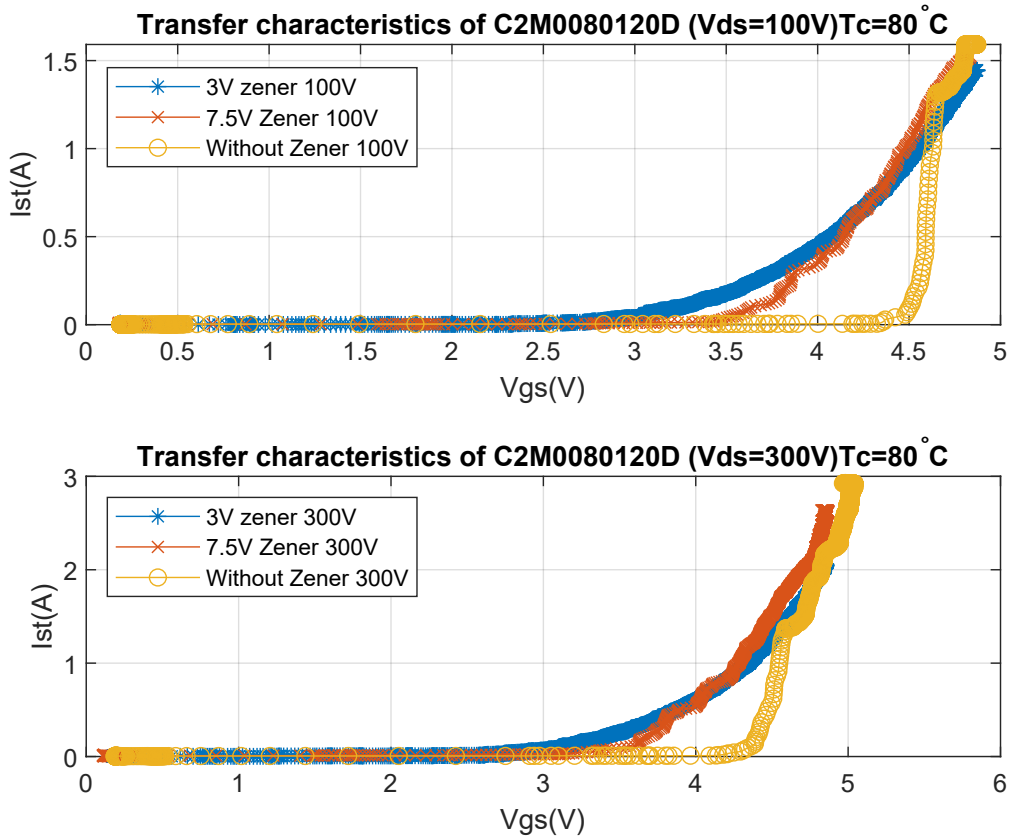


Figure 4.4: Transfer characteristics (Experimental) of Wolfspeed® C2M0080120D SiC MOSFET with 3 V, 7.5 V and without series Zener diode at 100 V and 300 V Drain to source voltage. (Experimental).

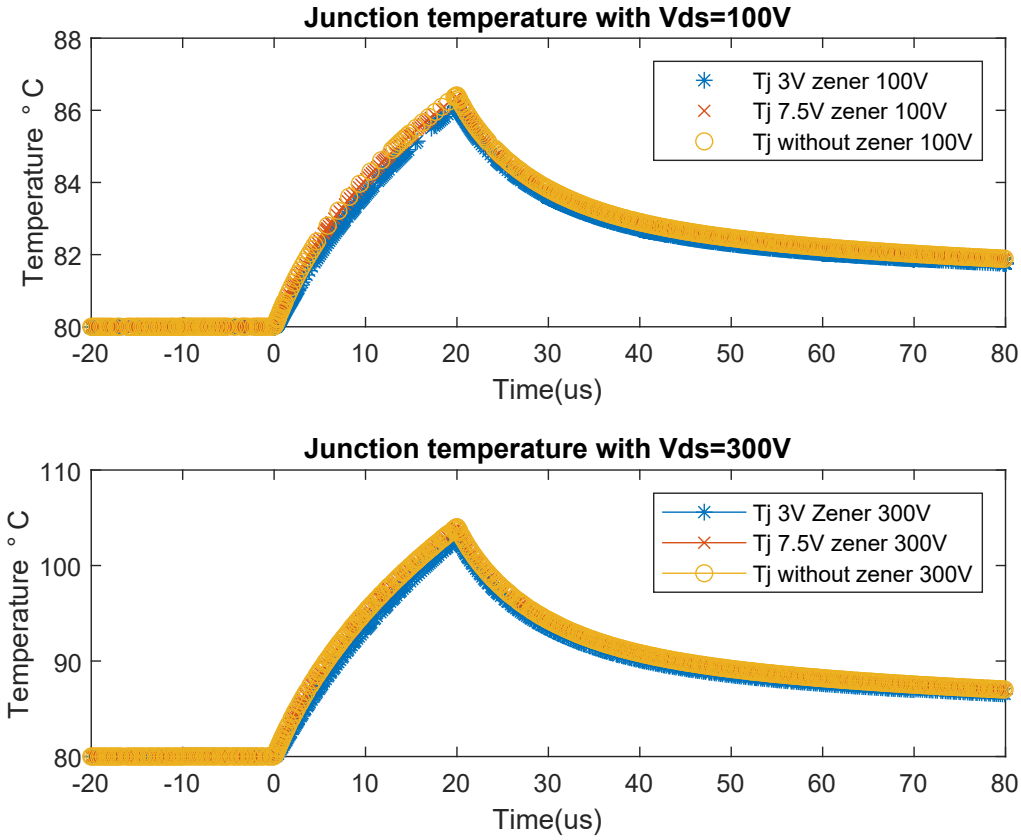


Figure 4.5: Simulation of Wolfspeed® C2M0080120D SiC MOSFET Junction temperature in LTspice® with V_{ds}=100 V, 300 V and 3 V, 7.5 V and without series Zener diode. (Simulation).

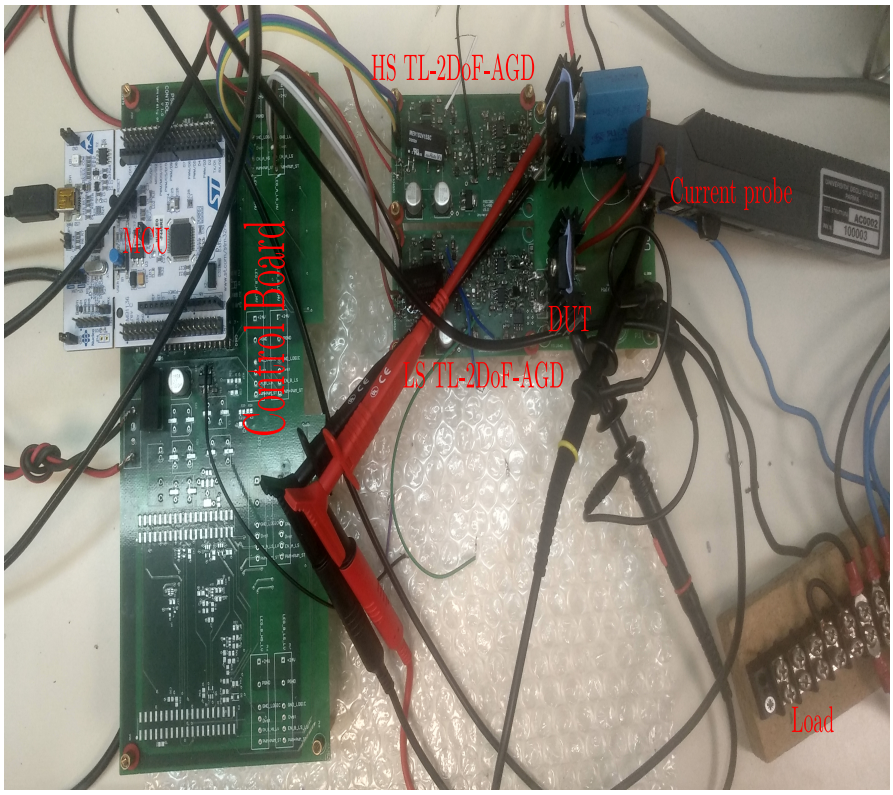


Figure 4.6: Experimental setup for testing TL-2DoF-AGD for controlled shoot-through technique. Setup containing Microcontroller Control Unit (MCU), control board, Device Under Test (DUT), current probe and Load.

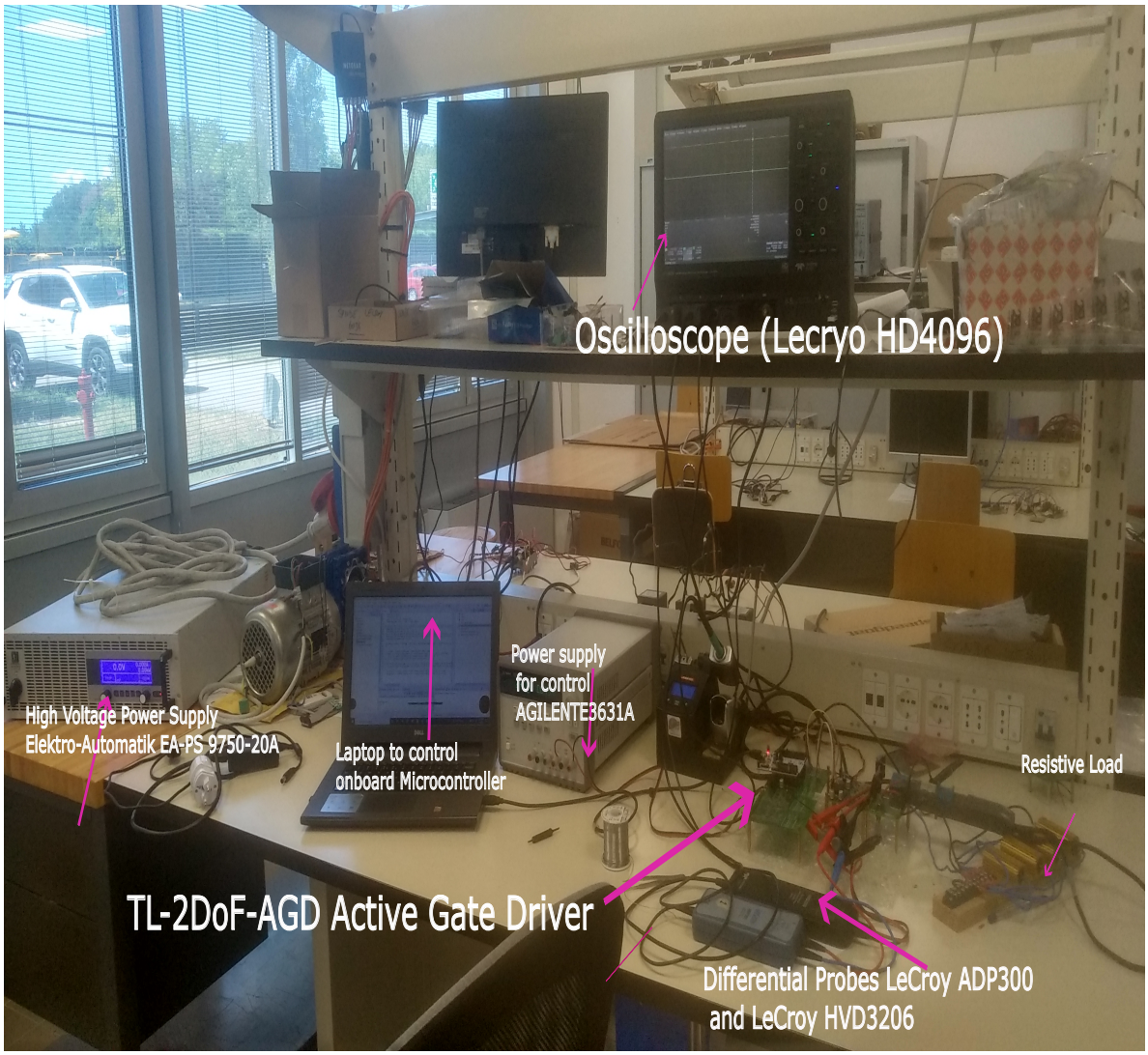


Figure 4.7: Complete experimental setup showing high voltage power supply, logic power supply, oscilloscope, gate driver and laptop to upload firmware in onboard microcontroller (STM32F446RE).

Discussion, Conclusion and Future Work

Discussion

Chapter 1 discussed different active thermal control techniques. It is classified as switching loss manipulation, loading manipulation, and convection media. The liquid-cooled power module from Danfoss was discussed. The third voltage generation stage is analyzed, and a comparison with the method implemented in this thesis is made. The proposed third-level voltage generation stage's industrial applicability is more than other methods.

The transient impedance term is defined at the initial of Chapter 2. The Zener diode effect on the gate current is analyzed. The inflection point is essential because CST operation in NTC can damage the device. Different loss models with and Without Zener diodes are analyzed. This chapter discusses the design of various components like gate resistors, power supply, and third-level voltage generation. The non-linearity of the optocoupler can give unexpected shoot-through voltage. Therefore linearity of the optocoupler is critical for the PWM-controlled LDO. The architecture and control signals for the gate driver are discussed. The architecture explains the detailed circuit of the TL-2DoF-AGD. The "sink gate driver" can be replaced with the optocoupler to reduce BOM cost. This BOM cost of a complete gate driver may impose a limitation. However, the Application Specific Integrated Circuit (ASIC) can be designed if this gate driver is used on the industrial level.

The Monte-Carlo analysis gives tolerances effect on the output stage of the third-

level voltage. The components with low tolerances should be selected for designing the third-level generation stage (PWM-controlled LDO). With the increase in the switching frequencies, the third-level voltage generation stage should be stable. Therefore, stability analysis for it is done. The false turn-on can give additive losses. Therefore, having lower gate resistance will reduce induced false turn-on voltage. However, with a negative power supply, this can be neglected.

As a result, the experimental validation of CST current shape with 3V, 7.5V Zener diode, and without Zener diode at V_{ds}= 100 V and 300 V completed. With a 3V Zener diode, the CST current shape is approximately triangular. Whereas For V_{ds}= 100 V with 7.5V Zener diode, and without Zener diode case, the drain current follows gate voltage and at 100 V, high on-state resistance is seen, it is called self-heating of the device. The experimental setup for the TL-2DoF-AGD is show in Figure 4.7

Conclusion

Increase in the temperate gradient of the junction temperature of power electronic devices, resulting in reduced life. Various active thermal control techniques are proposed in the literature to reduce the gradient from conventional air cooling to liquid cooling. Methods for heating up devices were also introduced to reduce temperature differences. A magneto-hydrodynamic pump is proposed to extract junction temperature at the chip level. As discussed in Chapter 2, the heating-up of power electronic devices does not eliminate the CST current shape change due to self-heating. However, if the heat generated at the die is removed instantly (which is not possible due to die-to-case thermal resistance), the self-heating of devices can be avoided, and the shape of the CST current shape is almost square wave as shown in Figure 4.1.

The controlled short circuit (also called controlled shoot-through) technique was proposed in [36]. This produces additive losses along with switching losses by creating a controlled short circuit. The amount of energy dissipated during a short circuit is varied by varying shoot-through duration and/or gate voltage.

While varying gate voltage in [36], the author used a series Zener diode of different combinations. This requires human interference to change the gate voltage. This method takes time and changes in the circuit. Therefore, this thesis proposes

the gate driver with dynamic shoot-through gate voltage (also termed third-level gate voltage).

The series Zener diode offers transient impedance as shown in Figure 2.2. For experimental purposes, the 3V and 7.5V series Zener diodes are selected. The transient impedance offered by the low voltage (3V) series Zener diode is higher than the higher voltage Zener diode (7.5V). Therefore, this affects the gate sourcing current and changes the gate to source voltage, as shown in Figure 2.9. Due to the high transient impedance of the Zener diode, the CST current shape is not as expected. In the case of the 7.5V series Zener diode, the CST current shape is similar to a square wave shape. The CST current is a square wave if in the absence of a series Zener diode.

However, this is true for lower currents (which do not start self-heating). The rise in junction temperature causes a decrease in the mobility carrier. This results in an increase in on-state resistance, and this phenomenon is called self-heating. Therefore, the CST current shape under the self-heating phenomenon is not a square wave or half-parabolic.The loss model by considering self-heating is proposed as Equation 2.30.

Future work

The research builds the understanding of the self-heating of SiC MOSFET and the proposed loss model by considering it. The application of CST includes heating batteries and thermo-sensitive electrical parameters. The self-heating for Si MOSFET, IGBT, and GaN devices can be studied using TL-2DoF-AGD.

- Nexperia®'s research explains that self-heating of MOSFET helps reduce drain current ringing, resulting in fewer components for passing electromagnetic compatibility tests [88]. The proposed gate driver can help in conducting experimental results in measuring an increase in dynamic on-state resistance due to the self-heating of the MOSFET.

- The self-heating phenomenon of the SiC MOSFET is analyzed in this thesis. A similar analysis of the Si-based MOSFET or IGBT can be performed. With an increase in junction temperature, the threshold voltage decreases, and the

on-state resistance of the MOSFET increases. The proposed TL-2DoF-AGD can be used to validate the self-heating phenomenon.

- Circulating current control: High current flows during synchronization of filterless parallel voltage source inverters [89]. This high current can damage the power devices. Therefore, TL-2DoF-AGD can be used to control the synchronization current. During synchronization of the parallel converter, the third-level gate voltage can dynamically vary and can limit the current. Due to reduced gate voltage, the MOS-based power devices will act as voltage-controlled current sources. After completion of the synchronization current, the traditional gate driver can be used for the operation.

- The DC-link capacitor is a must for the automotive inverter. The discharge of the DC-link capacitor is done through an external resistor; this is called the passive discharge technique. The DC-link capacitor discharged through power modules within a specified time is called the Active discharge technique [90] (also called "Weak Short-Circuit"). The DC-link capacitor must be discharged under the following conditions: 1. Accident or repair 2. Key off. According to Automotive Safety Integrity Level-D (ASIL-D), the DC-link capacitor must be discharged within 2 s [91]. The research proposed in the thesis will help implement the active discharge technique.

List of publications :

1. A. Soldati, V. Undre, R. Menozzi, "Investigation on the Thermal Stability of Silicon-carbide MOSFETs operating in Controlled Shoot-through mode", The 25th European Conference on Power Electronics and Applications, Aalborg, Denmark, September 2023 (Unpublished as on 09 July 2023).

2. A. Soldati, V. Undre, C. Concari, B. A. Alsayid and M. H. Dradi, "Parallel Operation of Voltage Source Converters without Filter Inductors: Control of the Circulating Current," 2020 2nd IEEE International Conference on Industrial Electronics for Sustainable Energy Systems (IESES), Cagliari, Italy, 2020, pp. 125-130, doi: 10.1109/IESES45645.2020.9210681.

3. M. Manganelli, V. Undre and A. Soldati, "Optimal Control of Domestic Storage via MPC: the Impact of the Prediction of User Habits, including Power Market and Battery Degradation," 2020 2nd IEEE International Conference on Industrial Electronics for Sustainable Energy Systems (IESES), Cagliari, Italy, 2020, pp. 67-72, doi: 10.1109/IESES45645.2020.9210656.

Patent:

- Alessandro Soldati, Patroncini Paolo, Vishal Undre, Dario Fusai, “Sistema per la termoregolazione attiva di batterie in uso su veicoli mediante utilizzo dei convertitori elettronici già presenti a bordo e relativo metodo di controllo”, brevetto n. 102021000003269.

Appendix A

Schematics for Three-level two-degree-of-freedom active gate driver (TL-2DoF-AGD)

A.1 Simulation circuit for different series Zener diodes

Simulation circuits for Zener diode in series for the analysis of transient impedance of Zener diodes. Figure A.1: 3 V Zener diode in series, Figure A.2: 7.5 V Zener diode in series, and Figure A.3: **NO** Zener diode in series.

The Figure 3.15 shows pole-zero compensation of feedback path for increasing phase margin and gain margin of the third-level dynamic gate voltage generation stage.

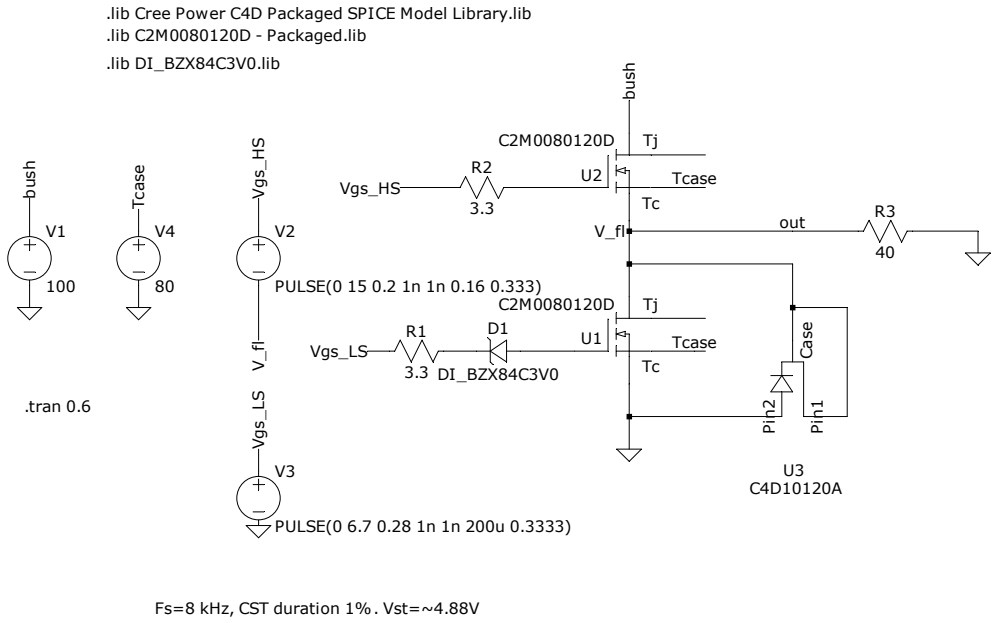


Figure A.1: 3V Zener diode in series with gate driver to generate third level gate voltage.

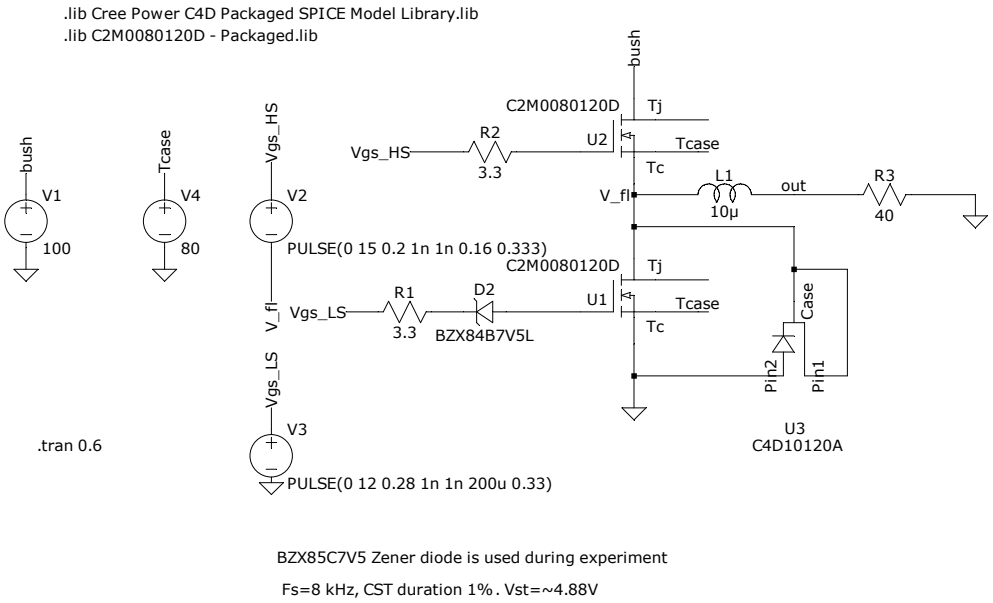


Figure A.2: 7.5V Zener diode in series with gate driver to generate third level gate voltage.

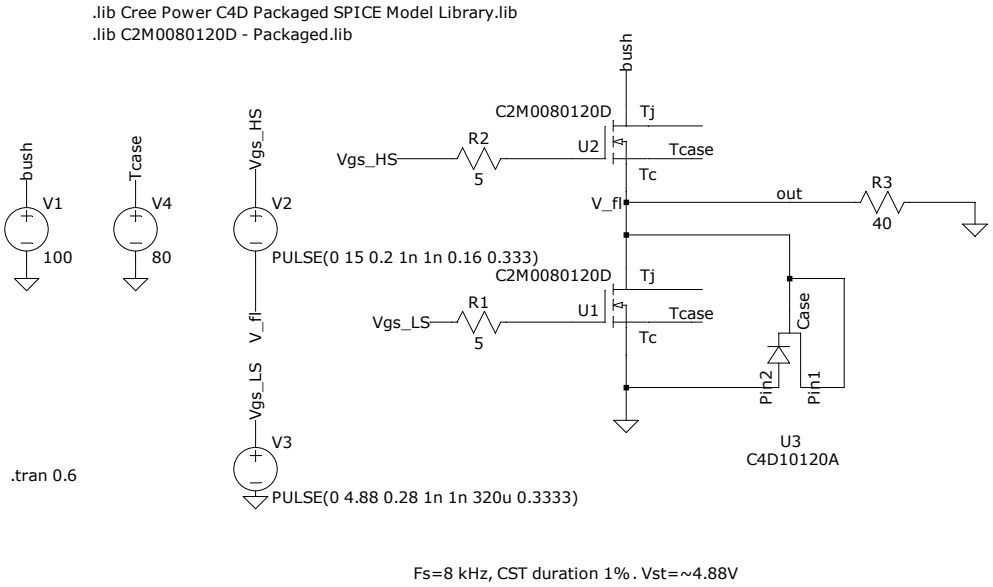


Figure A.3: Third voltage generation with Three-level two-degree-of-freedom Active Gate Driver (TL-2DoF-AGD) for third-level gate voltage generation.

A.2 Three-level Two-degree-of-freedom Active Gate Driver (TL-2DoF-AGD) schematics

The PWM and PWM ST signals are combined using **OR** gate shown in Figure A.4. The optical isolation of 3.75 kV is enforced between control signals and gate driver shown in Figure A.5.

The Figure A.6 shows schematics for the third-level dynamic gate voltage generation. Different control signals are given to gate driver IC SI8271AB as shown in Figure A.9 [85] . The traditional gate driver and shoot-through gate driver with series Zener diode is also shown. The gate charging sinking circuit pull-low the MOSFET.

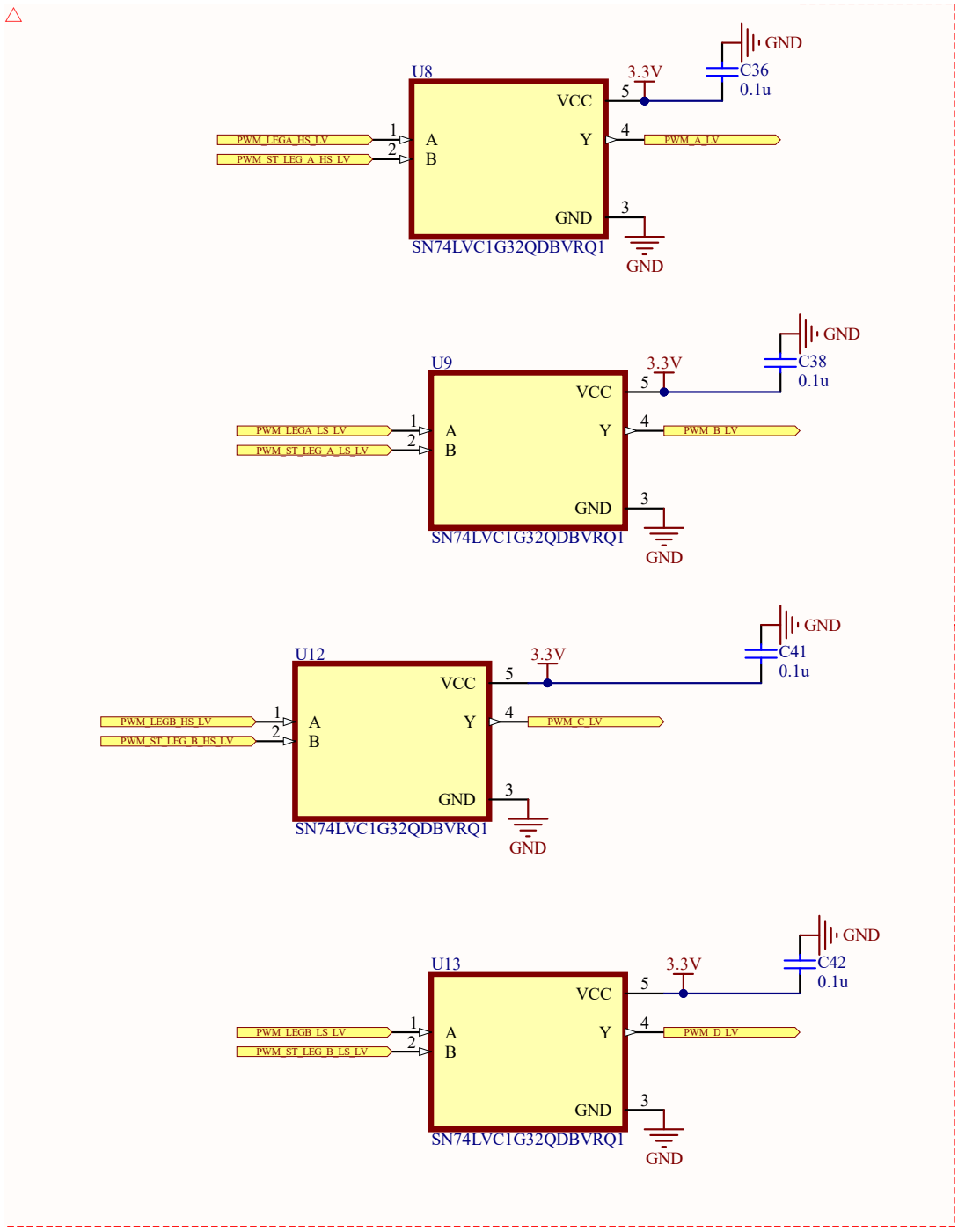


Figure A.4: PWM and PWM shoot-thorough (PWM ST) signals are combined using OR logic gate.

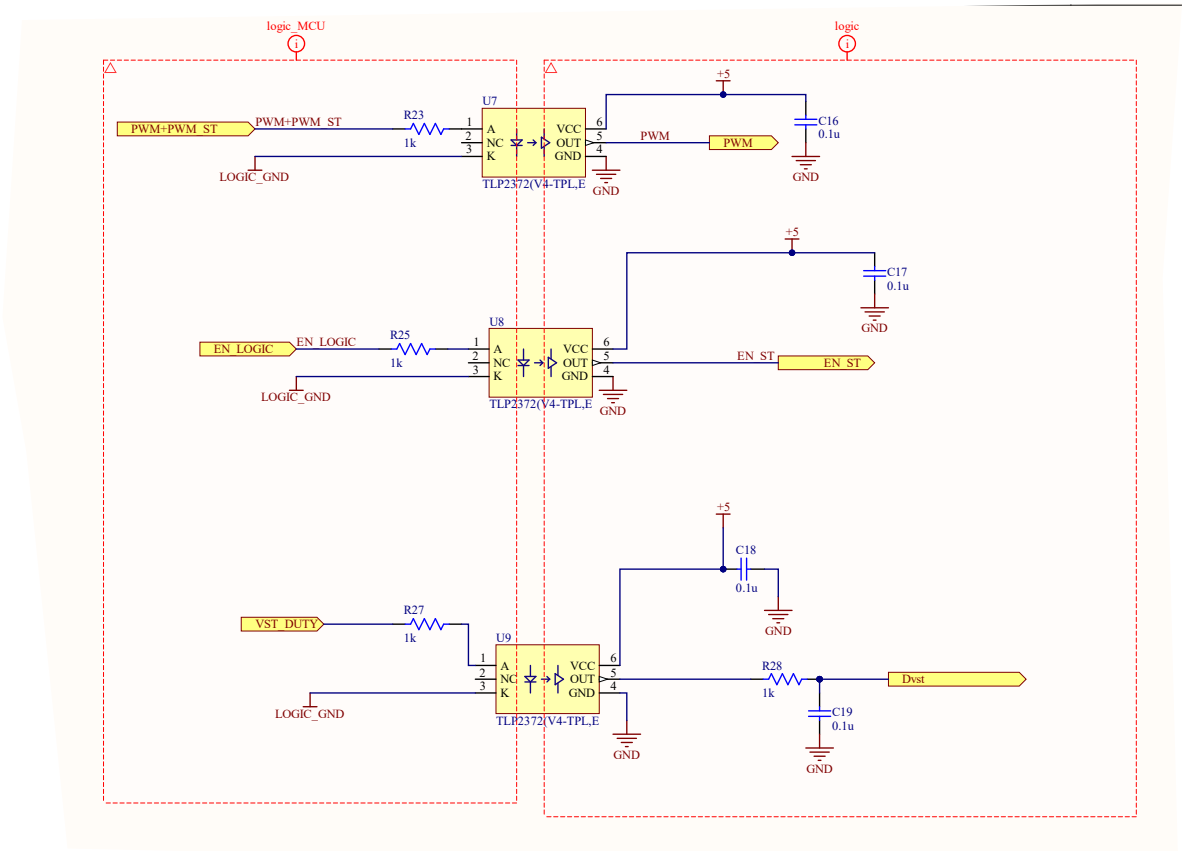


Figure A.5: Optocoupler for optical isolation between microcontroller logic and gate driver. The isolation voltage is 3.75 kV.

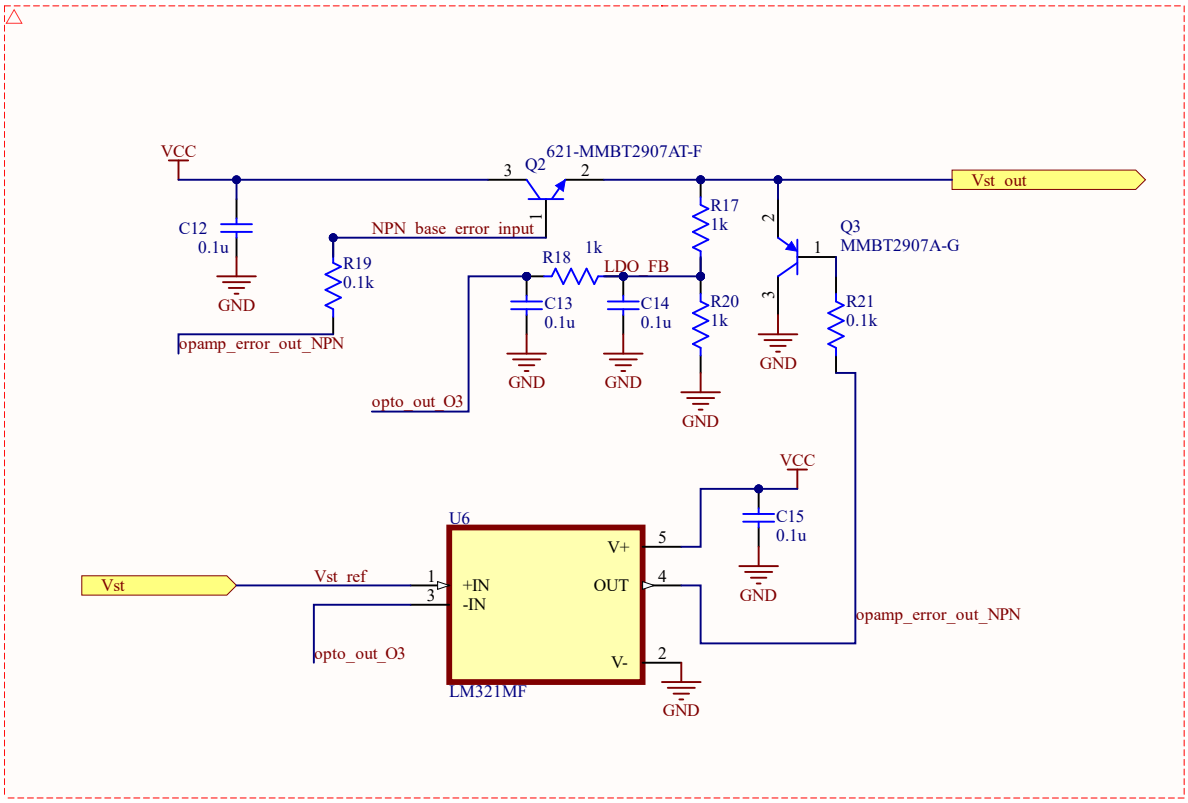


Figure A.6: Third voltage generation stage using PWM controlled low dropout regulator.

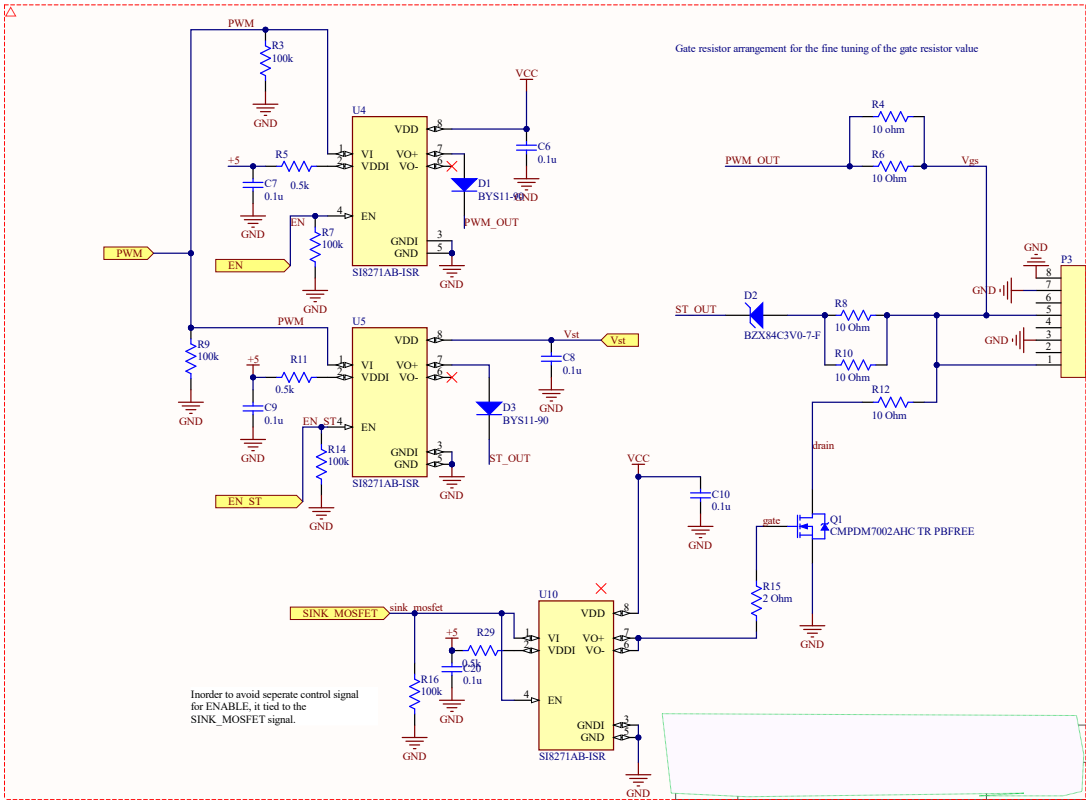


Figure A.7: Traditional gate driver IC are Third voltage gate driver IC in parallel and operate in complementary to each other. The separate gate driving IC for the sinking MOSFET.

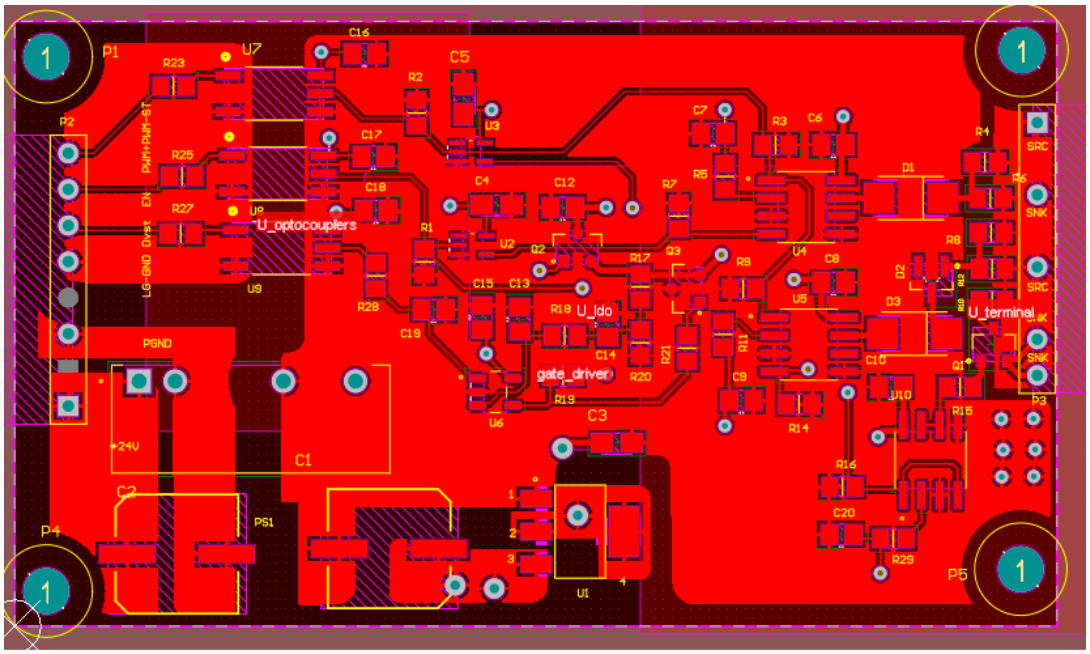


Figure A.8: TL-2DoF AGD top layer pcb layout. Design according to IPC®-2221.

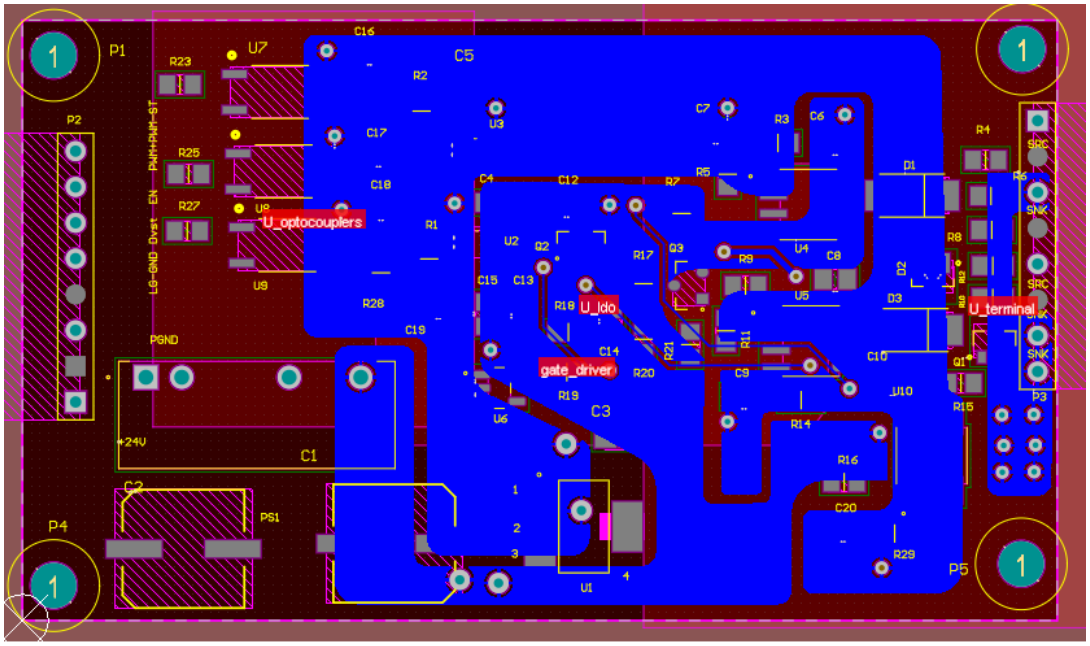


Figure A.9: TL-2DoF AGD bottom layer pcb layout

Appendix B

MATLAB scripts

B.1 Matlab script for pre-processing and post-processing of experimental data of calculation of transient impedance of Zener diode

```
% Matlab Script for the pre-processing and post-processing for finding minimum transient
    impedance
% and transfer characteristics of the MOSFET for Controlled Shoot-through Technique.
%% Cleaning
clc
clear
close all

%% Reading traces from results: With zener diode
fprintf('Readind data "With Zener" ...\n')

read_data_with_zener=readmatrix('scope_11.csv');% reading excel file % 30V
read_data_with_zener_lpf=readmatrix('scope_12.csv'); % reading excel file % 30V  %low pass
     filter (lpf) added for diff probe across Rg
time_w_z_=read_data_with_zener(:,1); % reading time axis
time_w_z=(time_w_z_)*10e6; % ms time base
I_st_w_z=(read_data_with_zener(:,2)) ; % reading Voltage across zener diode
Vzener=(read_data_with_zener(:,6)); % reading Vz
VRg_w_z=2*(read_data_with_zener(:,4));
Vgs_LS_w_z=(read_data_with_zener(:,5)); % Reading LS gate voltage Vgs LS

```

```
for m=1:length(Vgs_LS_w_z)
      if(Vgs_LS_w_z(m)<0)   % removing negative values from the Vgs
      Vgs_LS_w_z(m)=0;
      end
end

%% %%%%%%%%%%%%%%%%%%Preprocessing  %%%%%%%%%%%%%%%%%%%%%%%%%%%
fprintf('Working on pre-processing on data "With Zener" ...\n')
% Vgs_LS_w_z
Vgs_LS_w_z = fillmissing(Vgs_LS_w_z,'linear'); % Adding missing files
nanIndex_Vgs_LS_w_z = Vgs_LS_w_z<0 | Vgs_LS_w_z>13; % Replacing bad data with NaNs
Vgs_LS_w_z(nanIndex_Vgs_LS_w_z) = NaN;
OutlierIndex_Vgs_LS_w_z = isoutlier(Vgs_LS_w_z,'median','ThresholdFactor',13); %% Finding
     outliers in your data
Vgs_LS_w_z = smoothdata(Vgs_LS_w_z,'movmean',10) ;%% Smoothing noisy data

% I_st_w_z
nanIndex_I_st_w_z = I_st_w_z<0;
I_st_w_z(nanIndex_I_st_w_z) = 0;
I_st_w_z = fillmissing(I_st_w_z,'linear');
OutlierIndex_I_st_w_z = isoutlier(I_st_w_z,'median','ThresholdFactor',50);
I_st_w_z = smoothdata(I_st_w_z,'movmean',10);

% V_z
 nanIndex_Vzener = Vzener<0;
 Vzener(nanIndex_Vzener) = NaN;
 Vzener = fillmissing(Vzener,'linear');
 OutlierIndex_Vzener = isoutlier(Vzener,'median','ThresholdFactor',3);
 Vzener = smoothdata(Vzener,'movmean',5);

%V_Rg
% nanIndex_VRg_w_z = VRg_w_z<0.0019;
% VRg_w_z(nanIndex_VRg_w_z) = NaN;
% VRg_w_z = fillmissing(VRg_w_z,'nearest');
% VRg_w_z = filloutliers(VRg_w_z,'linear','median','ThresholdFactor',15);
VRg_w_z = smoothdata(VRg_w_z,'movmean',5)

fprintf('Ig, Zz calculation: "With Zener" ...\n')
src_current_w_z= VRg_w_z./3.3; % calculation of gate current. Multiply by 2 to compensate
     ration from diff probe
%
 for k=1:length(src_current_w_z)
       if(src_current_w_z(k)<=0.019) % removing values less than 0.006
       src_current_w_z(k)=0.020;
```

```
      end
 end


Zz_w_z=(Vzener./src_current_w_z); % Calculating dynamic impedance of Zener diode



%% Reading traces from results: Without zener diode
fprintf('Readind data "Without Zener" ...\n')
read_data_without_zener=readmatrix('setup_25_50V_without_zener.csv');  % reading excel
    file  % 30V
time_wout_z_=read_data_without_zener(:,1); %reading time axis
time_wout_z= (time_wout_z_)*10e6;
I_st_wout_z=(read_data_without_zener(:,2)) ;% reading gate current
VRg_wout=2*(read_data_without_zener(:,6)); % keysight probe was used .. no need to
    mulyiply by two factor

Vgs_LS_wout=(read_data_without_zener(:,5)); % Reading LS gate voltage Vgs LS

for m=1:length(Vgs_LS_wout)
      if(Vgs_LS_wout(m)<0)   % removing negative values from the Vgs
      Vgs_LS_wout(m)=0;
      end
end


%% Preprocessing Without zener diode
fprintf('Working on pre-processing on data "Without Zener" ...\n')

% Vgs_LS_wout
 nanIndex_Vgs_LS_wout = Vgs_LS_wout<0 | Vgs_LS_wout>13;
 Vgs_LS_wout(nanIndex_Vgs_LS_wout) = NaN;
 Vgs_LS_wout = fillmissing(Vgs_LS_wout,'nearest');
 OutlierIndex = isoutlier(Vgs_LS_wout,'mean','ThresholdFactor',13);
 Vgs_LS_wout = smoothdata(Vgs_LS_wout,'movmean',10);

%I_st_wout_z
nanIndex_I_st_wout_z = I_st_wout_z<0
I_st_wout_z(nanIndex_I_st_wout_z) = NaN;
I_st_wout_z = fillmissing(I_st_wout_z,'linear');
I_st_wout_z = smoothdata(I_st_wout_z,'movmean',20);
%I_st_wout_z = filloutliers(I_st_wout_z,'linear','median','ThresholdFactor',200);
%
```

```
%V_g_wout
 nanIndex_VRg_wout = VRg_wout<0.009;
 VRg_wout(nanIndex_VRg_wout) = NaN;
 VRg_wout = fillmissing(VRg_wout,'nearest');
 VRg_wout = smoothdata(VRg_wout,'movmean',5);
 %VRg_wout = filloutliers(VRg_wout,'movemean','5');



fprintf('Ig, Zz calculation: "Without Zener" ...\n')
src_current_wout_z=VRg_wout./3.3; % calculation of gate current. Multiply by 2 to
     compensate ration from diff

Z_src_path_wout_z=VRg_wout./src_current_wout_z;

%% Printing results
%% All signals
fprintf('Printing results ...\n')
%
figure(1)
subplot(2,1,1)
time_w_z_k=linspace(0,25,length(time_w_z));
time_w_z_k=time_w_z_k-0.2; % bad way to add delay



%% Plotting


% Plotting Vgs, Ist, Gate Current and Transient Impedance
figure(1)
subplot(4,1,1)
plot(time_w_z_k-12.3,Vgs_LS_w_z,time_wout_z_k-12.3,Vgs_LS_wout)
legend({'Vgs-LS-w-z','Vgs_LS-wout-z'},...
'Location','northeast')
xlabel('time (us)')
ylabel('Voltage (V)')
title('Vgs with and without zener diode')
xlim([0 1])

subplot(4,1,2)
plot(time_w_z_k-12.3,I_st_w_z,time_wout_z_k-12.3,I_st_wout_z)
legend({'Id+Ist-w-z','Id+Ist-wout-z'},...
'Location','northeast')
```

```
xlabel('time (us)')
ylabel('Current (A)')
title('Id+Ist with and without zener diode')
xlim([0 1])


subplot(4,1,3)
plot(time_w_z_k-12.3+0.046,src_current_w_z,time_wout_z_k-12.3+0.046,src_current_wout_z)
legend({'Gate-current-w-z','Gate-current-wout-z'},...
'Location','northeast')
xlabel('time (us)')
ylabel('Current (A)')
title('Gate current with and without zener diode')%
xlim([0 1])

subplot(4,1,4)
plot(time_w_z_k-12.3,Zz_w_z,time_wout_z_k-12.3,Z_src_path_wout_z)
legend({'Zz-w-z','Rg'},...
                          'Location','northeast')
xlabel('time (ms)')
ylabel('Zz (\Omega)')
title('Transient impedance Zz with and without zener diode')
xlim([0 1])
print('transient_impedance_Zz','-dpdf')


% Plotting Transfer Characteristics
for d=1:length(I_st_w_z)
      if(d>2100)   % removing negative values from the Vgs       % if(I_st_w_z(d)>30 | d
           >3110)
      I_st_w_z(d)=NaN;
      end
end



for d=1:length(I_st_wout_z)
      if(d>4000)   % removing negative values from the Vgs       %  if(I_st_wout_z(d)>26 |
            d>9000)
      I_st_wout_z(d)=NaN;
      end
end

```

```
%
figure(3)

plot(Vgs_LS_w_z,I_st_w_z,'b*',Vgs_LS_wout,I_st_wout_z,'o')
xlabel('Vgs_w_z')
ylabel('Idrain_w_z')
xlabel('Voltage (V)')
ylabel('Current (A)')
legend('Id With Zener','Id Without Zener')
title('Transfer characteristics')

hold on
grid on
```

B.2 Matlab script for pre-processing and post-processing of self-heating of CST current

```
%% Cleaning
clear
clc
close all


%% Addping path
addpath('3V zener/1kHz/3V_100V')
addpath('3V zener/1kHz/3V_300V')

addpath('7.5V zener/1kHz/7.5V_100V')
addpath('7.5V zener/1kHz/7.5V_300V')

addpath('without_zener_diode/1kHz/without_zener_diode_100V')
addpath('without_zener_diode/1kHz/without_zener_diode_300V')

%% Reading temperature data 100V
% 3V Zener
read_Ist_3V=readmatrix('C1cst_waveforms_3V_1kHz_100V00000.csv');
read_Vgs_LS_3V=readmatrix('C2cst_waveforms_3V_1kHz_100V00000.csv');
read_Vo_3V=readmatrix('C3cst_waveforms_3V_1kHz_100V00000.csv');
read_Vgs_HS_3V=readmatrix('C4cst_waveforms_3V_1kHz_100V00000.csv');

% 7.5V Zener
read_Ist_7V5=readmatrix('C1cst_waveforms_7.5V_1kHz_100V00000.csv');
read_Vgs_LS_7V5=readmatrix('C2cst_waveforms_7.5V_1kHz_100V00000.csv');
read_Vo_7V5=readmatrix('C3cst_waveforms_7.5V_1kHz_100V00000.csv');
read_Vgs_HS_7V5=readmatrix('C4cst_waveforms_7.5V_1kHz_100V00000.csv');

% Without Zener
read_Ist_wout_z=readmatrix('C1cst_waveforms_wout_z_1kHz_100V00000.csv');
read_Vgs_LS_wout_z=readmatrix('C2cst_waveforms_wout_z_1kHz_100V00000');
read_Vo_wout_z=readmatrix('C3cst_waveforms_wout_z_1kHz_100V00000');
read_Vgs_HS_wout_z=readmatrix('C4cst_waveforms_wout_z_1kHz_100V00000');

%% Reading temperature data 300V
% 3V Zener
read_Ist_3V_300V=readmatrix('C1cst_waveforms_3V_1kHz_300V00000.csv');
read_Vgs_LS_3V_300V=readmatrix('C2cst_waveforms_3V_1kHz_300V00000.csv');
read_Vo_3V_300V=readmatrix('C3cst_waveforms_3V_1kHz_300V00000.csv');
```

```
read_Vgs_HS_3V_300V=readmatrix('C4cst_waveforms_3V_1kHz_300V00000.csv');

% 7.5V Zener
read_Ist_7V5_300V=readmatrix('C1cst_waveforms_7.5V_1kHz_300V00000.csv');
read_Vgs_LS_7V5_300V=readmatrix('C2cst_waveforms_7.5V_1kHz_300V00000.csv');
read_Vo_7V5_300V=readmatrix('C3cst_waveforms_7.5V_1kHz_300V00000.csv');
read_Vgs_HS_7V5_300V=readmatrix('C4cst_waveforms_7.5V_1kHz_300V00000.csv');

% Without Zener
read_Ist_wout_z_300V=readmatrix('C1cst_waveforms_1kHz_300V00000.csv');
read_Vgs_LS_wout_z_300V=readmatrix('C2cst_waveforms_1kHz_300V00000');
read_Vo_wout_z_300V=readmatrix('C3cst_waveforms_1kHz_300V00000');
read_Vgs_HS_wout_z_300V=readmatrix('C4cst_waveforms_1kHz_300V00000');



%% Simulation data
% Add paths of the respective folders % simulation
addpath('../../../../../sim/CST_transfer_characteristics/Ltspice_sim/cst_20us')



read_data_3V_100V=readmatrix('Tj_3V_100V.txt');
read_data_3V_300V=readmatrix('Tj_3V_300V.txt');

read_data_7V5_100V=readmatrix('Tj_7.5V_100V.txt');
read_data_7V5_300V=readmatrix('Tj_7.5V_300V.txt');

read_data_wout_z_100V=readmatrix('Tj_without_z_100V.txt');
read_data_wout_z_300V=readmatrix('Tj_without_z_300V.txt');

time_Tj_3V_100V= read_data_3V_100V(:,1)*1e6-20
time_Tj_7V5_100V= read_data_7V5_100V(:,1)*1e6-20
time_Tj_without_z_100V= read_data_wout_z_100V(:,1)*1e6-20

time_Tj_3V_300V= read_data_3V_300V(:,1)*1e6-20
time_Tj_7V5_300V= read_data_7V5_300V(:,1)*1e6-20
time_Tj_without_z_300V= read_data_wout_z_300V(:,1)*1e6-20



Tj_3V_100V=read_data_3V_100V(:,2)
Tj_3V_300V=read_data_3V_300V(:,2)

```

```
Tj_7V5_100V=read_data_7V5_100V(:,2)
Tj_7V5_300V=read_data_7V5_300V(:,2)


Tj_without_z_100V=read_data_wout_z_100V(:,2)
Tj_without_z_300V=read_data_wout_z_300V(:,2)


% figure(3)
% plot(time_Tj_3V_100V,Tj_3V_100V,'*',...
%     time_Tj_3V_300V,Tj_3V_300V,'*-',...
%     time_Tj_7V5_100V,Tj_7V5_100V,'x',...
%     time_Tj_7V5_300V,Tj_7V5_300V,'x-',...
%     time_Tj_without_z_100V, Tj_without_z_100V,'o',...
%     time_Tj_without_z_300V, Tj_without_z_300V,'o-')
%
%
%
% xlabel('Time(us)')
% ylabel('Temperature \circ C')
% %xlim([-100 300])
% %ylim([0 2])
% legend({'Tj 3V zener 100V',...
%     'Tj 3V Zener 300V',...
%     'Tj 7.5V zener 100V',...
%     'Tj 7.5V zener 300V',...
%     'Tj without zener 100V',...
%     'Tj without zener 300V'},...
%     'Location','northeast')
% title('Junction temperature with different Vds and 3V, 7.5 V and NO series Zener diode')
% print('T_j_different_Vds','-dpdf')

figure(1)
tiledlayout(2,1)
nexttile
plot(time_Tj_3V_100V,Tj_3V_100V,'*',...
    time_Tj_7V5_100V,Tj_7V5_100V,'x',...
    time_Tj_without_z_100V, Tj_without_z_100V,'o')
xlabel('Time(us)')
ylabel('Temperature \circ C')
legend({'Tj 3V zener 100V',...
    'Tj 7.5V zener 100V',...
    'Tj without zener 100V'},...
    'Location','northeast')
```

```
129 title('Junction temperature with Vds=100V')
130
131 nexttile
132
133 plot(time_Tj_3V_300V,Tj_3V_300V,'*-',...
134      time_Tj_7V5_300V,Tj_7V5_300V,'x-',...
135      time_Tj_without_z_300V, Tj_without_z_300V,'o-')
136
137
138 xlabel('Time(us)')
139 ylabel('Temperature \circ C')
140 legend({'Tj 3V Zener 300V',...
141        'Tj 7.5V zener 300V',...
142        'Tj without zener 300V'},...
143     'Location','northeast')
144 title('Junction temperature with Vds=300V')
145 print('T_j_different_Vds','-dpdf')
146
147 %% Read value with condition Vds=100V
148 % 3V Zener
149 Ist_3V=read_Ist_3V(:,2);
150 Vgs_LS_3V=read_Vgs_LS_3V(:,2);
151 Vo_3V=read_Vo_3V(:,2);
152 Vgs_HS_3V=read_Vgs_HS_3V(:,2);
153
154
155 % 7.5V Zener
156 Ist_7V5=read_Ist_7V5(:,2);
157 Vgs_LS_7V5=read_Vgs_LS_7V5(:,2);
158 Vo_7V5=read_Vo_7V5(:,2);
159 Vgs_HS_7V5=read_Vgs_HS_7V5(:,2);
160
161 % Without Zener
162 Ist_wout_z=read_Ist_wout_z(:,2);
163 Vgs_LS_wout_z=read_Vgs_LS_wout_z(:,2);
164 Vo_wout_z=read_Vo_wout_z(:,2);
165 Vgs_HS_wout_z=read_Vgs_HS_wout_z(:,2);
166
167 % Reading time axis
168 time_3V=read_Ist_3V(:,1)*1e6;
169 time_7V5=read_Ist_7V5(:,1)*1e6;
170 time_wout_z=read_Ist_wout_z(:,1)*1e6;
171
172 %% Read value with condition Vds=300V
```

```
% 3V Zener
Ist_3V_300V=read_Ist_3V_300V(:,2);
Vgs_LS_3V_300V=read_Vgs_LS_3V_300V(:,2);
Vo_3V_300V=read_Vo_3V_300V(:,2);
Vgs_HS_3V_300V=read_Vgs_HS_3V_300V(:,2);


% 7.5V Zener
Ist_7V5_300V=read_Ist_7V5_300V(:,2);
Vgs_LS_7V5_300V=read_Vgs_LS_7V5_300V(:,2);
Vo_7V5_300V=read_Vo_7V5_300V(:,2);
Vgs_HS_7V5_300V=read_Vgs_HS_7V5_300V(:,2);

% Without Zener
Ist_wout_z_300V=read_Ist_wout_z_300V(:,2);
Vgs_LS_wout_z_300V=read_Vgs_LS_wout_z_300V(:,2);
Vo_wout_z_300V=read_Vo_wout_z_300V(:,2);
Vgs_HS_wout_z_300V=read_Vgs_HS_wout_z_300V(:,2);

% Reading time axis
time_3V_300V=read_Ist_3V_300V(:,1)*1e6;
time_7V5_300V=read_Ist_7V5_300V(:,1)*1e6;
time_wout_z_300V=read_Ist_wout_z_300V(:,1)*1e6;




%% Preprocessing experimental data to plot transfer characteristics Vds=100V


Ist_3V_nanIndex = Ist_3V<0;
Ist_3V(Ist_3V_nanIndex) = NaN; %% Replacing bad data with NaNs
Ist_3V = fillmissing(Ist_3V,'linear'); %% Filling missing data with using statistical
    techniques
Ist_3V = filloutliers(Ist_3V,'linear','median','ThresholdFactor',75); %% Finding and
    replacing outliers in data
Ist_3V = smoothdata(Ist_3V,'movmedian',100); %% Smoothing noisy data

Vgs_LS_3V_nanIndex = Vgs_LS_3V<0;
Vgs_LS_3V(Vgs_LS_3V_nanIndex) = NaN; %% Replacing bad data with NaNs
Vgs_LS_3V = fillmissing(Vgs_LS_3V,'linear'); %% Filling missing data with using
    statistical techniques
Vgs_LS_3V= filloutliers(Vgs_LS_3V,'linear','median','ThresholdFactor',75); %% Finding and
    replacing outliers in data
```

```
213 Vgs_LS_3V = smoothdata(Vgs_LS_3V,'movmedian',500); %% Smoothing noisy data
214
215
216
217 Ist_7V5_nanIndex = Ist_7V5<0;
218 Ist_7V5(Ist_7V5_nanIndex) = NaN; %% Replacing bad data with NaNs
219 Ist_7V5 = fillmissing(Ist_7V5,'linear'); %% Filling missing data with using statistical
      techniques
220 Ist_7V5 = filloutliers(Ist_7V5,'linear','median','ThresholdFactor',75); %% Finding and
      replacing outliers in data
221 Ist_7V5 = smoothdata(Ist_7V5,'movmedian',100); %% Smoothing noisy data
222
223 Vgs_LS_7V5_nanIndex = Vgs_LS_7V5<0;
224 Vgs_LS_7V5(Vgs_LS_7V5_nanIndex) = NaN; %% Replacing bad data with NaNs
225 Vgs_LS_7V5 = fillmissing(Vgs_LS_7V5,'linear'); %% Filling missing data with using
      statistical techniques
226 Vgs_LS_7V5= filloutliers(Vgs_LS_7V5,'linear','median','ThresholdFactor',75); %% Finding
      and replacing outliers in data
227 Vgs_LS_7V5 = smoothdata(Vgs_LS_7V5,'movmedian',500); %% Smoothing noisy data
228
229
230
231 Ist_wout_z_nanIndex = Ist_wout_z<0;
232 Ist_wout_z(Ist_wout_z_nanIndex) = NaN; %% Replacing bad data with NaNs
233 Ist_wout_z= fillmissing(Ist_wout_z,'linear'); %% Filling missing data with using
      statistical techniques
234 Ist_wout_z = filloutliers(Ist_wout_z,'linear','median','ThresholdFactor',75); %% Finding
      and replacing outliers in data
235 Ist_wout_z = smoothdata(Ist_wout_z,'movmedian',100); %% Smoothing noisy data
236
237 Vgs_LS_wout_z_nanIndex = Vgs_LS_wout_z<0;
238 Vgs_LS_wout_z(Vgs_LS_wout_z_nanIndex) = NaN; %% Replacing bad data with NaNs
239 Vgs_LS_wout_z = fillmissing(Vgs_LS_wout_z,'linear'); %% Filling missing data with using
      statistical techniques
240 Vgs_LS_wout_z= filloutliers(Vgs_LS_wout_z,'linear','median','ThresholdFactor',75); %%
      Finding and replacing outliers in data
241 Vgs_LS_wout_z = smoothdata(Vgs_LS_wout_z,'movmedian',500); %% Smoothing noisy data
242
243 %% Preprocessing experimental data to plot transfer characteristics Vds=300V
244
245
246 Ist_3V_300V_nanIndex = Ist_3V_300V<0;
247 Ist_3V_300V(Ist_3V_300V_nanIndex) = NaN; %% Replacing bad data with NaNs
```

```
Ist_3V_300V = fillmissing(Ist_3V_300V,'linear'); %% Filling missing data with using statistical techniques
Ist_3V_300V = filloutliers(Ist_3V_300V,'linear','median','ThresholdFactor',75); %% Finding and replacing outliers in data
Ist_3V_300V = smoothdata(Ist_3V_300V,'movmedian',100); %% Smoothing noisy data

Vgs_LS_3V_300V_nanIndex = Vgs_LS_3V_300V<0;
Vgs_LS_3V_300V(Vgs_LS_3V_300V_nanIndex) = NaN; %% Replacing bad data with NaNs
Vgs_LS_3V_300V = fillmissing(Vgs_LS_3V_300V,'linear'); %% Filling missing data with using statistical techniques
Vgs_LS_3V_300V= filloutliers(Vgs_LS_3V_300V,'linear','median','ThresholdFactor',75); %% Finding and replacing outliers in data
Vgs_LS_3V_300V = smoothdata(Vgs_LS_3V_300V,'movmedian',500); %% Smoothing noisy data



Ist_7V5_300V_nanIndex = Ist_7V5_300V<0;
Ist_7V5_300V(Ist_7V5_300V_nanIndex) = NaN; %% Replacing bad data with NaNs
Ist_7V5_300V = fillmissing(Ist_7V5_300V,'linear'); %% Filling missing data with using statistical techniques
Ist_7V5_300V = filloutliers(Ist_7V5_300V,'linear','median','ThresholdFactor',75); %% Finding and replacing outliers in data
Ist_7V5_300V = smoothdata(Ist_7V5_300V,'movmedian',100); %% Smoothing noisy data

Vgs_LS_7V5_300V_nanIndex = Vgs_LS_7V5_300V<0;
Vgs_LS_7V5_300V(Vgs_LS_7V5_300V_nanIndex) = NaN; %% Replacing bad data with NaNs
Vgs_LS_7V5_300V = fillmissing(Vgs_LS_7V5_300V,'linear'); %% Filling missing data with using statistical techniques
Vgs_LS_7V5_300V= filloutliers(Vgs_LS_7V5_300V,'linear','median','ThresholdFactor',75); %% Finding and replacing outliers in data
Vgs_LS_7V5_300V = smoothdata(Vgs_LS_7V5_300V,'movmedian',500); %% Smoothing noisy data



Ist_wout_z_300V_nanIndex = Ist_wout_z_300V<0;
Ist_wout_z_300V(Ist_wout_z_300V_nanIndex) = NaN; %% Replacing bad data with NaNs
Ist_wout_z_300V= fillmissing(Ist_wout_z_300V,'linear'); %% Filling missing data with using statistical techniques
Ist_wout_z_300V = filloutliers(Ist_wout_z_300V,'linear','median','ThresholdFactor',75); %% Finding and replacing outliers in data
Ist_wout_z_300V = smoothdata(Ist_wout_z_300V,'movmedian',100); %% Smoothing noisy data

Vgs_LS_wout_z_300V_nanIndex = Vgs_LS_wout_z_300V<0;
Vgs_LS_wout_z_300V(Vgs_LS_wout_z_300V_nanIndex) = NaN; %% Replacing bad data with NaNs
```

```
282 Vgs_LS_wout_z_300V = fillmissing(Vgs_LS_wout_z_300V,'linear'); %% Filling missing data
        with using statistical techniques
283 Vgs_LS_wout_z_300V= filloutliers(Vgs_LS_wout_z_300V,'linear','median','ThresholdFactor'
        ,75); %% Finding and replacing outliers in data
284 Vgs_LS_wout_z_300V = smoothdata(Vgs_LS_wout_z_300V,'movmedian',500); %% Smoothing noisy
        data
285
286 %% Plotting
287 % figure(1)
288 % yyaxis left
289 % plot((time_3V)-744-0.34,Vgs_LS_3V,...
290 %     (time_7V5)-240.894,Vgs_LS_7V5,...
291 %     (time_wout_z-744.774),Vgs_LS_wout_z,...
292 %     time_3V_300V-241.172,Vgs_LS_3V_300V,...
293 %     (time_7V5_300V)-240-0.88-0.31,Vgs_LS_7V5_300V,...
294 %     time_wout_z_300V-241.3,Vgs_LS_wout_z_300V)
295 % ylabel('Vgs(V)')
296 %
297 % yyaxis right
298 % plot((time_3V)-744-0.34,Ist_3V,...
299 %     (time_7V5)-240.894, Ist_7V5,...
300 %     (time_wout_z-744.774),Ist_wout_z,...
301 %     (time_3V_300V)-241.172,Ist_3V_300V,...
302 %     (time_7V5_300V)-240-0.88-0.31, Ist_7V5_300V,...
303 %     (time_wout_z_300V)-241.3,Ist_wout_z_300V) % Intentional delay introduced just to see
        the waveforms
304 % xlabel('Time(us)')
305 % ylabel('Ist(A)')
306 % %xlim([-100 300])
307 % %ylim([0 2])
308 % legend({'Vgs 3V zener 100V',...
309 %     'Vgs 7V5 Zener 100V',...
310 %     'Vgs Without Zener 100V',...
311 %     'Vgs 3V zener 300V',...
312 %     'Vgs 7V5 Zener 300V',...
313 %     'Vgs Without Zener 300V',...
314 %     'Ist 3V zener',...
315 %     'Ist 7V5 Zener',...
316 %     'Ist Without Zener',...
317 %     'Ist 3V zener 300V',...
318 %     'Ist 7V5 Zener 300V',...
319 %     'Ist Without Zener 300V'},...
320 %     'Location','northwest')
321 % title('Shoot-through voltage and current(Experiment)at Tc=80^{\circ}C')
```

```
% print('Vgs_Ist_Experiment','-dpdf')

figure(2)
tiledlayout(3,1)
nexttile
%%%% 3V Zener Vgst ISt 100V
yyaxis left
plot((time_3V)-744-0.34,Vgs_LS_3V)
ylabel('Vgs(V)')

yyaxis right
plot((time_3V)-744-0.34,Ist_3V)
ylabel('Ist (A)')
legend('Vgs','Ist',...
    'Location','northwest')
title('Vst and Ist with 3V Zener, Vds=100V and Tc=80^{\circ}C')

xlim([-10 25])
grid on
box on

%%%% 7.5V Zener Vgst ISt 100V
nexttile
yyaxis left
plot((time_7V5)-240.894,Vgs_LS_7V5)
ylabel('Vgs(V)')

yyaxis right
plot((time_7V5)-240.894, Ist_7V5)
ylabel('Ist (A)')

legend('Vgs','Ist',...
    'Location','northwest')
title('Vst and Ist with 7.5V Zener, Vds=100V and Tc=80^{\circ}C')
xlim([-10 25])
grid on
box on

%%%% Without Zener Vgst ISt 100V
nexttile
yyaxis left
plot((time_wout_z-744.774),Vgs_LS_wout_z)
ylabel('Vgs(V)')

```

```
yyaxis right
plot((time_wout_z-744.774),Ist_wout_z)
ylabel('Ist (A)')

legend('Vgs','Ist',...
    'Location','northwest')
title('Vst and Ist withouy Zener, Vds=100V and Tc=80^{\circ}C')
xlim([-10 25])
grid on
box on

print('Vgs_Ist_Experiment_100V','-dpdf')

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
figure(3)
tiledlayout(3,1)
nexttile
%%%% 3V Zener Vgst ISt 300V
yyaxis left
plot(time_3V_300V-241.172,Vgs_LS_3V_300V)
ylabel('Vgs(V)')

yyaxis right
plot((time_3V_300V)-241.172,Ist_3V_300V)
ylabel('Ist (A)')

legend('Vgs','Ist',...
    'Location','northwest')
title('Vst and Ist with 3V Zener, Vds=300V and Tc=80^{\circ}C')
xlim([-10 25])
grid on
box on

%%%% 7.5V Zener Vgst ISt 300V
nexttile
yyaxis left
plot((time_7V5_300V)-240-0.88-0.31,Vgs_LS_7V5_300V)
ylabel('Vgs(V)')

yyaxis right
plot((time_7V5_300V)-240-0.88-0.31, Ist_7V5_300V)
ylabel('Ist (A)')

legend('Vgs','Ist',...
```

```
    'Location','northwest')
title('Vst and Ist with 7.5V Zener, Vds=300V and Tc=80^{\circ}C')
xlim([-10 25])
grid on
box on


%%%% Without Zener Vgst ISt 300V
nexttile
yyaxis left
plot(time_wout_z_300V-241.3,Vgs_LS_wout_z_300V)
ylabel('Vgs(V)')

yyaxis right
plot((time_wout_z_300V)-241.3,Ist_wout_z_300V)
ylabel('Ist (A)')

legend('Vgs','Ist',...
    'Location','northwest')
title('Vst and Ist with without Zener, Vds=300V and Tc=80^{\circ}C')
xlim([-10 25])
grid on
box on
print('Vgs_Ist_Experiment_300V','-dpdf')

%
% figure(1)
% yyaxis left
% plot((time_3V)-744-0.34,Vgs_LS_3V,...
%     (time_7V5)-240.894,Vgs_LS_7V5,...
%     (time_wout_z-744.774),Vgs_LS_wout_z,...
%     time_3V_300V-241.172,Vgs_LS_3V_300V,...
%     (time_7V5_300V)-240-0.88-0.31,Vgs_LS_7V5_300V,...
%     time_wout_z_300V-241.3,Vgs_LS_wout_z_300V)
% ylabel('Vgs(V)')
%
% yyaxis right
% plot((time_3V)-744-0.34,Ist_3V,...
%     (time_7V5)-240.894, Ist_7V5,...
%     (time_wout_z-744.774),Ist_wout_z,...
%     (time_3V_300V)-241.172,Ist_3V_300V,...
%     (time_7V5_300V)-240-0.88-0.31, Ist_7V5_300V,...
%     (time_wout_z_300V)-241.3,Ist_wout_z_300V) % Intentional delay introduced just to see
      the waveforms
```

```
% xlabel('Time(us)')
% ylabel('Ist(A)')
% %xlim([-100 300])
% %ylim([0 2])
% legend({'Vgs 3V zener 100V',...
%     'Vgs 7V5 Zener 100V',...
%     'Vgs Without Zener 100V',...
%     'Vgs 3V zener 300V',...
%     'Vgs 7V5 Zener 300V',...
%     'Vgs Without Zener 300V',...
%     'Ist 3V zener',...
%     'Ist 7V5 Zener',...
%     'Ist Without Zener',...
%     'Ist 3V zener 300V',...
%     'Ist 7V5 Zener 300V',...
%     'Ist Without Zener 300V'},...
%     'Location','northwest')
% title('Shoot-through voltage and current(Experiment)at Tc=80^{\circ}C')
% print('Vgs_Ist_Experiment','-dpdf')


%% Plotting transfer characteristics
%
%
  for d=1:length(Ist_3V)
      if(d>1.12e5)
       Ist_3V(d)=NaN;
      end
      if(d<6e4)
       Ist_3V(d)=NaN;
      end
  end
%
   for d=1:length(Ist_7V5)
      if(d>6.6e4)
       Ist_7V5(d)=NaN;
      end
      if(d<6e4)
       Ist_7V5(d)=NaN;
      end
   end

  for d=1:length(Ist_wout_z)
      if(d>6.296e4)
```

```
497       Ist_wout_z(d)=NaN;
498       end
499       if(d<6e4)
500        Ist_wout_z(d)=NaN;
501       end
502   end
503 %
504 %
505   for d=1:length(Ist_3V_300V)
506       if(d>1.121e5)
507        Ist_3V_300V(d)=NaN;
508       end
509       if(d<6e4)
510        Ist_3V_300V(d)=NaN;
511       end
512   end
513
514
515   for d=1:length(Ist_7V5_300V)
516       if(d>1.1245e5)
517        Ist_7V5_300V(d)=NaN;
518       end
519       if(d<6e4)
520        Ist_7V5_300V(d)=NaN;
521       end
522   end
523
524
525   for d=1:length(Ist_wout_z_300V)
526       if(d>1.128e5)
527        Ist_wout_z_300V(d)=NaN;
528       end
529       if(d<6e4)
530        Ist_wout_z_300V(d)=NaN;
531       end
532   end
533
534
535 % figure(4)
536 % plot(Vgs_LS_3V,Ist_3V,'*-',...
537 %     Vgs_LS_7V5,Ist_7V5,'x-',...
538 %     Vgs_LS_wout_z,Ist_wout_z,'o-',...
539 %     Vgs_LS_3V_300V,Ist_3V_300V,'*-',...
540 %     Vgs_LS_7V5_300V,Ist_7V5_300V,'x-',...
```

```
%     Vgs_LS_wout_z_300V,Ist_wout_z_300V,'o-')
% xlabel('Vgs(V)')
% ylabel('Ist(A)')
% legend({'3V zener 100V',...
%     '7.5V Zener 100V',...
%     'Without Zener 100V',...
%     '3V zener 300V',...
%     '7.5V Zener 300V',...
%     'Without Zener 300V'},...
%     'Location','northwest') % exp - experimental, sim- simulation
% % % %xlim([0 6])
% % % %ylim([0 2])
% grid on
% title('Transfer characteristics of C2M0080120D (Vds=100V and 300V)Tc=80^{\circ}C')
%

figure(4)
tiledlayout(2,1)
nexttile
plot(Vgs_LS_3V,Ist_3V,'*-',...
    Vgs_LS_7V5,Ist_7V5,'x-',...
    Vgs_LS_wout_z,Ist_wout_z,'o-')
xlabel('Vgs(V)')
ylabel('Ist(A)')
legend({'3V zener 100V',...
    '7.5V Zener 100V',...
    'Without Zener 100V'},...
    'Location','northwest') % exp - experimental, sim- simulation
% % %xlim([0 6])
% % %ylim([0 2])
grid on
title('Transfer characteristics of C2M0080120D (Vds=100V)Tc=80^{\circ}C')

nexttile
plot(Vgs_LS_3V_300V,Ist_3V_300V,'*-',...
    Vgs_LS_7V5_300V,Ist_7V5_300V,'x-',...
    Vgs_LS_wout_z_300V,Ist_wout_z_300V,'o-')
xlabel('Vgs(V)')
ylabel('Ist(A)')
legend({'3V zener 300V',...
    '7.5V Zener 300V',...
    'Without Zener 300V'},...
    'Location','northwest') % exp - experimental, sim- simulation
% % %xlim([0 6])
```

```
585 % % %ylim([0 2])
586 grid on
587 title('Transfer characteristics of C2M0080120D (300V)Tc=80^{\circ}C')
588
589  print('transfer_characteristics_Experiment','-dpdf')
```

B.3 Matlab script for characterization of isolated DC-DC converter for gate driver

```
% Experimental characterization of Recom RP2415S DC/DC

%% Cleaning
clc
clear
close all

%% Input data
Vin = [5 10 15 20 24];
Vout = [3.29 6.52 9.76 13.10 15.83];

%% Processing
par = polyfit(Vin, Vout, 1);
x_points = linspace(0, max(Vin), 100);
y_points = polyval(par, x_points);
rmserr = std(Vout - polyval(par, Vin));

%% Results
fprintf('Recom RP2415S characterization\n')
fprintf('-----------------------------------\n')
fprintf(' Slope: % 4.3f\n', par(1))
fprintf('Origin: % 4.3f\n', par(2))
fprintf(' Error: % 4.3f\n', rmserr)
figure
hold on
plot(Vin, Vout, 'b.')
plot(x_points, y_points, 'r-')
box on
grid on
xlabel('Input voltage (V)')
ylabel('Output voltage (V)')
legend({'Data', 'Linear model'}, 'Location', 'northwest')
print('dc_dc_characterization','-dpdf')
```

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