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Development of DC Nanogrid Devices

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List of Acronyms

AC	Alternating Current
BES	Battery Energy Storage
CAGR	Compound Annual Growth Rate
DAB	Dual Active Bridge
DC	Direct Current
DERs	Distributed Energy Resources
DMA	Direct Memory Access
EU	European Union
FEM	Finite Element Method
GaN	Gallium Nitride
IMS	Insulated Metal Substrate
IR	Infrared
LPF	Low Pass Filter

LPT	Load Power Tracking
MEA	More Electric Aircraft
MPPT	Maximum Power Point Tracking
NGs	NanoGrids
PD	Power Delivery
PDO	Power Data Object
PG	Power Grid
PI	Proportional Integral
PV	Photovoltaic
PWM	Pulse Width Modulation
RES	Renewable Energy Sources
SCU	Supervision and Control Unit
SF	Soiling Factor
SiC	Silicon Carbide
SoC	State of Charge
TAB	Triple Active Bridge
WBG	Wide Band Gap
ZVS	Zero Voltage Switching

Introduction

The shift toward the increased use of Distributed Energy Resources (DERs) and the need for efficient energy use, has favored the development and deployment of smart grids. The different DERs that can be used, the sizes of the network, and the power capacities of smart grids lead to numerous research and development projects [1]. Photovoltaic (PV) sources as DERs are more and more included into the grid architecture topologies, often together with storage units and small power electronic converters [2]. Considering the most common Renewable Energy Sources (RES) and the increasing Direct Current (DC) loads, DC connection lines are progressively integrated in the grid architectures. Even when Alternating Current (AC) motors have to be powered, for example, it's customary to drive them with an inverter, starting from a defined DC bus voltage. The main objectives of the research about DC architectures are the reduction of the number of conversion stages, an increase in the efficiency (facilitated by the aforementioned objective), together with smart systems [3].

Development and deployment of electrical grids are necessary not only where access to the Power Grid (PG) is possible and economically viable. For remote communities, especially in developing countries, NanoGrids (NGs) with storage systems can improve the reliability and availability of electricity [4]. Different definitions for NGs can be found in literature, focusing on the size of the system or the functional aspects of the topology [5]. Interest in NGs research is proven by a constant increasing number of scientific publications over the last decade.

The main reasons behind NGs research can be summarized as follows:

- Increased use of DC DERs;
- Need for higher energy management efficiency and reduction of power conversion stages;
- Increased use of DC loads;
- Integration of storage units in the grid;
- Improved reliability and availability of the PG in developing countries or rural areas.

Beyond the impulse to the research given by the spreading of DERs, during the last decade, the technology evolution of semiconductors is influencing the development of power converters. Wide Band Gap (WBG) materials, such as Silicon Carbide (SiC) and Gallium Nitride (GaN), allow a boost in power electronics applications [6]. The efficiency improvement in the electric energy transformations, therefore in semiconductor devices, leads to a reduction of the main consumption in the electrical grids.

In this work, many aspects of NGs have been analyzed. The research objectives of this work can be summarized as follows:

- Simulations and early tests of a new DC NG architecture;
- Triple Active Bridge (TAB) converter development for PV, battery, and DC bus interface;
- Smart point of load converters for DC loads interface;
- Active load board development for arbitrary power profiles absorption;
- PV monitoring analysis with soiling sensor, irradiation measuring, and I-V characteristic extraction;
- Thermal analysis of GaN transistors and snubber capacitors through Finite Element Method (FEM) simulations and tests.

A new NG architecture has been proposed, with a TAB converter with GaN devices as the key element. The TAB allows a direct interface between PV, battery, and DC bus. Starting from three DC ports, the converter uses three Full-bridges and a high-frequency transformer for the power transfer between the ports. The control strategy applied to the converter is defined to have both a controlled 48 V voltage on the DC bus port and a Maximum Power Point Tracking (MPPT) on the PV port side. The TAB has been analyzed, simulated and prototypes have been designed for experimental tests.

The proposed NG includes smart point of load converters as well. A solution to the so-called smart plugs has been investigated in order to connect different loads, adjusting the voltage and current ratings. Moreover, an active load board has been developed to absorb arbitrary power profiles, useful to test converters at early stages and to extract battery characteristics through programmed discharge profiles.

In order to consider the use of PV modules in the NG, PV monitoring issues were also analyzed. An ad-hoc board with a soiling sensor, irradiation measuring, and I-V characteristic extraction has been designed. The board works whenever the power output of the PV modules reaches low values. In these cases, the TAB excludes the PV port and an I-V characteristic of the PV modules can be registered to observe if there is low irradiation, soiling or concentrated dirt on the modules, and PV cells malfunctions.

Finally, thermal analysis of the different components and prototype boards have been provided. In particular, FEM simulations and tests have been carried out on the GaN transistor used in the TAB, and snubber capacitors. Thermal maps and thermal dynamic behavior have been analyzed also on the different prototypes: the TAB, the smart plug converter, and the active load. In fact, thermal issues have an important role for the reliability of the proposed NG architecture.

Research and scientific publications have been done about power electronic devices in the field of PV applications, Battery Energy Storage (BES) technologies, power converters with WBG devices, and thermal issues analyses related to power electronic applications. For space limitations, marginal PhD activities not strictly related to NGs are not presented in this work. However, a list of publications can be

found in the appendix A.

The dissertation is organized as follows:

- Chapter 1 provides a quick overview of DERs, main NGs architecture topologies, and Wide Band Gap semiconductor devices;
- Chapter 2 shows the working principle of the TAB, the PV interfacing control strategy, simulations, and experimental results of the TAB;
- Chapter 3 explains two DC bus devices developed for the proposed NG architecture;
- Chapter 4 presents the PV modules soiling monitoring system;
- Chapter 5 covers thermal issues analysis for the proposed prototypes.
- Appendix A includes a list of publications made during the PhD years;
- Appendix B shows the circuit schematic and PCB layout of the TAB interface board for the microcontroller interconnection, current, and voltage sensing, and PWM conditioning;
- Appendix C shows the circuit schematics and PCB layouts of the smart plug and the active load prototype boards;
- Appendix D shows the circuit schematic and PCB layout of the soiling sensor board, used for the PV monitoring.

Chapter 1

State of the Art

1.1 Distributed Energy Resources

Environmental issues and the global need to increase economically sustainable access to electricity addressed and boost scientific research on DERs, such as solar PV, wind turbines, bioenergy plants, etc. Therefore, the concept of a common grid structure with a central generator and a large distribution network with different voltage levels is changing rapidly over time. In the meantime, the electricity demand is increasing worldwide. Considering the years between 2019 and 2021, with a global pandemic situation of Covid-19 that sensibly reduced the electricity demand in 2020, the total demand still increased by 4.5 %. In figure 1.1, the change in electricity demand between 2019 and 2021 is represented [7].

The increased energy demand should be addressed with an environmental and economically sustainable concept of PG. Alongside that, the change in the electrical generation sources and the increased use of DERs, should be addressed as well. Solar PV generation has increased globally in the last two years of almost 45 %. However, generation is highly intermittent in nature, and changes day after day. Just below, the use of wind turbines allowed a power generation of over 30 % more in 2021 than in 2019. The overall change in electricity generation between 2019 and 2021 is represented in figure 1.2.

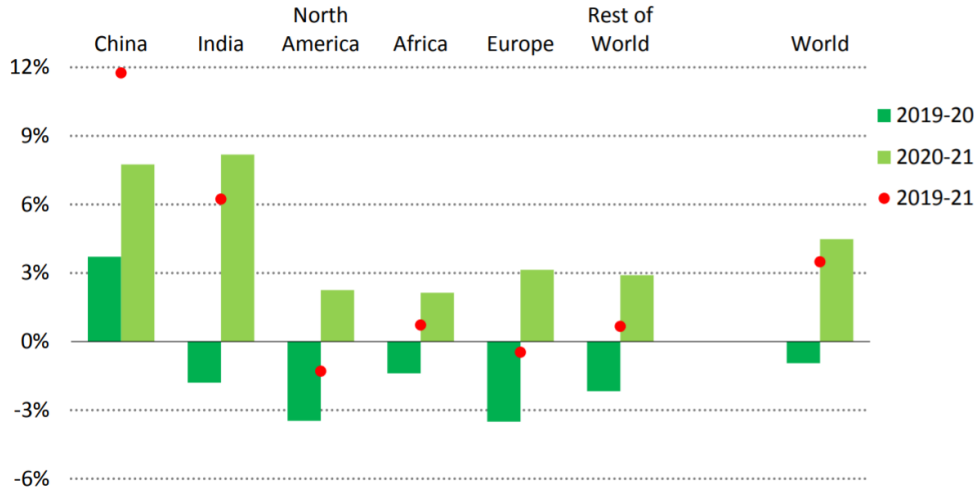


Figure 1.1: Change in electricity demand between 2019 and 2021 worldwide.

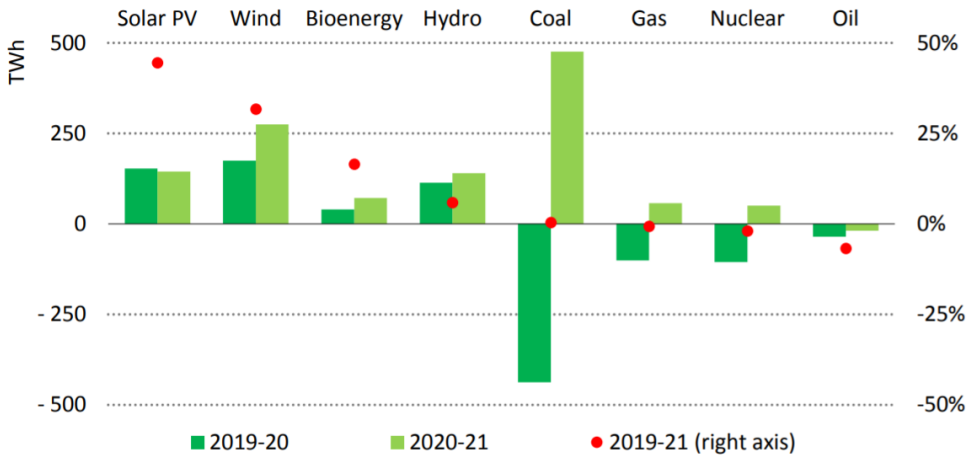


Figure 1.2: Change in electricity generation between 2019 and 2021 worldwide.

Considering the 27 countries forming European Union (EU) in 2021, the electrical generation from RES has increased from 14.2 % in 2004, to 34.2 % in 2019. In detail, considering solar PV sources in Italy, 80 % of the PV installations are for domestic applications [8]. Therefore, the DERs disadvantages should be addressed. Mainly, the intermittent nature of its power output, but also the financial capital required. In this scenario, and considering domestic applications or offices, NGs, and in particular DC NGs, have promising characteristics that can be investigated. In literature, numerous system architecture proposals can be found focusing on NGs. Different authors present as well strategic future visions of the distribution grid and the PG in general. Moreover, in the last decade, many advantages have been stated for DC NGs for the development of residential or commercial building electrical systems, compared to AC NGs [9]. In figure 1.3, a representation of the increased interest in the last decade in NGs is presented through an IEEE Xplore research.

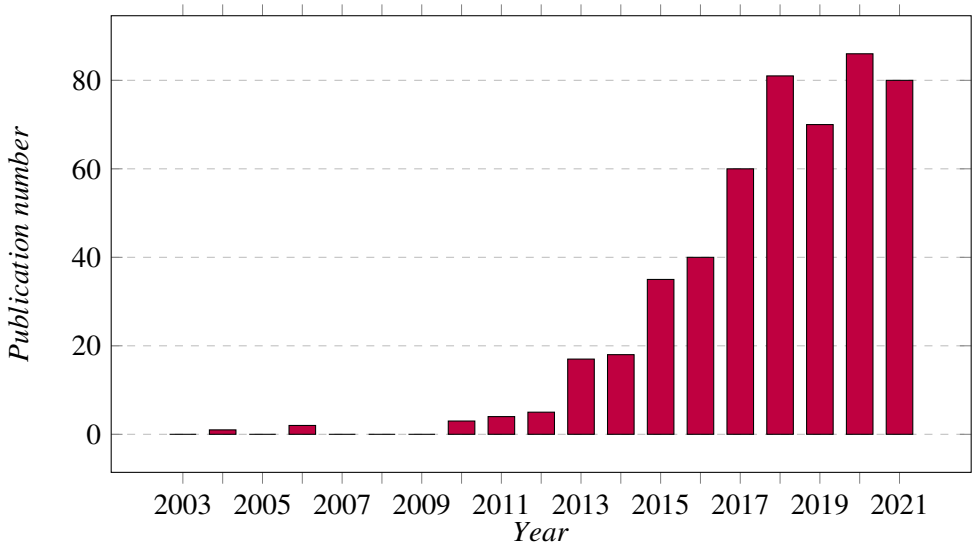


Figure 1.3: Articles on NGs related topics indexed on IEEE Xplore (updated on January 2022).

Today's electric distribution systems are designed for a one-way energy flow, introducing some challenges in integrating DERs into the network. For example, feeder

circuits are often quite long serving rural or developing areas. If small amounts of energy are injected into the grid, the system control parameters can suffer a mismatch between load and the DERs. When the local energy demand is exceeded, energy flows through the distribution feeder, as well as the local substations, increasing the potential of damages to the utility grid and impacts to other utility customers served by the same distribution circuit [10]. I.e., voltage stability, frequency stability, and overall power quality are all issues related to DERs integration [11].

Among distributed generation, solar PV records the most increasing use. However, the power yield depends on the very intermittent irradiation. Therefore, the only possible control that could be achieved by power electronic converters, in order to satisfy the power requested by the loads at the NG level, can be a reduction of power generation leaving MPPT. If a high autarky is desired, a huge overestimation of the PV plant would be necessary, beyond the necessity of storage systems. Due to these reasons, the power electronic converters are usually used to obtain the highest possible energy through MPPT algorithms, and the eventual power produced in exceeding is sent to the PG, delegating the PV integration issues to the power management entity.

Considering an AC network, if the DC voltage is transformed into AC voltage with inverters, harmonics issues are introduced. Compared to traditional energy sources, solar PV plants suffer also from inertial capability, raising large scale distribution stiffness. Storage integration or instantaneous power generator with small PV plants can help to reduce power stability issues. But also forecasting tools with prediction algorithms have to be included. Furthermore, the load supply can be controlled with smart algorithms in order to shift the electricity use when available [12].

Key factors of the integration in the PG of DERs are:

- Increase in electricity demand worldwide;
- Environmental and economical sustainability issues;
- Intermittent nature of power output;
- Voltage stability;

- Frequency stability;
- Power quality.

An important advantage of solar PV plants is the scaling flexibility, mostly dependent only on area occupation [13]. On the other hand, land degradation and habitat losses phenomena could raise. Therefore, multiple and different DERs, such as wind facilities, should be considered to allow a better sharing of land areas for agricultural uses.

1.2 Nanogrid Architectures

NGs architecture can have different requirements depending on the application and the environment. Transport vehicles, such as aircraft, ships, or electric cars, mostly need to be islanded NGs with isolation between converters [14, 15]. In these cases, a grid connection could be needed only to restore the energy consumed. A bidirectional power exchange with the grid is only recently explored in the field of vehicle to grid research, where the vehicles could improve the storage capabilities and help the grid stability. However, for some NGs applications, i.e. space satellites, it is physically impossible to supply from the grid or to change the storage devices for long periods [16]. Nevertheless, in developing countries or rural areas, the investment cost of a grid connection of a residential or commercial building can be higher than the installation of islanded NGs [17].

In figure 1.4, a country-by-country assessment about the access to electricity is shown, with a focus on developing countries [18]. In 2019, the number of people without access to electricity is about 770 million, in particular in sub-Saharan Africa, where solar PV plants can have a very high power yield.

In figure 1.5, a comparison of initial investment costs of solar PV systems, with and without storage, and PG connection in relation to the PG network distance is provided [19, 20]. Costs have been compared in 2021, considering updated average rates.

Beyond the need for electricity access, and the investment costs in the case of low

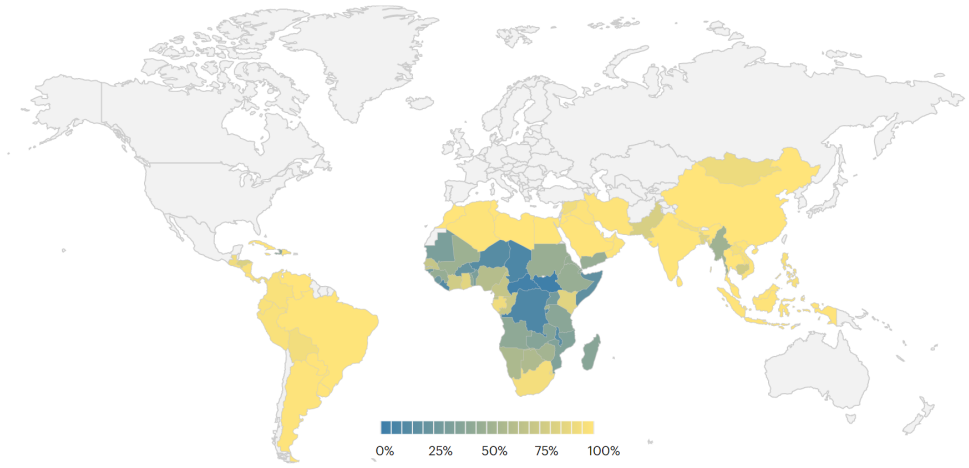


Figure 1.4: Proportion of population with access to electricity, country-by-country assessment of the International Agency of Energy (IEA), 2019. The assessment has been done with a focus on developing countries, not taking into consideration the grey colored ones.

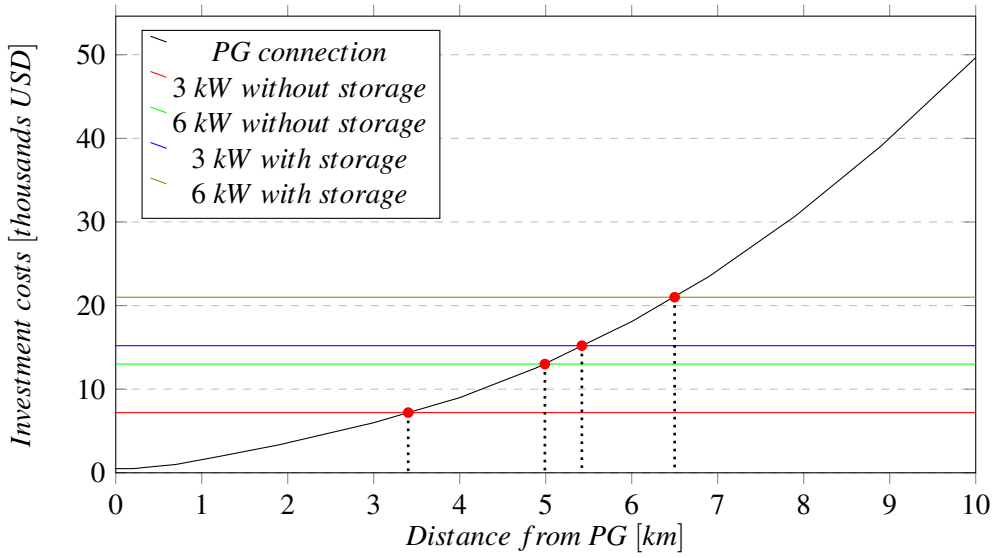


Figure 1.5: Comparison of initial investment costs of PV modules, with or without storage, and PG connection in relation to the PG distance (updated 2021).

branched and distant PG networks, low reliability and availability of the grid in many geographical regions increase as well the interest in islanded NGs deployment [21]. Therefore, research on NGs, and in particular on islanded solutions, can be considered of high interest. The main issues at the state of the art can be identified in the lack of standardization for this kind of architectures, properly designed power conversion stages, and storage units. In the literature, different proposals for the optimal sizing of the RES, mostly solar PV, and battery-based energy storage can be found [22]. MPPT of PV modules and bidirectional converters used for battery control are widely explored [23].

Whit a grid-connection possibility, the NGs can be considered as simple passive loads, or both passive/active electronic loads from the electricity provider's point of view [24]. Considering a PG connection through a rectifier or a unidirectional converter, energy from the grid is provided only when needed. Storage, in these cases, could be reduced or avoided. Thus, the system would be less flexible and issues with

grid stability rises. If a bidirectional converter is provided for the grid connection, the NGs could provide energy to the grid. When storage is included, the NGs could be used from the grid point of view in case of a greater availability of energy, therefore flattening the consumption peaks. However, the supervision complexity of the system strongly increases [25].

Islanded NGs also need to be controlled in a stable and autonomous operation mode. Load shedding strategies and storage device monitoring should be strongly recommended to solve this issue [26]. Dedicated algorithms, related to the DERs in use, have to be developed for good energy management [27]. Depending on the architecture, a dedicated communication system has to be included. For DC NGs control, the deviation of the DC bus could be used [28]. For AC NGs, V-f control schemes could be implemented for the robustness of the system [29].

Different universities, research centers, institutes, and some commercial products are already demonstrating the effectiveness and efficiencies of different NGs [30]. However, work of assessment and standardization is needed to increase commercial realization. Different components of NGs could be included in some existing architecture and low cost data loggers favor the monitoring of areas where off-grid RES are most needed [31]. Residential islanded NGs need a bottom up approach which can be considered a successful requirement for the United Nations goal of affordable and clean energy [32]. In figure 1.6, an example of AC typical NGs with a grid interface is shown.

AC NG architectures suit very well in cases where a grid connection is already available and where the main scope of the NGs is to achieve major self-sufficiency, using the utility grid only when necessary. Another advantage of this architecture, which has made it already commercial, is the lack of a necessary retrofit of the already diffused AC interconnections and load interfacing. In many cases, the two DC/DC converters for PV and battery interfacing are coupled together in the same chassis. In figure 1.7, an example of DC NG with a grid interface is shown.

In this DC NG example, the DC/AC converter should be bidirectional in order to both provide or consume energy from the PG. At the same time, if a grid connection is not available or used only to supply energy to restore the battery state of charge,

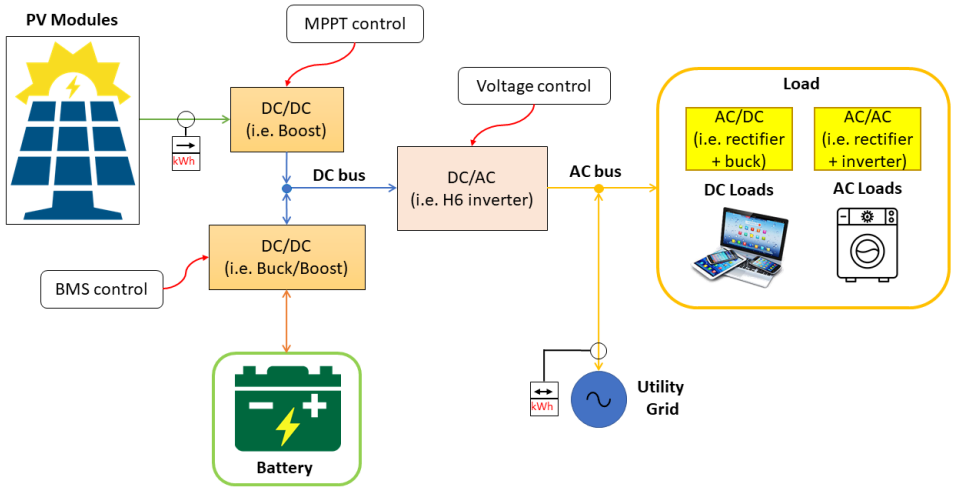


Figure 1.6: Typical AC nanogrid architecture.

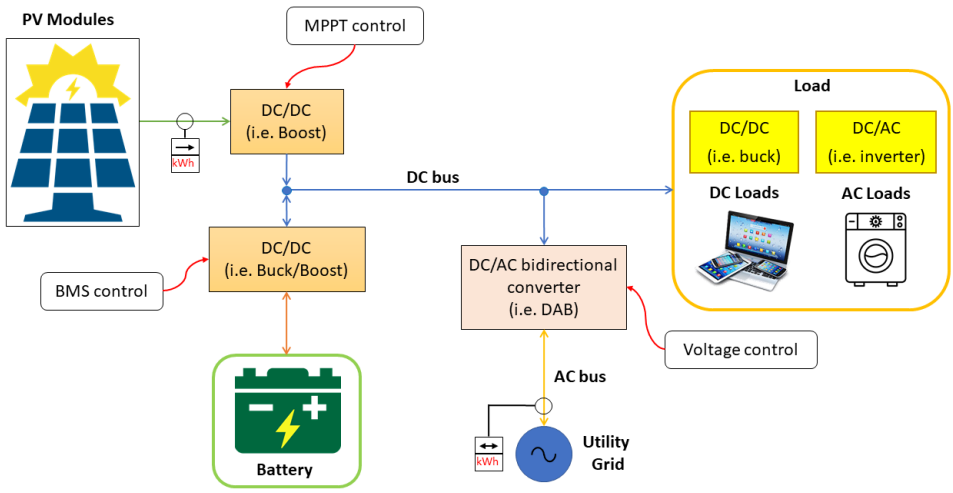


Figure 1.7: Typical DC nanogrid architecture.

a rectifier with a DC/DC converter could be used. An advantage of this architecture is the simplification of the DC/DC converter at the point of load. In fact, there is no need for rectifiers and for AC loads only an inverter could be used instead of a two stages AC/AC converter.

Typically, DC/AC converters used in power-electronics-based distributed power systems are designed to feature high efficiency and high power factor by interfacing sources and loads. This means that the whole system can be defined in terms of several subsystems. However, system integration issues should be considered, such as the instability due to subsystem interactions. When grid-tied inverters are used for renewable energy applications, the NGs interact sensibly in AC distribution systems [33]. Small-signal stability can be investigated through the General Nyquist criterion, where source and load subsystems' impedance matrices are involved [34]. Nevertheless, AC/DC converters have their issues as well. Costs, efficiency, and safety are the main characteristics studied in the literature. In particular, grounding configurations have to be addressed, for example using different transformer configurations [35].

Alternative architecture solutions can be identified with hybrid DC and AC systems. In these cases, hybrid converter topologies suits for simultaneous AC and DC outputs. The number of switches can be reduced for this scope respect to conventional architectures [36].

Considering the different architectures, multiport converters are a promising field of research. Advantages can be identified by working with a higher overview, reducing the subsystem interactions. At the state of the art, different solutions can be found in the literature. However, proposals are mostly customized for specific applications and hardly scalable [37, 38].

1.3 Wide Band Gap Semiconductors

Research in the field of power electronics converters is strongly increasing also due to the investigation of WBG semiconductors technologies. WBG semiconductor materials, where the bonding energy of atoms is greater than conventional semiconductors, introduce interesting behavior differences. A wide field of research activities can be

found on this topic. Typically, compound semiconductors devices have been introduced in power converters such as GaN and SiC. These semiconductors usually have a bandgap greater than 3 eV, compared with 1.12 eV for silicon. In table 1.1, the physical characteristics of GaN and 6H-SiC compared to Si are shown [6].

Table 1.1: Wide Band Gap semiconductors physical characteristics compared to silicon.

	E_g $[eV]$	E_c $[kV/cm]$	μ_n $[cm^2/V \cdot s]$	μ_h $[cm^2/V \cdot s]$	v_{sat} $[cm/s]$
Si	1.1	300	1500	600	1×10^7
GaN	3.4	3300	1250	850	2.2×10^7
6H-SiC	3.0	2500	500	101	2×10^7

Where E_g is the energy bandgap, E_c is the electric breakdown field, μ_n is the electron mobility, μ_h is the hole mobility, and v_{sat} is the saturated electron drift velocity.

In fact, SiC and GaN present a good trade-off between theoretical characteristics and technological processes availability. Respect to Si, WBG devices offer higher voltage blocking capabilities, higher temperature operation points, and higher switching frequencies [39]. The device breakdown voltage characteristic is increased due to the higher electrical field capability, at the same drift layer thickness. This allows different considerations: if the breakdown voltage is kept the same, the drift layer thickness could be reduced for a higher power density. Moreover, SiC and GaN could be doped more, without necessarily increasing the drift layer thickness as for Si. This allows using a higher electrical field, reducing therefore the depletion area and the on-resistance.

SiC and GaN semiconductors offer as well interesting thermal features. The wider energy gap, combined with higher melting points, allows these devices to work at higher temperatures. However, considering smaller devices to achieve faster switching frequencies, considerations about the thermal conductivity should be done. There are some sensible differences between the thermal conductivity of SiC and GaN devices. SiC devices have 4.9 $W/cm \cdot K$, while GaN devices have 1.3 $W/cm \cdot K$, respect

to 1.5 $W/cm \cdot K$ for Si devices. This means that the heat extraction for GaN devices is a critical aspect, or, for the same cooling considerations, GaN devices should work at lower power ratings.

The increased drift velocity of WBG semiconductors allows the reduction of turn-on and turn-off times. This is relevant to improve the switching characteristics, reduce the power dissipation, as well as possibly increase the working frequencies.

Summing up, WBG devices have improved performances respect to Si counterparts. Faster switching characteristics, higher blocking voltages, and lower power losses are the main reason to consider these devices very important, influencing the power electronic application field [40]. Increasing the switching frequency in power converters without recording higher power losses, for example, allows the use of smaller passive components like capacitors or inductors.

However, there are still some issues to consider. Due to higher difficulties in epitaxial growth and the fact that as mainstream the industry is moving from 6-inch towards 8-inch substrates, the costs of GaN and Sic substrates are 5 to 20 times more expensive than Si counterparts. Reliability issues as well have to be investigated more. But also from the board design point of view, there are some critical aspects to be considered. GaN devices, for example, don't offer good reverse recovery integrated diodes. This means that in the case of a H-bridge configuration, external diodes should be included. These have to work at the same switching frequency and therefore need the same board layout scrupulousness, which can introduce a barrier to the maximum switching frequency.

Nevertheless, WBG semiconductors are gaining interest in the power converters market. In particular, GaN devices for power electronic applications have been introduced in 2009, but are already very suited for low voltage applications, below 650 V. On the contrary, SiC devices are more prominent in high voltage applications, and in general, for higher power ratings. This rough division depends on the structure and manufacturing processes. GaN devices are mostly fabricated with a lateral structure growing up a thin GaN epitaxial layer on a Si wafer. This is due from the relevant GaN crystals costs, which don't make it suitable realizing entire devices with GaN crystals. Moreover, fabricating lateral GaN structures is possible in standard silicon

CMOS foundries, reducing production costs. However, the thin structure and the absence of a dedicated package limit GaN devices operating voltage. SiC devices, on the contrary, are mostly fabricated with a vertical structure, considering that the SiC crystals are of lower costs than GaN ones. This enables higher voltage and power ratings. At the same time, the size of SiC devices is still much lower than Si-based devices at the same power ratings. This makes SiC very competitive for high power density applications where still compact, not heavy or bulky converters are needed. Even in harsh environments, SiC-based devices demonstrate high reliability [41].

WBG devices have been evaluated in the last decade in many applications. Regarding NGs, improvements in efficiency and size reduction of bidirectional converters could be obtained with the use of SiC or GaN-based devices [42, 43]. In particular, for GaN power devices, the main three applications for GaN consumption are consumer electronics, NEVs, and telecom/data centers. Therefore, according to TrendForce, the GaN power market will undergo the highest magnitude of growth with revenues for 2021 reaching $83 million. Going forward, annual GaN power devices revenue is expected to grow at a 78 % Compound Annual Growth Rate (CAGR) and reach $850 million in 2025.

1.4 Proposed Nanogrid Architecture Prototype

Between the different possible NG solutions, DC NGs with multi-port bidirectional converters results to be very competitive. In particular, considering that DC NGs advantages can be identified in the reduced conversion stages and complexity. Moreover, DC NGs with PV modules are expected to grow significantly in the next decades. The integration of multi-port power converters and high-frequency isolation links could act as central nodes of the power flows, providing high efficiencies to the NG overall system.

As described in chapter 1, grid-islanded architectures are of important interest in developing countries, but also in small islands, rural and mountain areas, or transport vehicles. The main characteristics can be identified in the high cost of the utility grid connection (e.g., long cables for small loads); not reliable local power grid; inability

to connect to a local grid with fixed cables (e.g., power distribution on aircraft, or ships). In these applications, multi-port DC/DC converters, such as the TAB, could be key elements for DC NG realization. The NG architecture proposed in this work is shown in Fig 1.8.

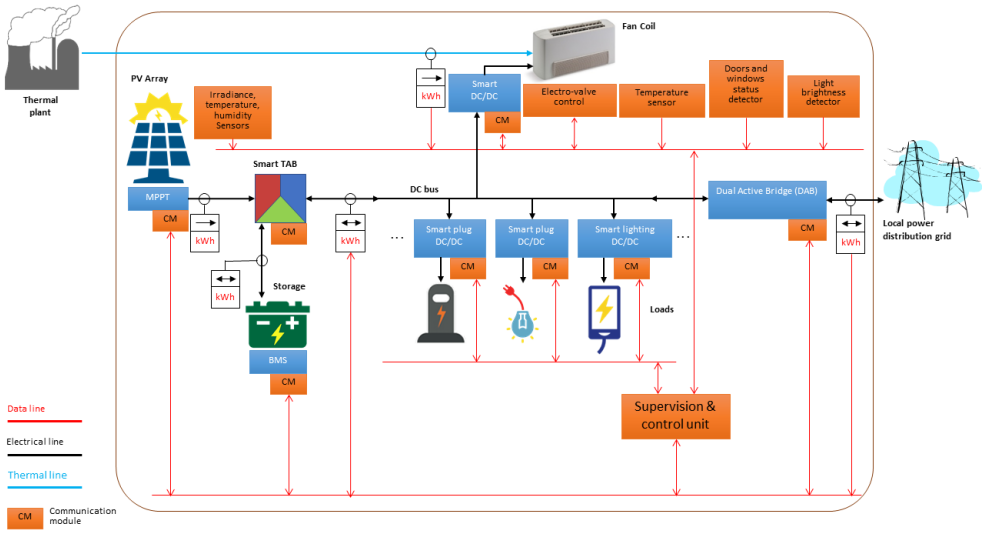


Figure 1.8: Nanogrid architecture.

The key element of the proposed architecture is the TAB. The TAB is used to interface solar PV, storage, and DC bus through a single conversion stage. Each converter communicates to a Supervision and Control Unit (SCU). The main parameters are input and output currents and voltages, but also working temperature, and failure analysis signals. Moreover, sensors are included in the system such as humidity, brightness, motion detection, etc. All this data can be used for smart control of lights, fan coil, and load shedding. In fact, the SCU, considering the storage State of Charge (SoC), the solar irradiation, and the load requests, sends an energy availability level parameter to the smart plugs. The main objective of this data is to reduce or increase power consumption. The smart plugs are DC/DC converters that can adjust dynamically the voltage output and current limitation, therefore the power profile, depending

on the load attached and the SCU supervision. The communication protocol proposed between smart plug and load is similar to the USB-C Power Delivery (PD) protocol. Finally, a possible PG connection can be achieved through a Dual Active Bridge (DAB) converter. However, the NG proposed is thought to be off-grid, which is of higher interest and easier integration (no retrofit required). Therefore, analysis and experimental are without a utility grid connection.

Chapter 2

Bidirectional Converter for PV, Storage, and Load Interfacing

2.1 Triple Active Bridge

The TAB converter topology shows interesting advantages in terms of isolation, Zero Voltage Switching (ZVS) over wide load and input voltage ranges, and high-frequency operation capability. Nevertheless, the integration of the TAB in a DC NG results in a complex and difficult to control system. In fact, the TAB power transfer functions have many degrees of freedom, and the relationship between any of two ports is always dependent on the third one.

The interest in the TAB converter topology grew up in the last years. NGs and microgrids are the main applications where it is proposed. In particular where multiple electrical systems are interconnected together [44]. In literature, different examples can be found using TAB for storage backup interface in data centers [45], More Electric Aircraft (MEA) [46], and ships grids [47]. Moreover, TAB-based NGs could gain interest in different new applications, such as MEA with solar PV modules. The reason for this interest can be found in safety purposes, such as the electrical insulation of the DC bus on conventional passenger aircraft. In [48], first simulations and experimental results of TAB converters are shown. In this case, TAB interfaces a fuel cell,

a battery, and loads. In fact, fuel cells have a slower transient response than batteries. The TAB offers the possibility to control the power flow transferred to the loads in the NG, giving different priorities to the attached sources [49].

A different scenario is defined when the TAB interfaces solar PV modules, as shown in figure 2.1. In this case, the converter should be able to achieve both a good MPPT and low-ripple bus voltage control.

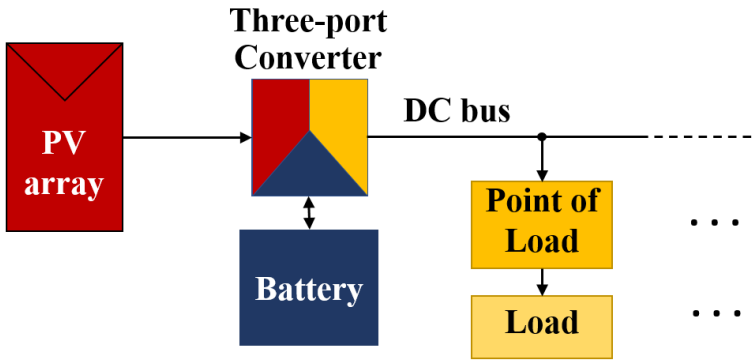


Figure 2.1: TAB interfacing PV panels, battery, and DC bus.

Similar architectures can be found in literature. In [50], the TAB converter is used to control the power flow from the PV module and from the grid to the loads. However, an MPPT algorithm is applied to a DC/DC converter that is positioned between the PV modules and the TAB, while the TAB deals the control of the fixed bus voltage for the loads. This architecture is similar to the one proposed in figure 2.1, with the addition of an MPPT converter. This reduced the control complexity. However, the overall efficiency is therefore considered as the product of both converter efficiencies. Current control strategies are proposed in different other architectures. For example, in [51], the control is based on the decoupling matrix defined in [44]. In these cases, precise, fast, and reliable current sensors are required. But also complexity in the conditioning circuits and the control algorithms is introduced. In fact, the reference current for MPPT control has to be defined. Considering the voltage non-linear dependence of the TAB power flow transfer equations and the V-I curves of the PV modules, the decoupling matrix should be adjusted in relation to the instant

voltages, changing the different control gains. Another example can be found in [52], where the TAB converter is modeled in an architecture for electric vehicle on-board charger applications. In this case, current-oriented control loops have been defined, where the voltages on the three ports are fixed.

2.1.1 Working Principle

The TAB converter is realized with three full-bridge modules coupled with a high-frequency multi-winding transformer. Three inductors are included between the full-bridges and the transformer to reduce current peaks and raise the voltage ratio between the three ports. The TAB topology is depicted in figure 2.2.

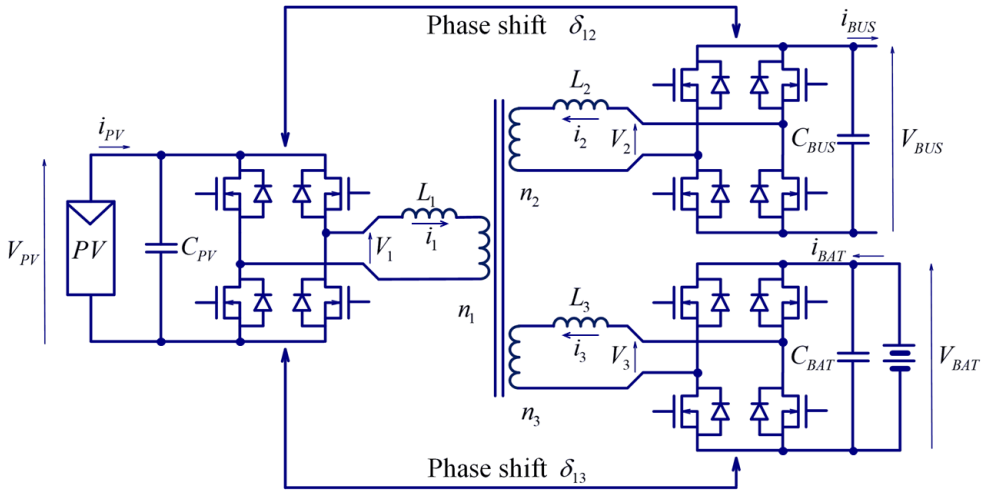


Figure 2.2: TAB converter circuit topology.

With some simplifications, from a theoretical point of view, the TAB can be represented as three inductors in a triangle connection grid. Sources of the grid are the three voltages V_1, V_2, and V_3 generated through the three full-bridges starting from V_{PV}, V_{bus}, and V_{BAT}. Figure 2.3 represents the theoretical representation of the TAB, where L_{12}, L_{23}, and L_{13} represent the primary referred leakage inductors of the trans-

former, with the integrated external inductors.

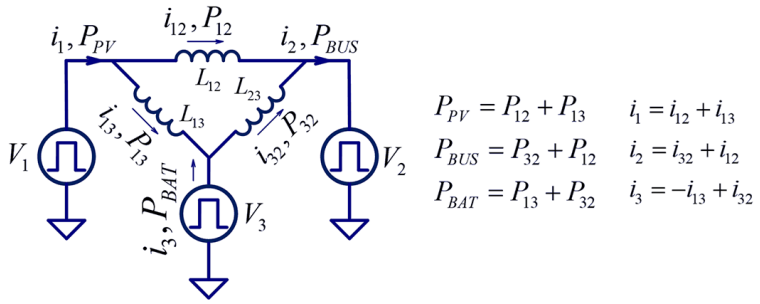


Figure 2.3: TAB converter theoretical equivalent circuit.

Electrical isolation between the three ports is provided by the high-frequency transformer. The leakage inductance and the additional series inductors adjust the current transfer. The power transfer is therefore provided by controlling the inductor charging and discharging. In fact, the three full-bridges are controlled with a 50 % duty-cycle Pulse Width Modulation (PWM) control signal, where the phase shift between the three PWM signals (and the corresponding complementary ones) is adjusted from 0 to $\pi/2$ of the PWM period. Therefore, the converter switching cycle is defined by twelve operation modes. Depending on the voltage amplitudes and phase shifts between the ports, different waveforms of the current flowing on the inductors can be observed.

In figure 2.4 and 2.5, the case with $V_1 > V_2 > V_3$ and $\delta_{12} > \delta_{13} > 0$ is shown. These parameters represent the case where $V_{PV} > V_{BAT} > V_{bus}$. Therefore, when the irradiation is high and the battery is charged. While having δ_{12} higher than δ_{13} means that power required from the load is transferred both from the PV port and from the battery port.

Each port is enabled for a bidirectional power transfer. However, in the proposed NG architecture, the first port where the PV is attached, will always have a unidirectional power exchange. This means, that when the irradiation is very low, for example during the night, the H-bridge has to be turned off. This enables to increase the efficiency of the converter and reduce the TAB topology to a DAB. For this reason,

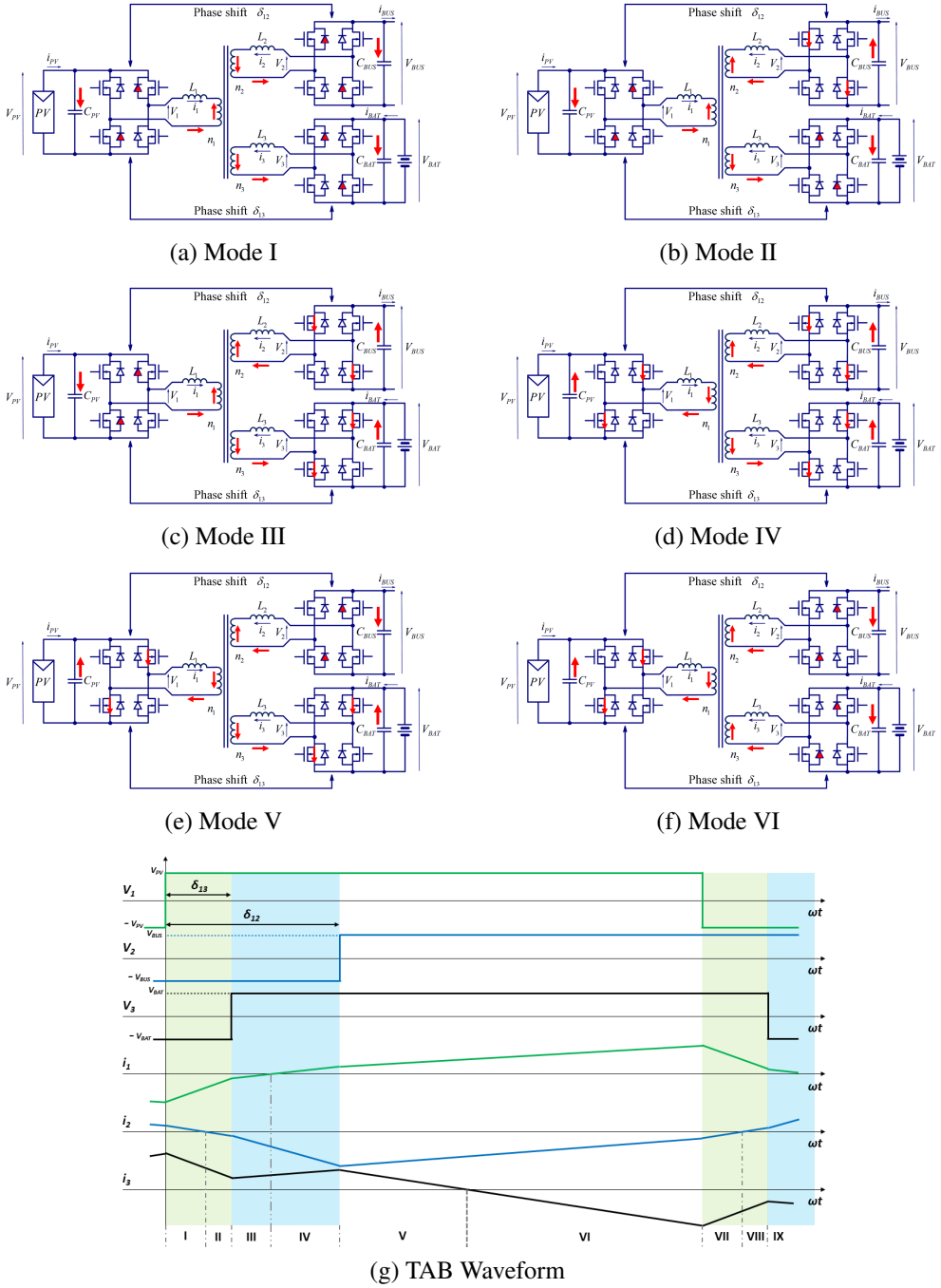
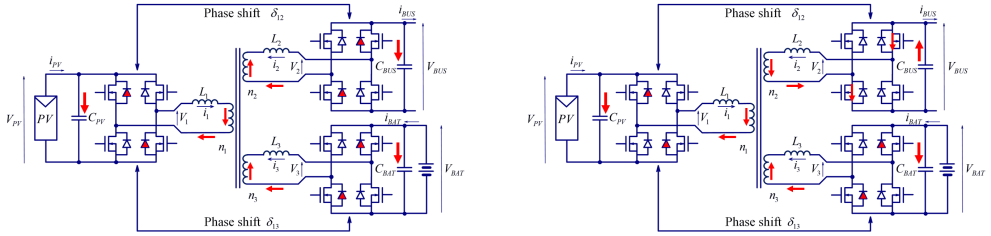
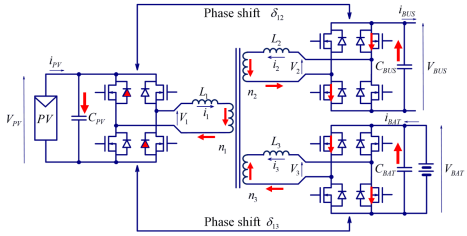


Figure 2.4: First 6 TAB functioning modes for $V_1 > V_2 > V_3$ and $\delta_{12} > \delta_{13} > 0$.

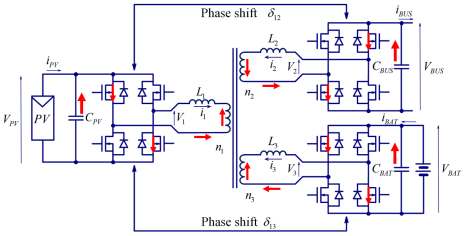


(a) Mode VII

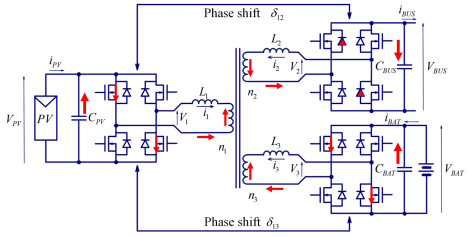
(b) Mode VIII



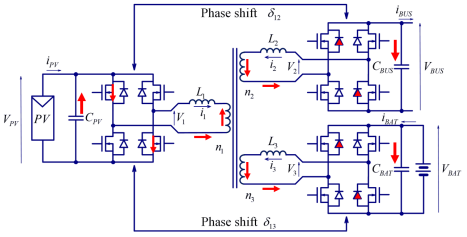
(c) Mode IX



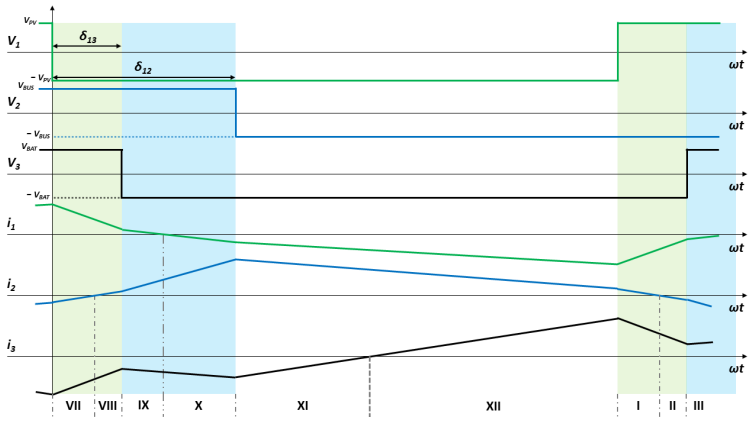
(d) Mode X



(e) Mode XI



(f) Mode XII



(g) TAB Waveform

Figure 2.5: Second 6 TAB functioning modes for $V_1 > V_2 > V_3$ and $\delta_{12} > \delta_{13} > 0$.

a monitoring board with an irradiation sensor is attached on the PV port side, and communicates with the TAB microcontroller in case of low power absorption. Considering this working condition, where the PV port is turned off, the current i_2 on the inductor L_2 can be calculated as:

$$i_2(\omega_s t) = i_2(0) + \frac{1}{L_{23}} \int_{\omega_s t} (v_2(\omega_s t) - v_3(\omega_s t))\, d(\omega_s t) \tag{2.1}$$

where ω_s is the angular switching frequency.

Assuming constant supply voltages, two operation modes can be extracted from 0 to the instantaneous value of the phase shift between the bus and the battery ports, which is: $\delta_{12} - \delta_{13} = \delta_{23}$, and from δ_{23} to π:

$$i_2(\omega_s t) = \begin{cases} \frac{V_2+V_3}{\omega_s L_{23}} \cdot \vartheta + i(0) & \text{when } 0 \leq \omega_s t \leq \delta_{23} \\ \frac{V_2-V_3}{\omega_s L_{23}} \cdot (\omega_s t - \delta_{23}) + i(\delta_{23}) & \text{when } \delta_{23} \leq \omega_s t \leq \pi \end{cases} \tag{2.2}$$

These equations are reverse signed from π to 2π. Moreover, considering this symmetry condition, $i_2(0) = -i_2(\pi)$ and the average power can be calculated considering one half cycle.

Finally, the power transfer between the battery and the bus port can be calculated as follow:

$$P_{bus} = \frac{V_2}{\pi} \left(\int_0^{\delta_{23}} i_2(\omega_s t) d(\omega_s t) + \int_{\delta_{23}}^{\pi} i_2(\omega_s t) d(\omega_s t) \right) = \frac{V_{bus} V_{BAT}}{\omega_s L_{23}} \cdot \frac{\delta_{23}(\delta_{23} - \pi)}{\pi} \tag{2.3}$$

More in general, considering the bidirectional power flow capability of each port, the equation can be written as:

$$P_{bus} = \frac{V_{bus} \cdot V_{BAT}}{\omega_s L_{23}} \cdot \delta_{23} \left(1 - \frac{|\delta_{23}|}{\pi} \right) \tag{2.4}$$

Starting from these considerations, the total power transfer flow equations can be extracted also when the PV port is enabled. Considering the power transfer to the load:

$$P_{bus} = \frac{V_{PV} \cdot V_{bus}}{\omega_s L_{12}} \cdot \delta_{12} \left(1 - \frac{|\delta_{12}|}{\pi} \right) + \frac{V_{bus} \cdot V_{BAT}}{\omega_s L_{23}} \cdot \delta_{23} \left(1 - \frac{|\delta_{23}|}{\pi} \right) \tag{2.5}$$

ZVS condition occurs when the device turn-on takes place when its anti-parallel diode is conducting. Considering the four devices on the PV port side of figure 2.4 and figure 2.5, ZVS condition is ensured only on the PV side and bus side port. Parameters that enable ZVS are:

$$\begin{aligned} &i_1(0)\ ,\ i_2(\delta_{12})\ ,\ i_3(\delta_{13}) \leq 0 \\ &i_1(\pi)\ ,\ i_2(\delta_{12}+\pi)\ ,\ i_3(\delta_{13}+\pi) \geq 0 \end{aligned} \tag{2.6}$$

However, the duty-cycle on the battery port side can be modulated to achieve ZVS condition. [53] and [54] proposes control strategy methods to adjust the duty-cycle. Therefore, the ZVS region can be extended and soft switching characteristics can be obtained over the whole period.

Finally, some considerations can be done for the TAB design. The maximum power that can be transferred, as defined in 2.5, is achieved when the phase-shift δ_{12} and δ_{23} are equal to $\pm\pi/2$. The maximum power results:

$$P_{bus}(MAX) = \frac{V_{PV} \cdot V_{bus}}{\omega_s L_{12}} \cdot \frac{\pi}{4} + \frac{V_{bus} \cdot V_{BAT}}{\omega_s L_{23}} \cdot \frac{\pi}{4} \tag{2.7}$$

Therefore, increasing the switching frequency ω_s, reduced the maximum transferable power. This is a considerable limit for a high-frequency converter. Same considerations for the inductances L_{12} and L_{23}, which should be kept low, thus increasing the current amplitudes on the transformer. Considering that reactive current always flows through the TAB, even if no power is transferred, increasing the current amplitudes means having higher power losses on the devices. Therefore, voltages on the three ports should be kept as high as possible, adjusting properly the turns ratio of the transformer.

2.2 Simulation Model

Interfacing solar PV modules to the TAB is not trivial nor deeply studied in literature. The main disadvantages can be identified in the intermittent nature of its power output, therefore the power transfer between the PV port and the other two TAB ports.

Theoretical equations consider normally a fixed voltage for the power transfer equation. In our case, the I-V curve of the PV should be taken into consideration, and the power transfer has to be adjusted in order to achieve MPPT even in case of voltage variations.

For this reason, two control loops can be defined on the two phase-shifts: the bus voltage and the MPPT control loop. Then, a third control loop can be defined to achieve ZVS [55]. Design considerations on PV modules and battery sizing can be made starting from the required output power. Conditions where irradiation is low, and therefore the TAB is reduced to a DAB, or when the SoC is low, meaning that the TAB should not extract any more power from the storage, have to be considered. A strategy that can be applied to help in these conditions is the load shedding strategy. In this case, for example, the battery storage capacity can be reduced, and an algorithm based on the battery power extraction and load priorities can reduce the storage usage of the NG.

A MATLAB/Simulink model of the TAB, the PV modules, and the battery has been defined. Simulation results have been used to define the control loop strategy, and to prove different working conditions. The reliability of the model, and the proposed control loops, has been validated through early experimental results. Irradiation, temperature, and load changes are set through fixed sequences. The three port voltages and currents are the measured parameters on which the control loops are based. The proposed control solution is a simple but effective implementation. Alternatives are the use of complex matrix decoupling systems, which are not always possible with general purpose microcontrollers. In this section, the model characteristics and the simulation results will be shown.

2.2.1 Model Characteristics

The model of the TAB considers a 1:1:1 turns ratio transformer. Optimization of the turn ratio can be done depending on the PV modules attached. In fact, battery and bus voltages work at the same levels (48 V), while increasing the PV port side voltage could increase the power transfer capability. Considering the NG architecture, having a higher power transfer capability from PV to both battery and bus is a great

advantage. This, together with an optimization of the series inductance, allows to have a greater PV module power capability and to transfer with good efficiency the power at high irradiation values and optimal temperatures [56]. However, the wide capable operating capability of the TAB and considering a first prototype test, the system is not heavily affected by the transformer turn ratio.

The model key parameters are the switching frequency and series inductance. These define the trade-off between the control simplicity, power transfer capability, current peaks, and converter costs and sizes. From equation (2.7), increasing the switching frequency or series inductance results in a reduced power transfer capability. At the same time, reducing series inductance leads to lower voltage drops between the transformer ports. This limits the input voltage range, therefore the capability to have different input voltages between the ports. As for the frequency, higher values enable to reduce the sizes and costs of the passive components.

In the proposed model, solar PV modules are used as generators only source, and the loads are modeled with a variable current generator. Table 2.1 lists the parameters of the chosen architecture model.

Applying the model parameters, the maximum load capacity can be calculated from (2.7). The maximum PV power is defined from three series connected 240 W PV modules. The MATLAB/Simulink model is shown in figure 2.6.

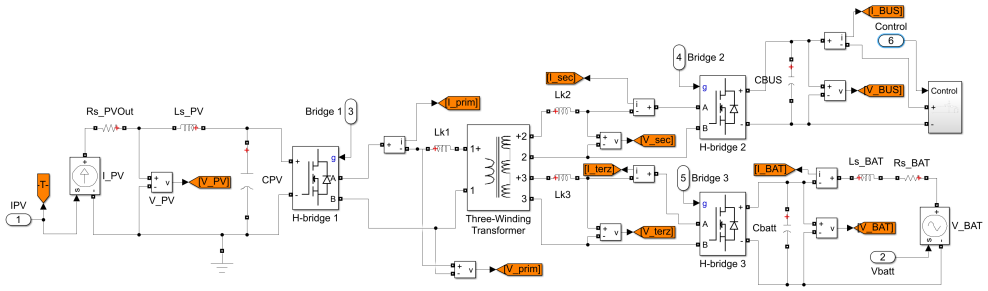


Figure 2.6: MATLAB/Simulink electrical model.

The model has been simulated with MATLAB Simulink on an OPAL Real Time

Table 2.1: Architecture model parameters.

(a) PV parameters.

Max P_{PV} [W]	V_{oc} [V]	I_{SC} [A]	C_{PV} [μF]
721	112.2	8.6	470

(b) Bus parameters.

Max P_{bus} [W]	V_{bus} [V]	C_{bus} [μF]
1570	48	470

(c) BAT parameters.

Capacity [Ah]	V_{NOM} [V]	C_{BAT} [μF]	I_{MAX} [A]
200	48	470	450

(d) Transformer parameters.

f_s [kHz]	$n_1 : n_2 : n_3$	L_m [mH]
100	1:1:1	0.2
L_1 [μH]	L_2 [μH]	L_3 [μH]
2.8	1.4	1.6

simulator. The whole system is therefore divided into two subsystems: the TAB electrical subsystem, simulated on the Xilinx Kintex 7 FPGA, and the control subsystem, simulated on the CPU.

The MATLAB/Simulink software has been chosen considering the aim of defining the best control strategy. SPICE models have been used during the board design process to evaluate single component models and the related signal quality (i.e. the PWM conditioning, voltage, and current sensing), as well as the resistor and capacitor optimal sizing definition. PLECS software has not been used considering the necessary integration of the model into the OPAL RT simulator platform.

Parasitic elements have been added to observe their contribution and second order effects. In particular: 10 $m\Omega$ equivalent series resistances and 1 nH equivalent series inductances. The parameters of the simulation are shown in table 2.2. The time step of 25 ns has been chosen for a tolerable resolution in the power transfer control. In the worse case, a resolution of 0.01 p.u. normalized over the power transfer between two ports is obtained.

Table 2.2: Simulation parameters.

T_s Simulation [ns]	T_c Control [μs]	T_{MPPT} Control MPPT [ms]
25	100	1
K_{FF} Feed Forward δ_{12}	K_{pA}	δ_{13} Step
2.6×10^{-3}	6×10^{-3}	1×10^{-4}
K_I Feed Forward δ_{13}	K_{iA}	
-2.3×10^{-3}	10	

Where T_s is the simulation time step, T_s is the time sample for the bus voltage control loop, T_{MPPT} is the time sample for the MPPT control loop. K_{FF} and K_I are the feed forward constants used to adjust δ_{12} and δ_{13} respectively, in relation to the current I_{bus}. These constants will be explained in the control loop subsections. K_{pA} and K_{iA} are respectively the proportional and integral constants for the bus voltage control loop. δ_{13} Step is the constant step applied to δ_{13} for the MPPT control loop.

The current controlled source representing the PV model is based on an analyt-

ical mathematical expression. The PV behavior is defined in MATLAB Simulink as follows [57]:

$$I_{PV} = G(I_{sc} + K_{Ti}(T - T_{ref})) - I_s(e^{\frac{q(V_{PV}+I_{PV}R_s)}{kAnT}} - 1), \tag{2.8}$$

where

$$I_s = \frac{I_{SC}}{e^{\frac{q(V_{OC}+K_{TV}(T-T_{ref}))}{kAnT}} - 1} \cdot \left(\frac{T}{T_{ref}}\right)^3 \cdot e^{\frac{qV_{OC}}{kn}(\frac{1}{T_{ref}} - \frac{1}{T})}, \tag{2.9}$$

G is the solar irradiance per 1000 W/m^2, I_{sc} is the short circuit current, K_{Ti} is the current constant correlation to temperature, T is the temperature, T_{ref} is the reference temperature: 25 °C, q is the electron charge, R_s is the PV series resistance, k is the Boltzmann's constant, n is the Diode ideality Factor, V_{ov} is the open circuit voltage, K_{Tv} is the voltage constant correlation to temperature.

The same principle is applied to the battery model. A voltage source is controlled with the following analytical expression [58]:

$$V_{BAT} = E_0 - K \cdot \frac{Q}{Q - it} + A \cdot e^{-B \cdot it}, \tag{2.10}$$

where

$$it = Q + \int I_{BAT}, \tag{2.11}$$

and E_0 is a constant voltage, K is the polarization constant, Q is the maximum battery capacity, A is the exponential voltage, B is the exponential capacity.

Finally, the CPU of the OPAL Real Time Simulator has been used for the PWM signal generation and the control algorithms. For the three full-bridges control, asymmetric PWMs are needed with controlled phase-shifts. Therefore, a saw-tooth reference wave defines the switching frequency, and four variable signals are defined for the duty-cycle and the phase shift definition. The variable signals define the on-wall and the off-wall of the PWMs. Dead time can be adjusted as well by reducing the duty-cycle, due to the center alignment of the wall signals. The algorithm flow chart is shown in figure 2.7. On-wall1 and off-wall1 define the turn-on and turn-off on one PWM signal, while on-wall2 and off-wall2 define the turn-on and turn-off of the complementary PWM signal. Each PWM, and its complementary one, can be generated with a different offset and duty-cycle.

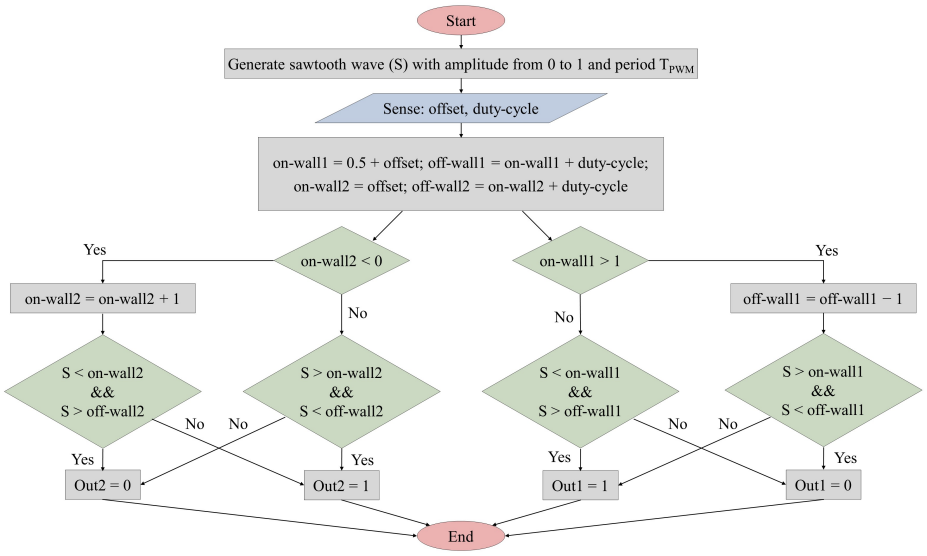


Figure 2.7: Asymmetric PWM generator algorithm flow chart.

An example with an offset of 20 % and a duty-cycle of 40 % is shown in figure 2.8. The PWM algorithm is applied for the four switches and replied for the three full-bridges in order to control the twelve GaN transistor devices.

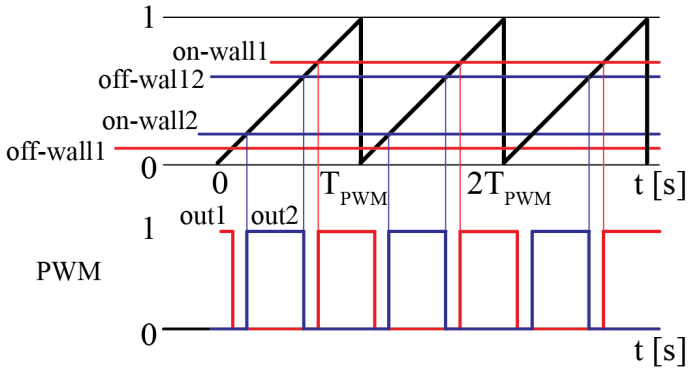


Figure 2.8: Asymmetric PWM generation example.

2.2.2 Bus Voltage Control Loop

One of the aims of the TAB is to provide power to the loads, by keeping a constant bus voltage. The non-linear, mutual dependent functions of the power transfer over phase-shift, shown in eq. (2.5), are extracted assuming constant voltages on the three ports. Therefore, it is important that on the bus port side there is a constant voltage. For this reason, a fast V_{bus} control loop is needed to avoid voltage variations in case of load changes. Otherwise, in case of a fast voltage reduction, power transfer is heavily reduced and the right power distribution between the ports has to be restored with higher phase-shift changes, risking control saturation and system instability.

The proposed bus control loop architecture is shown in figure 2.9. A feedback on the V_{bus} is used to generate the voltage error signal, and a Proportional Integral (PI) block generates the adjusted δ_{12} signal. At the same time, a feed forward on the load current I_{bus} is provided in order to reduce V_{bus} voltage variations in case of fast load changes. The transfer function G shown in the figure is a linearization of the more complex transfer function between output voltage V_{bus} and phase-shift δ_{12} (between the solar PV port and the bus port). This transfer function has been extracted with MATLAB SISOtool.

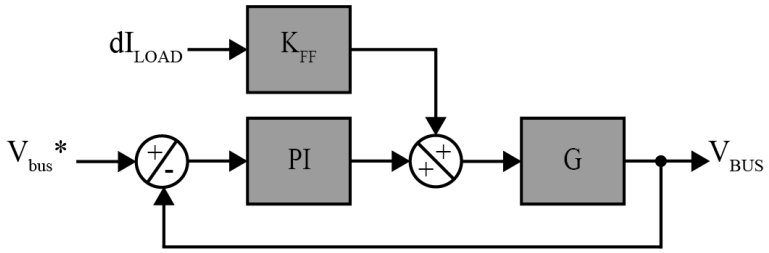


Figure 2.9: V_{bus} control loop architecture.

To extract the transfer function, the system is simplified with an R_{LOAD} resistor as load, and in parallel the C_{bus} capacitor as shown in figure 2.10.

Starting from the steady state equation (2.5), the transfer function equation of the

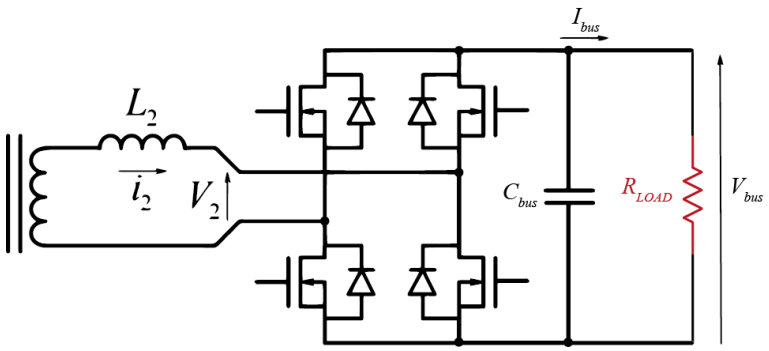


Figure 2.10: Bus port side representation for the control loop definition.

V_{bus} output voltage can be expressed as follows [59]:

$$\begin{aligned} V_{bus} = R_{LOAD} \cdot \Bigg\{ & \left[\frac{V_{PV}}{2 f_S L_{12}} (1 - |2\delta_{12}|) \right. \\ & \left. + \frac{V_{BAT}}{2 f_S L_{23}} (1 - |2\delta_{12} - 2\delta_{13}|) \right] \times \frac{\delta_{12}}{\tau s + 1} \\ & + \left[\frac{V_{BAT}}{2 f_S L_{23}} (|2\delta_{12} - 2\delta_{13}| - 1) \right] \times \frac{\delta_{13}}{\tau s + 1} \\ & + \left[\frac{1}{2 f_S L_{12}} \delta_{12} (1 - |\delta_{12}|) \right] \times \frac{V_{PV}}{\tau s + 1} \\ & + \left[\frac{1}{2 f_S L_{23}} (\delta_{12} - \delta_{13})(1 - |\delta_{12} - \delta_{13}|) \right] \times \frac{V_{BAT}}{\tau s + 1} \Bigg\}. \end{aligned} \tag{2.12}$$

The dominant pole τ can be extracted considering the output capacitor:

$$\tau = R_{LOAD} \cdot C_{bus} = 4.23 \times 10^{-3} s. \tag{2.13}$$

Considering that the bus voltage control loop has 10 times smaller time sample than the one for the MPPT control loop, some terms of equation (2.12) can be considered as constants. Therefore, the relation of V_{bus} over δ_{12} can be defined around

notable points as:

$$\begin{aligned}\frac{\partial V_{bus}}{\partial \delta_{12}} = R_{LOAD}\cdot\Big[&\frac{V_{PV}}{2f_S L_{12}} - 4\delta_{12}\frac{V_{PV}}{2f_S L_{12}} \\ &+ \frac{V_{BAT}}{2f_S L_{23}} - 4\delta_{12}\frac{V_{BAT}}{2f_S L_{23}} + 2\delta_{13}\frac{V_{BAT}}{2f_S L_{23}} \\ &+ \frac{V_{PV}}{2f_S L_{12}} - 2\delta_{12}\frac{V_{PV}}{2f_S L_{12}} + \frac{V_{BAT}}{2f_S L_{23}} \\ &- 2\delta_{12}\frac{V_{BAT}}{2f_S L_{23}} + 2\delta_{13}\frac{V_{BAT}}{2f_S L_{23}}\Big] \times \frac{1}{\tau s + 1},\end{aligned} \tag{2.14}$$

$$\frac{\partial V_{bus}}{\partial \delta_{12}}\Big|_{\delta'_{12}=0,\delta'_{13}=0,V_{PV}=0} = \frac{1136.84}{4.23\times 10^{-3}s+1}, \tag{2.15}$$

$$\frac{\partial V_{bus}}{\partial \delta_{12}}\Big|_{\delta'_{12}=0.25,\delta'_{13}=0,V_{PV}=0} = \frac{284.21}{4.23\times 10^{-3}s+1}, \tag{2.16}$$

$$\frac{\partial V_{bus}}{\partial \delta_{12}}\Big|_{\delta'_{12}=0.25,\delta'_{13}=0.1,V_{PV}=V_{PV_{MPP}}} = \frac{816.09}{4.23\times 10^{-3}s+1}. \tag{2.17}$$

From these equations, it is clear that the impacts on V_{bus} of the phase-shift changes are strongly dependent on the δ_{12} and δ_{13} values in the previous instant.

To supplement the analytical calculation, MATLAB SISOtool has been used to determine the transfer function of V_{bus} over δ_{12} directly from the electrical model. A step signal has been applied on δ_{12} keeping the V_{bus} voltage as output. The simulation is done with $\delta_{13} = 0$, and a 93.4% fit is found on the estimated transfer function in the open loop:

$$\frac{V_{bus}}{\delta_{12}} = \frac{921.78}{4.12\times 10^{-3}s+1}. \tag{2.18}$$

The PI block can be defined and simulated based on the transfer function of V_{bus} over δ_{12}. Proportional and integral constants are defined in order to keep the V_{bus} constant, with good rejection of step disturbance derived from load changes. To support the response rapidity of the system, also the current feed forward plays a very important role. The integral constant has been set at a value of 10 and the proportional

constant 6×10^{-3}. The estimated response to the step command is shown in figure 2.11, obtained by the MATLAB SISOtool simulation.

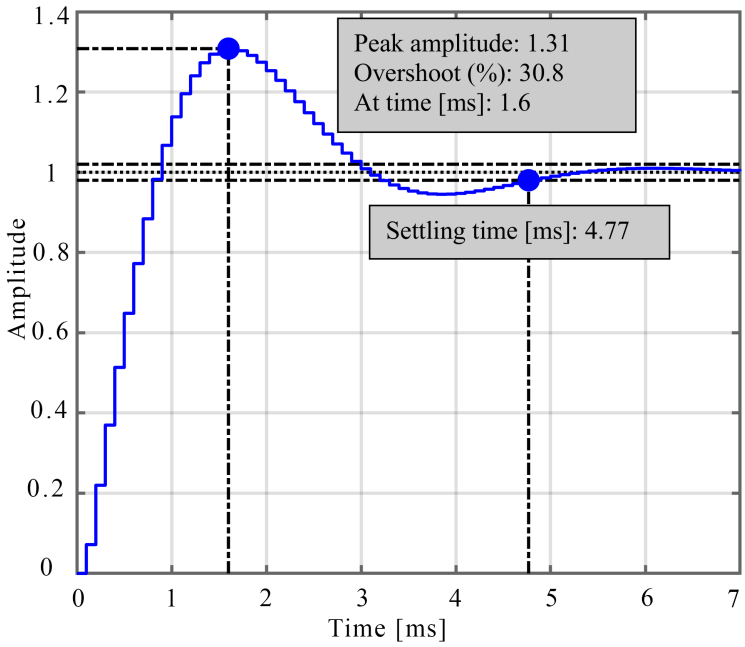


Figure 2.11: Estimated voltage control step response with SISOtool. On the ordinate axis, the amplitude is normalized over the reference voltage of the step command.

Figure 2.12, shows the simulation results with a step in the bus voltage reference from 0 to 48 V. For this simulation, a load of 9 Ω has been used. For good PI constants definition, the current feed forward control is disabled during these simulations.

Based on the V_{bus} over δ_{12} transfer function (2.18), the estimated rejection response can be extracted with MATLAB SISOtool. Figure 2.13, shows the normalized rejection response.

With the same criteria of the bus voltage reference response, a simulation with a change of the load from 36 to 9 Ω has been done. Simulation results are shown in figure 2.14. As in the previous case, the current feed forward is not introduced and δ_{13} is kept to 0.

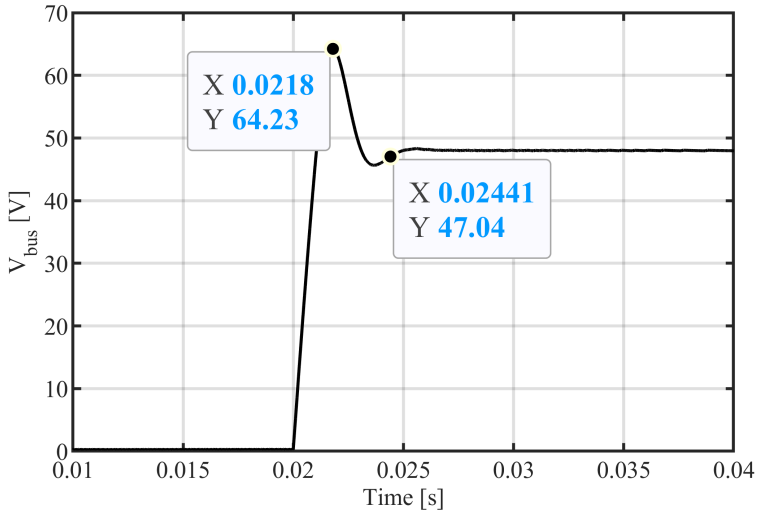


Figure 2.12: Simulation with a bus voltage reference step from 0 to 48 V.

2.2.3 MPPT Control Loop

For the direct interfacing of solar PV modules to the TAB, an MPPT control loop definition is needed. In the cases where the power that is obtained by the PV modules can be entirely transferred to the load or the storage, the TAB should work with the MPPT algorithm. When the extracted power from the PV port goes below a minimum defined value, the full-bridge attached to the PV modules has to be turned-off, obtaining a DAB between battery and load. In case the battery is fully charged, MPPT is abandoned and the full-bridge attached to the storage has to be turned-off, obtaining a DAB between PV and load. In all cases, the bus voltage control loop remains active.

The MPPT control loop has been defined with an incremental conductance algorithm, with an additional feed forward based on the I_{bus} current. The algorithm adjust δ_{13} every 1 ms. This sample time is defined to be 10 times slower than the V_{bus} control loop sample time. Therefore, the V_{bus} control, i.e. the power transferred to the load, is not heavily affected by the MPPT control loop. Still, controlling MPPT with a 1 ms step can be considered enough to follow the MPP, due to the solar PV power slow dynamic changes. δ_{13} is increased or decreased by a 1×10^{-4} incremental constant

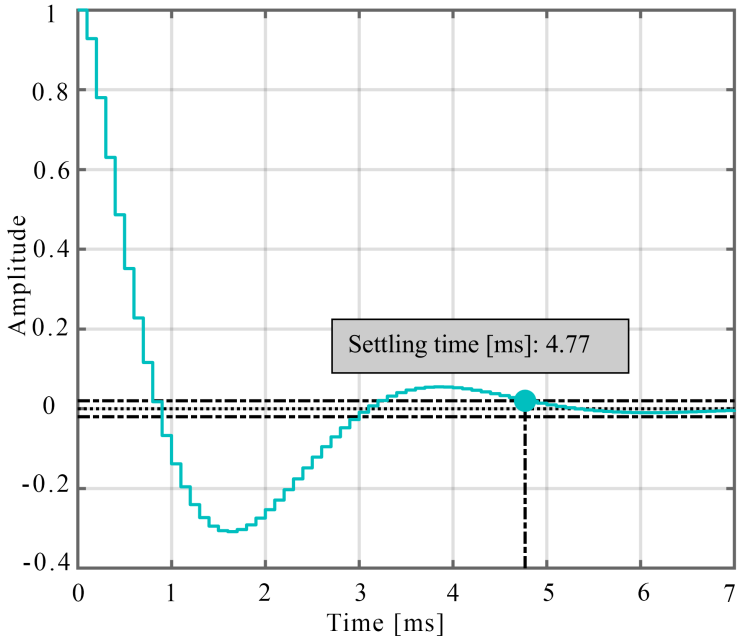


Figure 2.13: Estimated voltage step rejection response with SISOtool. On the ordinate axis, the output voltage variations to be rejected are normalized.

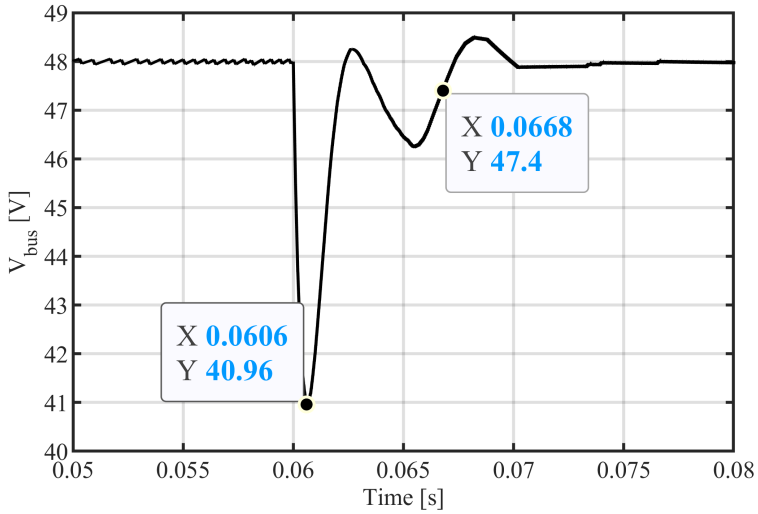


Figure 2.14: Simulation results with a load change from 36 to 9 Ω.

every control cycle. Considering a steady load condition, if a step change in solar irradiance occurs from 0 to 1000 $W\,/\,m^2$, the MPP is reached within about 1 s.

The incremental conductance algorithm has been chosen for a small perturbation of δ_{13} when MPP conditions are reached. Considering the finite resolution of δ_{13}, a small error is obtained around V_{MPP} at each irradiation or temperature condition. A good resolution step can be defined with a 40 MHz timer frequency microcontroller. In this case, in order to achieve 100 kHz PWM frequency, 400 steps have to be counted. The power transfer is defined by the phase-shift over half of the PWM period. Therefore, the resolution obtained over δ_{13} is around $1\,/\,200$. At the same time, the power transfer control resolution is divided in a non-linear way between 0 and the maximum transferable value. This can be seen from the power transfer equation from the PV modules and the other two ports (load and storage):

$$P_{PV} = \frac{V_{PV} \cdot V_{bus}}{\omega_s L_{12}} \cdot \delta_{12} \left(1 - \frac{|\delta_{12}|}{\pi}\right) + \frac{V_{PV} \cdot V_{BAT}}{\omega_s L_{13}} \cdot \delta_{13} \left(1 - \frac{|\delta_{13}|}{\pi}\right) \tag{2.19}$$

The worst error in the power extraction that can occur from the MPPT algorithm,

would be when the MPP corresponds to low phase-shift values. In fact, in this region, the power transfer to the phase-shift relation slope is higher.

The error that can occur on the MPPT can be observed in figure 2.15, where the voltage over current relation of the PV modules is shown. Here, the error is highlighted around the MPPs with three irradiation conditions, at fixed temperature.

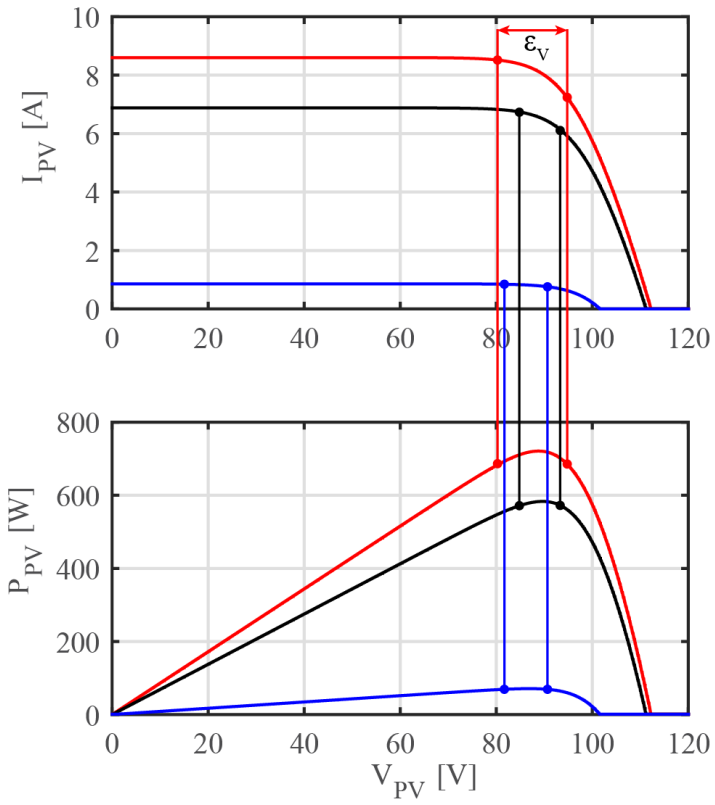


Figure 2.15: Error estimation on the PV modules I-V curve and P-V curve at different irradiation values, @Tref.

To evaluate the maximum possible error $\mathscr{E}_V$, a simulation has been done with solar irradiation of 1000 W/m^2 and zero power transfer to the load. In this case, δ_{13}

is the phase-shift normalized over π, therefore a dimensionless value, and a change from 0 to 0.005 (resolution of $1 \,/\, 200$) shows the maximum possible error $\mathscr{E}_V$ of 8 V. Considering V_{oc} equal to 112.2, the maximum error is about 7.13 %. Figure 2.16 shows the simulation results of the solar PV power transfer in relation to δ_{13}.

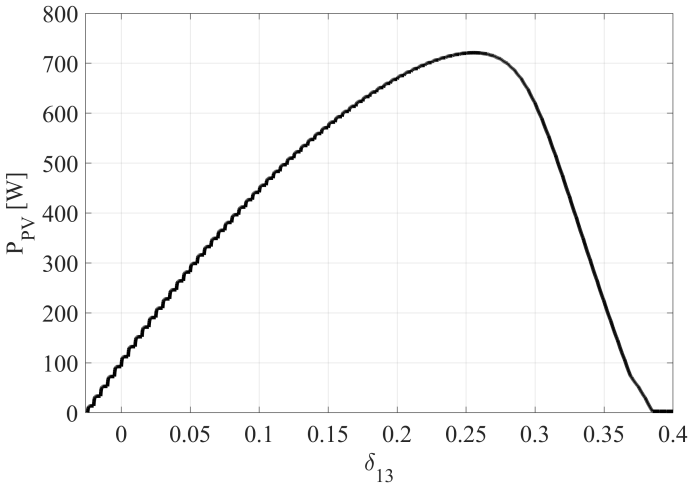


Figure 2.16: Simulation results of the PV module power transfer in relation to the phase-shift between the PV port and the battery port (δ_{13}).

Considering figure 2.16, it can be shown that the maximum transferable power isn't obtained with δ_{13} equal to $\pi/2$. This is due to the solar PV power characteristic and voltage dependence. In fact, increasing δ_{13} over the MPP corresponding values, increases the PV current despise the PV voltage, and therefore the PV power. Decreasing the PV voltage not only means going on the second half of the PV power characteristic but also decreasing the power transfer due to the TAB relations ((2.19)).

For this reason, the current feed forward has to be used to maintain the TAB working in MPPT conditions in case of fast load variations. Looking at the bus voltage control loop, in case of load current increasing, δ_{12} should increase to maintain the V_{bus}. Looking at the MPPT control loop, and in particular to equation (2.19) and figure 2.16, increasing δ_{12} means going downhill the PV power characteristic, requir-

ing more I_{PV} current. Therefore, δ_{13} should decrease instantaneously, not with the MPPT algorithm sample time, by using a current feed forward constant. Considering the case of PV power availability (shining sun), it's possible to calculate dP_{PV}, where the other variables are the phase-shifts, considering that the aim is to have $dP_{PV} = 0$. Starting from (2.19), the equation (2.20) can be defined:

$$\begin{aligned} P_{PV} &= K_1\delta_{12}(1-|\delta_{12}|)+K_2\delta_{13}(1-|\delta_{13}|) \\ &= K_1\delta_{12}^{'}(1-|\delta_{12}^{'}|)+K_2\delta_{13}^{'}(1-|\delta_{13}^{'}|) = P_{PV}^{'}. \end{aligned} \tag{2.20}$$

Observing the relationship between the derivative of the solar PV power and the derivatives of two phase shifts, the feed forward control constants can be adequately defined. The multiplicative factor between the two phase-shifts is defined by setting $dP_{PV} = 0$. While the absolute values can be extracted considering the P_{bus} derivative equations:

$$\begin{aligned} P_{bus} &= K_1\delta_{12}(1-|\delta_{12}|) \\ &\quad + K_3(\delta_{12}-\delta_{13})(1-|\delta_{12}-\delta_{13}|), \end{aligned} \tag{2.21}$$

$$\begin{aligned} \frac{\partial P_{bus}}{\partial \delta_{12}} &= K_1(1-|\delta_{12}|) - K_1\frac{\delta_{12}^2}{|\delta_{12}|} \\ &\quad - K_3\frac{(\delta_{12}-\delta_{13})^2}{|\delta_{12}-\delta_{13}|} - K_3|\delta_{12}-\delta_{13}| + K_3, \end{aligned} \tag{2.22}$$

$$\frac{\partial P_{bus}}{\partial \delta_{13}} = K_3\frac{(\delta_{12}-\delta_{13})^2}{|\delta_{12}-\delta_{13}|} + K_3|\delta_{12}-\delta_{13}| - K_3, \tag{2.23}$$

$$\begin{aligned} \frac{\partial P_{bus}}{\partial \delta_{12}} &= \frac{\partial V_{bus}}{\partial \delta_{12}} \times I_{bus} + \frac{\partial I_{bus}}{\partial \delta_{12}} \times V_{bus} \\ &= 0 + \frac{\partial I_{bus}}{\partial \delta_{12}} \times V_{bus}, \end{aligned} \tag{2.24}$$

where

$$K_1 = \frac{V_{PV}V_{bus}}{2f_sL_{12}}, \tag{2.25}$$

$$K_2 = \frac{V_{PV} V_{BAT}}{2 f_s L_{13}}, \tag{2.26}$$

$$K_3 = \frac{V_{BAT} V_{bus}}{2 f_s L_{23}}. \tag{2.27}$$

The influence of the load current I_{bus} on the solar PV power output P_{PV} in relation to the phase-shifts is shown in the analytical extracted equations (2.23) and (2.24). This can be verified through the MATLAB/Simulink model, which has been used as well to determine the feed forward parameters. Simulations with constant irradiation ($800\ W/m^2$) and a slow I_{bus} ramp change have been used to determine the phase-shift behavior with both the bus voltage and MPPT control loop activated. Figure 2.17, shows the power P_{bus} in relation to the phase-shift δ_{12}, considering that δ_{12} is varied due to the PI block in order to maintain the V_{bus} voltage constant.

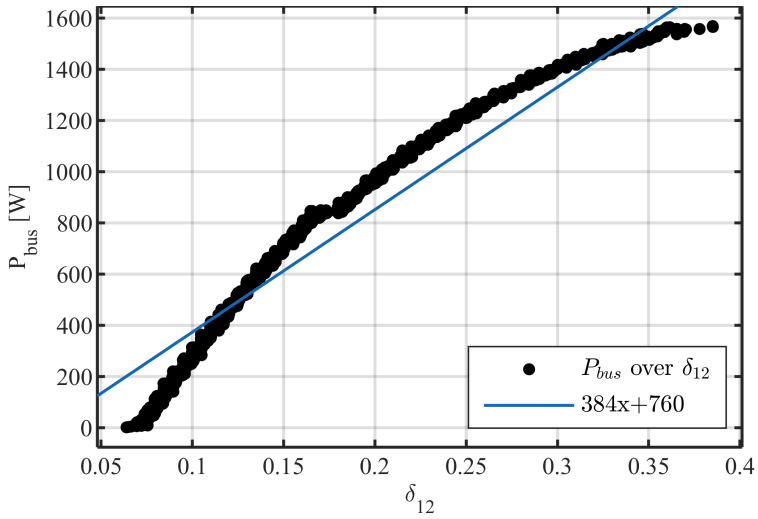


Figure 2.17: P_{bus} over δ_{12} simulation results with an I_{bus} ramp change. Bus voltage and MPPT control loops are calculated with the parameters shown in 2.2.

Figure 2.18, shows the power P_{bus} in relation to the phase-shift δ_{13}, considering that δ_{13} is varied due to the MPPT algorithm.

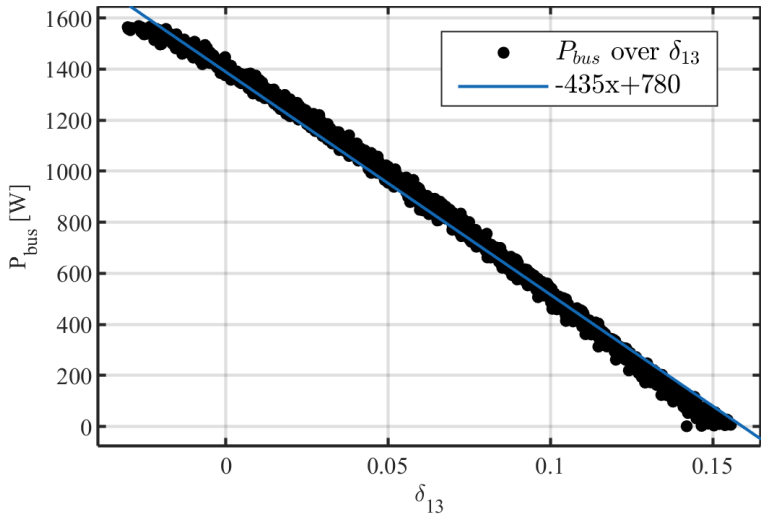


Figure 2.18: P_{bus} over δ_{13} simulation results with an I_{bus} ramp change. Bus voltage and MPPT control loops are calculated with the parameters shown in 2.2.

Both simulations are done applying a slow and constant current I_{bus} ramp from 0 to 32 A. At the same time, the MPPT algorithm and bus voltage control are applied without any feed forward. Modifying the irradiation value, for example at 1000 W/m^2, changes slightly the relation sloop and the feed forward constants can be considered effective. However, at very low irradiation values, such as 200 W/m^2, a feed forward on the δ_{13} phase-shift should be avoided. In fact, with low irradiation values, δ_{13} is reduced to maintain the PV voltage V_{PV} around V_{MPP} values. In this working region, as shown in figure 2.16, small changes in the phase-shift δ_{13} means high power transfer variations. On the other side, the MPPT algorithm can reach easily the desired δ_{13} phase-shift value.

Considering the P_{bus} over phase-shift transfer functions fitting, the feed forward constants have been defined as K_{FF} for δ_{12} and K_I for δ_{13}. The MPPT algorithm with the feed forward integration is represented in the flow chart of figure 2.19.

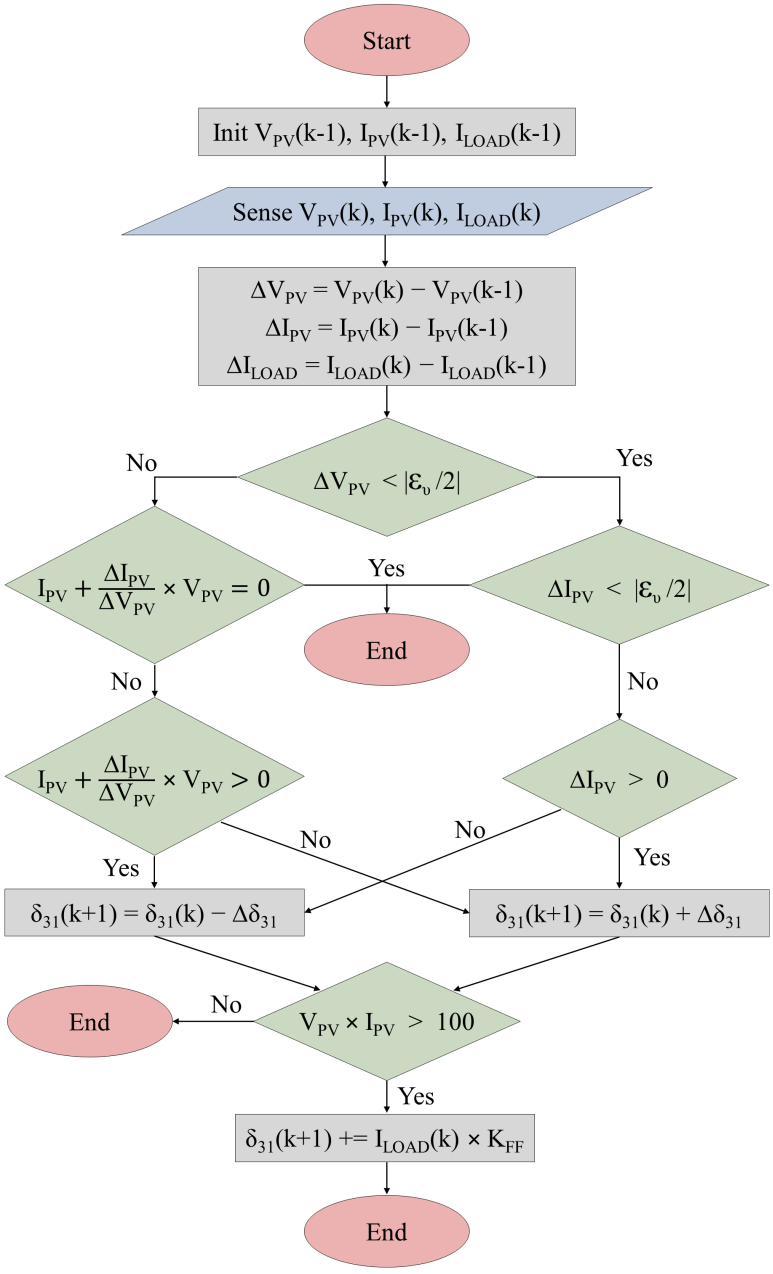


Figure 2.19: One control cycle MPPT algorithm flow chart.

2.2.4 Simulation Results

The control strategy of the TAB has been validated with different simulations. Results are shown considering a one-day irradiation profile, compressed in 240 s to reduce simulation times. However, the computational time with the OPAL simulator is still about 8 hours. This is due to the small simulation step of 25 ns and the 240 s simulated. Figure 2.20, shows the results with summer standard irradiation and temperature conditions in Parma, Italy, with a repeating load step profile. The three P_{bus} steps are 64 W, 256 W, and 620 W (blue), changing every 20 s. When the irradiation is 0 W/m^2 and the capacitor C_{PV} is discharged, V_{PV} (black) is 0 V. A low ripple on V_{bus} (blue) has been registered, below 0.5 V. The battery current I_{BAT} (red) supplies the fast load current I_{bus} (blue) changes, maintaining the PV power P_{PV} (black) on the MPP.

Figure 2.21, shows the results with winter standard irradiation and temperature conditions in Parma, Italy, with the same repeating load step profile of P_{bus}: 64 W, 256 W, and 620 W (blue). In this figure, an insert of the voltage V_{bus} (blue) ripple is shown.

Due to the different irradiation and temperature profiles, storage discharge can be observed with different ratings. Starting with a SoC of 50%, with summer conditions the discharge is slight, while with winter ones, a heavier discharge can be observed. The MPP is maintained with different load profiles and conditions in both simulations, obtaining the maximum available power at the defined irradiation and temperature conditions.

Simulation results show as well critical points of the TAB topology. In particular, with low irradiation and heavy load conditions, power losses increase. The high load factor and low distribution ratio between the ports induce a huge amount of reactive power to flow also on the solar PV side port where low active power is obtained [60]. This characteristic of TAB is an important disadvantage. In particular, low voltage high current applications are more stressed by the reactive power always present in the ports also without power transfer [61]. An overall efficiency can be estimated as well. Considering the winter condition simulation at around 120 s: P_{bus} = 620 W, P_{PV} = 314 W, and P_{BAT} = 383 W. This means that the efficiency of $\frac{P_{bus}}{P_{PV}+P_{BAT}}$ is 88.9 %.

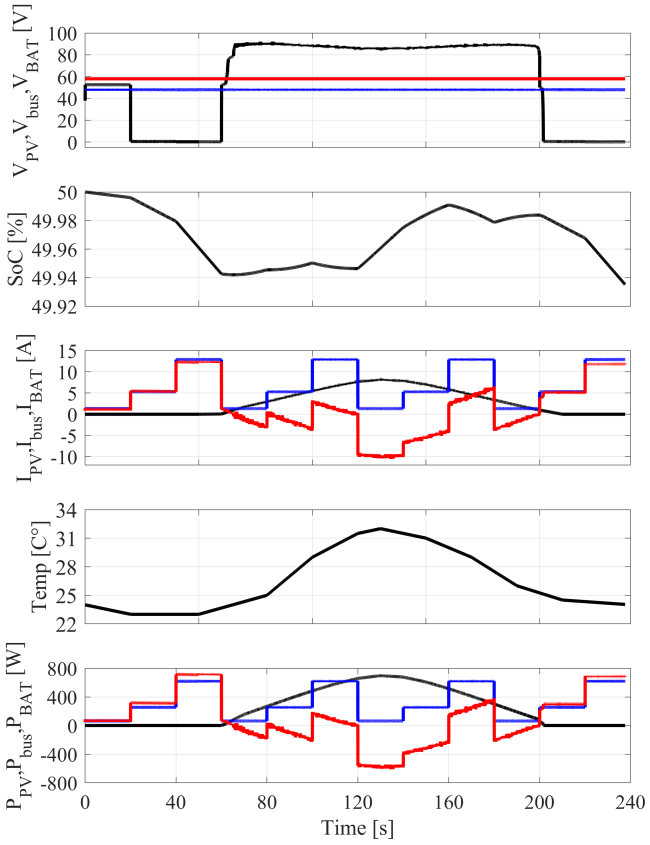


Figure 2.20: Simulation results in summer standard conditions for Parma, 44°45'53"N 10°18'26"E, Italy. V_{PV}, I_{PV}, P_{PV} (black), V_{bus}, I_{bus}, P_{bus} (blue), V_{BAT}, I_{BAT}, P_{BAT} (red), SoC, Temp.

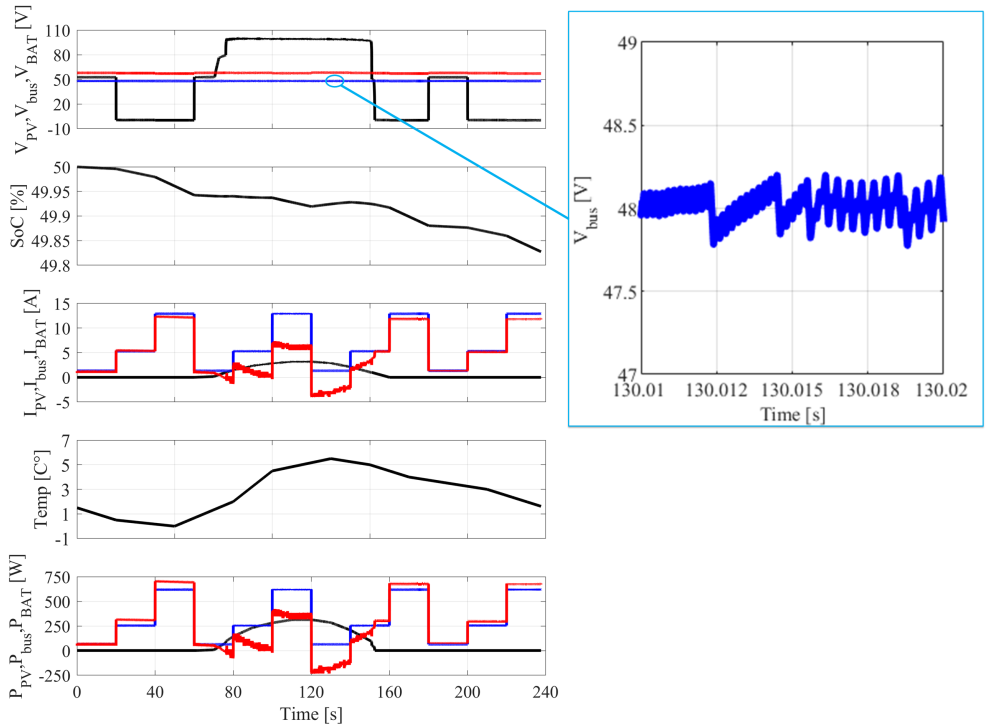


Figure 2.21: Simulation results in winter standard conditions for Parma, 44°45'53"N 10°18'26"E, Italy. V_{PV}, I_{PV}, P_{PV} (black), V_{bus}, I_{bus}, P_{bus} (blue), V_{BAT}, I_{BAT}, P_{BAT} (red), SoC, Temperature. In the insert, a part of the ripple voltage V_{bus} is magnified.

Considering the case of low irradiation, and high P_{bus} at 50 s: P_{bus} = 620 W, P_{PV} = 0 W, and P_{BAT} = 701 W. The efficiency, in this case, is 88.4 %.

2.2.5 Model Validation

Two TAB circuit prototypes have been designed for both early tests for the model validation and experimental results. The first one uses TPH3212PS GaN transistors by Transphorm ($V_{ds(MAX)}$ = 650 V, $I_{ds(MAX)}$ = 27 A, $R_{ds(on)}$ = 72 mΩ). The second one uses EPC9047 half-bridge boards with the EPC2033 transistors ($V_{ds(MAX)}$ = 150 V, $I_{ds(MAX)}$ = 48 A, $R_{ds(on)}$ = 7 mΩ). For space limitations, the first prototype will not be discussed, more details can be found in [A1, A9]. The second prototype, with the EPC2033 transistors, has been designed with an ad-hoc interface board for the micro-controller unit (MCU) connections, and the current and voltage sensing circuits. The MCU that has been chosen is the ST Microelectronics NUCLEO-F767ZI. I_{PV}, I_{bus}, and I_{BAT} current sensing have been provided with three integrated ACS712 hall effect-based linear current sensors. For the voltage sensing of V_{PV}, V_{bus}, and V_{BAT}, a resistor voltage divider has been used. The reduced voltage outputs of the voltage dividers, have been connected to three AMC1100 isolated amplifiers for the isolation between the ports and the logic circuitry.

The six PWM signals generated by the NUCLEO board (three phase-shifted PWMs with the relative complementary signals) are decoupled for isolation through six HCPL2300 optocouplers. The PWM signals have been generated through the use of TIMER 1 with a center aligned counter based on the frequency of 108 MHz. A second timer, with the same internal clock frequency, triggers the ADC converter at a frequency of 10 kHz. The ADC callback function is used to update the voltage and current values, and change the phase-shifts between the PWM signals.

The ad-hoc interface board and the EPC9047 boards have been interconnected through a stripboard, with accordingly soldered connectors. In the appendix, the circuit schematics of the interface board are shown, with the relative Altium layout. In figure 2.22, the test bench is shown with the oscilloscope, thermal Infrared (IR) camera, and the TAB prototype.

The simulated model has been validated through early tests under certain condi-

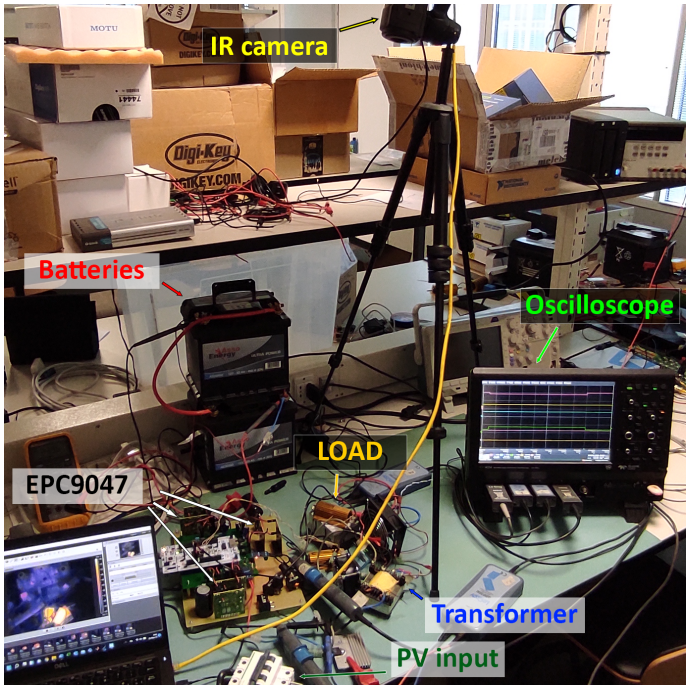


Figure 2.22: TAB prototype test bench with six EPC9047 half-bridge boards.

tions. The transformer currents have been taken as a reference, in order to validate the model at the transistor level. For this purpose, solar PV modules have been replaced by a DC generator connected to the first port. The tuning of the PI block parameters for the V_{bus} control loop is therefore simplified and can be easily compared between simulation and experimental results. Replacing the first port with a DC generator instead of solar PV modules doesn't change the currents and voltages on the transformer, which can be compared with those of the simulations.

In figure 2.23, the gate signals G_1, G_2, G_3 (yellow), input voltages V_{PV}, V_{bus}, V_{BAT} (red), output currents I_{PV}, I_{bus}, I_{BAT} (green), transformer currents I_1, I_2, I_3 (blue), and power transfer of each port P_{PV}, P_{bus}, P_{BAT} (orange) are shown. The boundary conditions are: V_{PV} = 60 V, $V_{BAT} \cong$ 12 V (one battery). As load, a power resistor of R_{LOAD} = 5 Ω has been used. The phase-shifts for these early tests have been fixed at δ_{12} = 0.47 and δ_{13} = 0.45.

With the same conditions, the MATLAB/Simulink model has been simulated. The results of the simulation are shown in figure 2.24. Comparing with the experimental results, a good matching has been proved, allowing to consider the model reliable with different working conditions. Considering power values, an error of 1 % is registered, while on the transformer currents, 0.7 % on the RMS values. A slight difference can be noticed in the behavior of the port currents I_{PV}, I_{bus}, and I_{BAT}. This can be due to the battery and DC voltage generator models, as well as some parasitic element, that hasn't been considered in the simulation model.

2.3 Experimental Results

In this section, the experimental results of the TAB prototype are shown. During the different tests, the irradiation values changed sensibly. Therefore, experimental with the TAB at the same environmental conditions are non-repeatable tests.

A first test has been done with a voltage generator as a PV source fixed at V_{PV} = 40 V, one battery, and a bus voltage controlled at V_{bus} = 5 V. On the load side: a 10 Ω power resistor is connected directly to the bus port, and a second 10 Ω resistor is connected in parallel to the first one through a relay. For this test, δ_{13} has been fixed

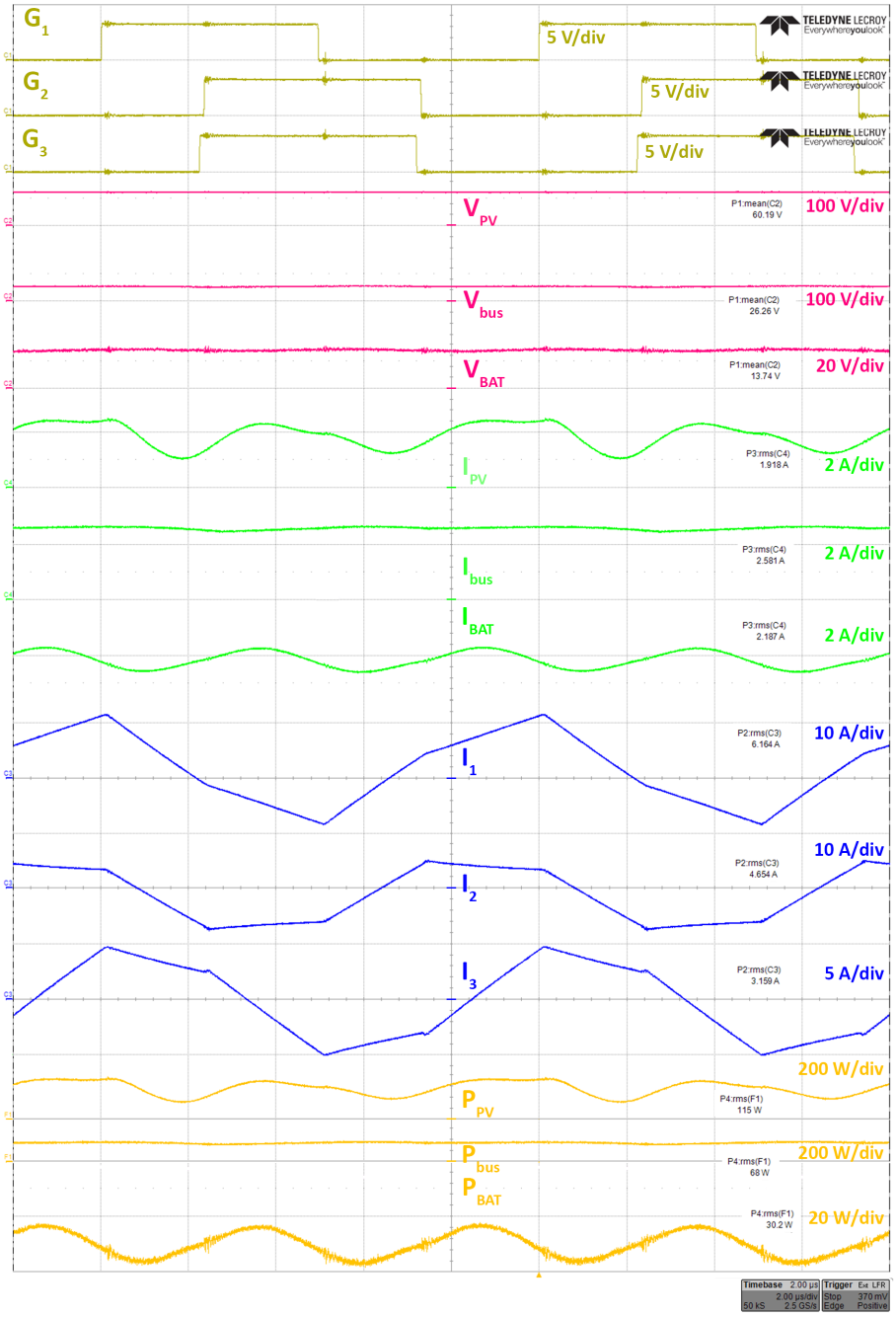


Figure 2.23: Experimental results of the gate control signals (yellow), port voltages (red), port currents (green), transformer currents (blue), and port power transfers (orange). Boundary conditions: V_{PV} = 60 V, V_{BAT} = 12 V (one battery), R_{LOAD} = 5 Ω, δ_{12} = 0.47, and δ_{13} = 0.45. Settings of the oscilloscope are shown in the figure, whit a time base of 2 $\mu s/div$.

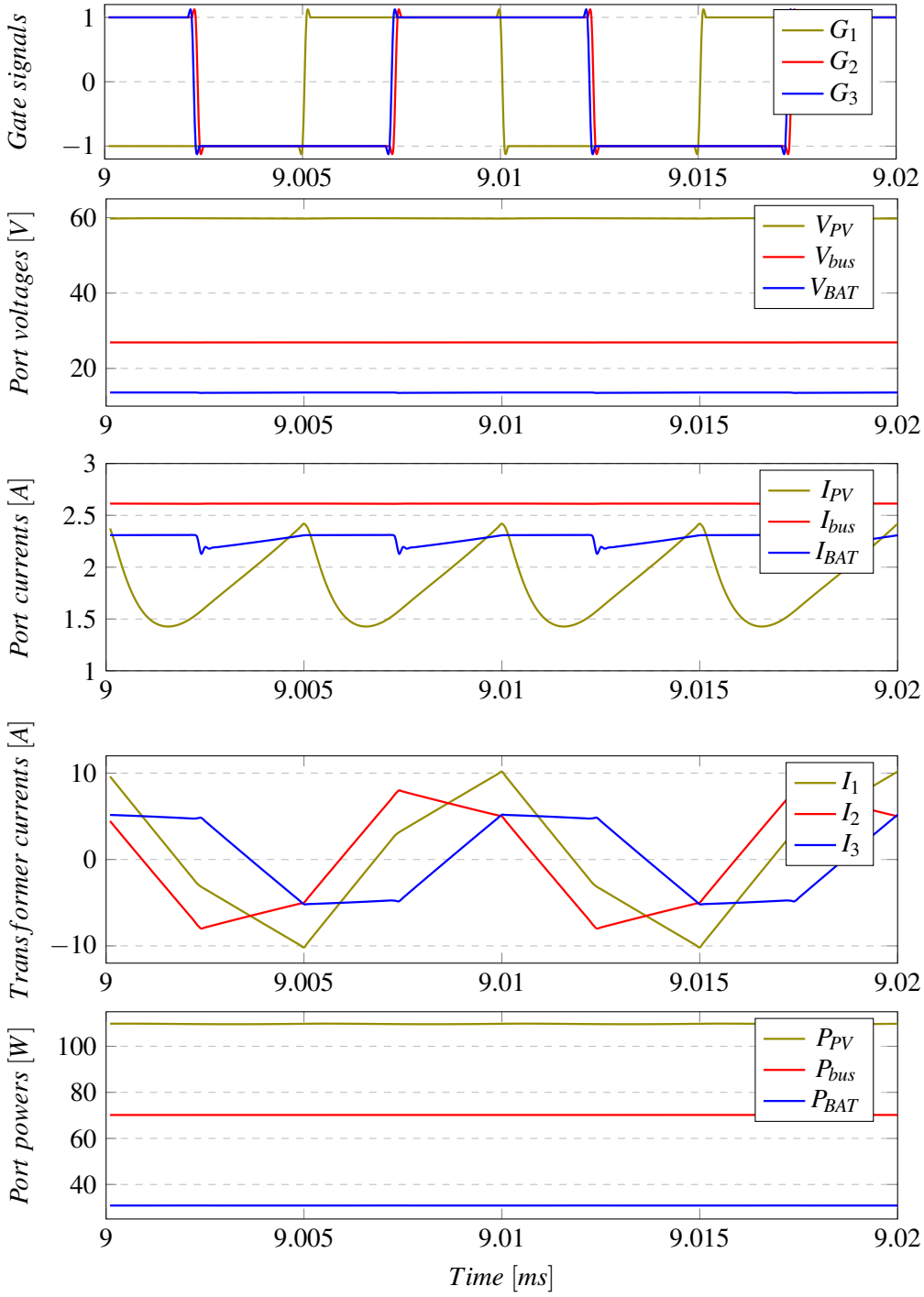


Figure 2.24: Simulation results with V_{PV} = 60 V, V_{BAT} = 12 V (one battery), R_{LOAD} = 5Ω, δ_{12} = 0.47, and δ_{13} = 0.45. The time window is 20 μs, starting from steady-state conditions at 9 *ms*.

at 0.16. The control parameters for the PI block are set as the same extracted from the simulations: $K_{pA} = 6 \times 10^{-3}$ and $K_{iA} = 10$. The feed forward on the current I_{bus} has been controlled with a constant $K_{FF} = 2.6 \times 10^{-3}$.

Figure 2.25, shows the experimental results to evaluate the V_{bus} control loop.

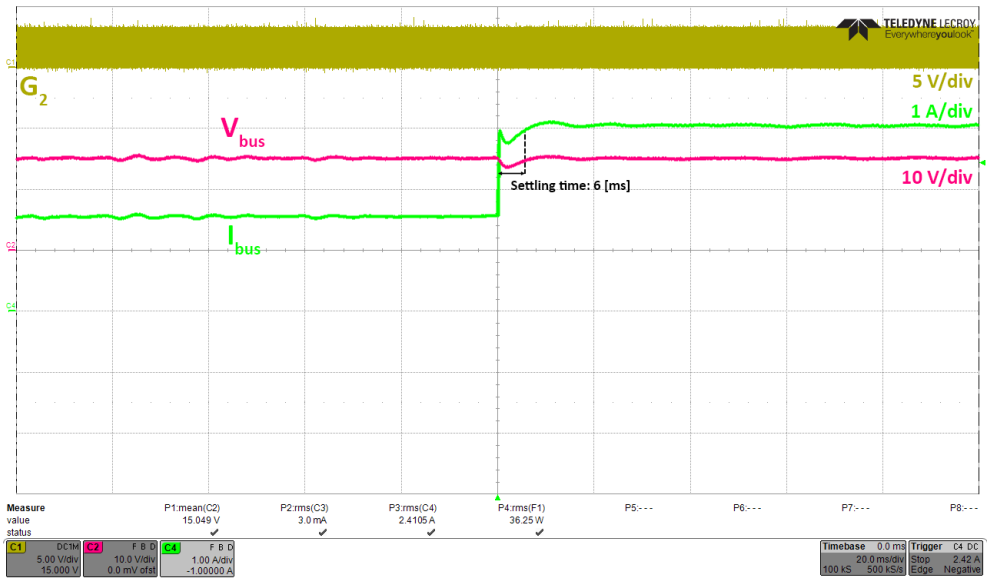


Figure 2.25: Experimental results of the voltage V_{bus} and the current I_{bus} in relation to a load change from 10 Ω to 5 Ω, with a fixed δ_{13} and a controlled δ_{12} for a 15 V V_{bus}.

Setting the trigger to 2.42 A on the I_{bus}, a capture of the voltage V_{bus} and current I_{bus} provides the behavior in case of load change from 10 Ω to 5 Ω. V_{bus} is controlled at 15 V, and the power P_{bus} goes from 22.5 W to 45 W. The settling time of the V_{bus} voltage to reduce the peak to peak value below 0.3 V (2 % of the value), is about 6 ms. This value is compatible with the simulation results shown in figure 2.13 and 2.14.

A different test has been done with two PV modules in series, four batteries in series, and a load voltage controlled at V_{bus} = 36.5 V. On the load side: a 10 Ω power resistor is connected directly to the bus port, and a second 10 Ω resistor is connected

in parallel to the first one through a relay. In these tests, δ_{13} is controlled for MPPT, with a feed forward on the current I_{bus} controlled with a constant $K_I = -2.3 \times 10^{-3}$. Figure 2.26, shows the experimental results, where every second the relay duplicates the power absorption on the load.

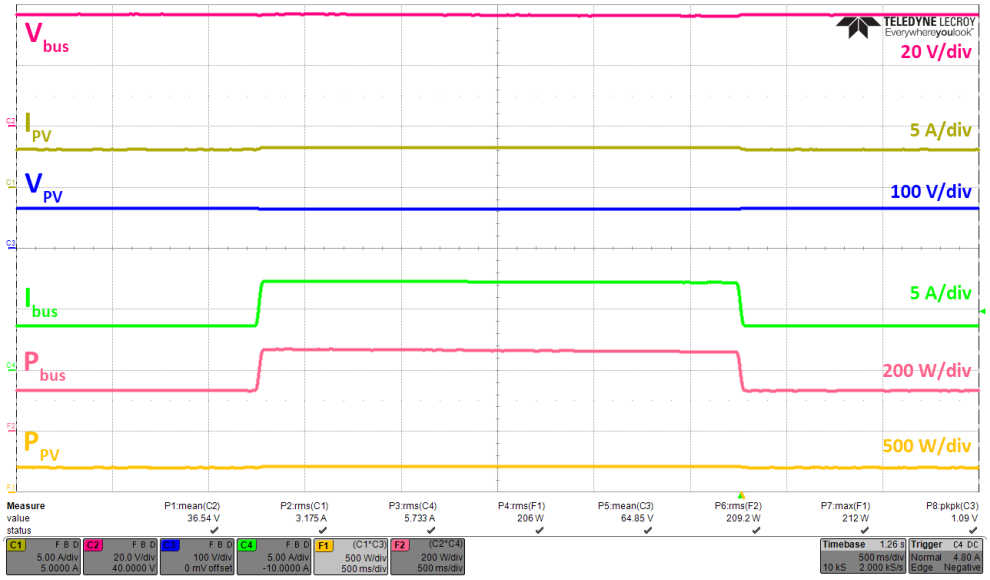


Figure 2.26: Experimental results of the V_{bus} and the current I_{bus} in relation to a load change from 10 Ω to 5 Ω. V_{bus} is the magenta trace, I_{bus} is the green trace, V_{PV} is the blue trace, I_{PV} is the yellow trace. Two math signal has been calculated with the oscilloscope: P_{PV} (yellow) and P_{bus} (magenta).

In this case, the average extracted power from the solar PV modules is $P_{PV} = 206$ W. The average power delivered to the load, P_{bus}, is 209.2 W. The battery interacts for 3 seconds receiving power, and the other 3 seconds where a 5 Ω load resistance is active, delivering power. The average value of power delivered by the battery is 38.9 W. This means that the TAB converter has an efficiency of $\frac{P_{bus}}{P_{PV}+P_{BAT}} = 85.4\%$.

Chapter 3

DC Bus Devices

This chapter presents the devices connected to the DC bus for the load interface. Figure 3.1, shows the proposed NG architecture where the devices analyzed in this chapter are highlighted.

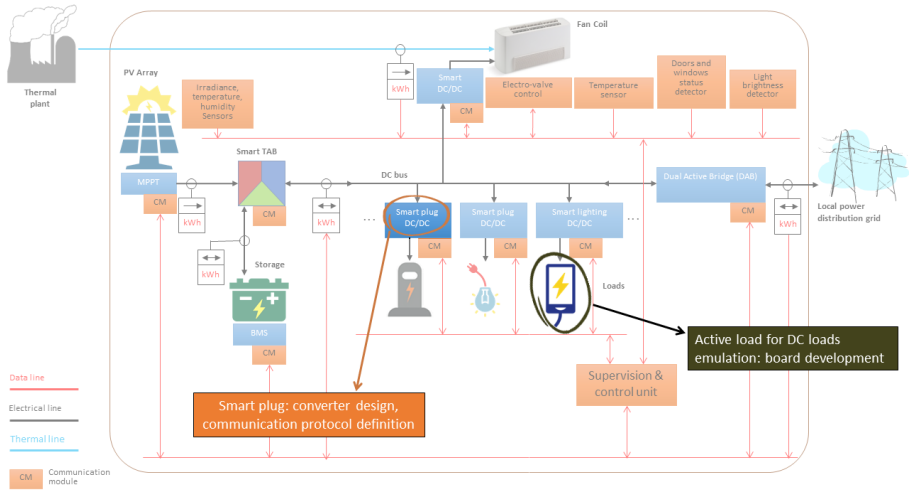


Figure 3.1: Proposed NG with a focus on smart plug and active load.

3.1 Smart Plug

The proposed NG has three main elements that can be identified: the solar PV modules for the power production, the battery for energy storage, and the supervision and control unit. However, for the load interconnection to the DC bus, small DC/DC converters have to be used. These converters should be able to monitor the energy consumption of the loads and communicate the power transfer values to the supervision and control unit. At the same time, intercommunication with the load can be established to reduce or increase the voltage and current levels, i.e. the power transfer, in dependence on the device attached requirements and the available NG power. If the load is not a smart device, the output voltage can be fixed on the indication of the supervision and control unit. Therefore, the smart plugs include a power electronic stage with monitoring and control circuitry and a communication module. A representation of the smart plug with the attached DC load is shown in figure 3.2.

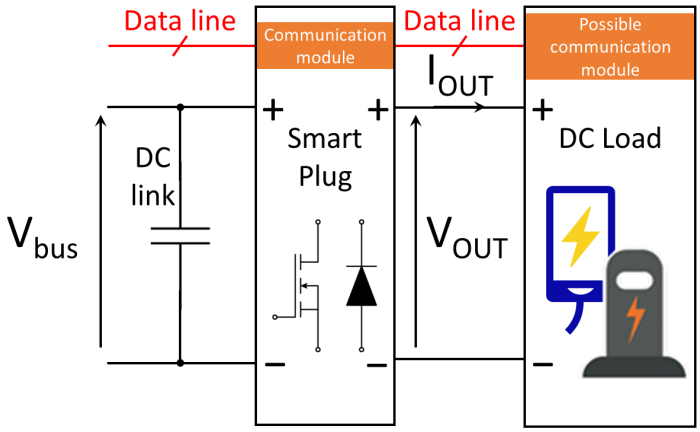


Figure 3.2: Smart Plug block diagram representation.

On the market, smart plugs are already present, but always AC powered and only for consumption monitoring and load on-off control. In literature, different research on AC smart plugs can be found, where voltages and currents values are acquired and the data are transmitted to a central supervision unit. In [62], a smart plug prototype with voltage and current sensing and power factor determination is proposed. In this

prototype, a Zigbee module is implemented for the data transmission to a server. In [63], a similar smart plug is proposed but with a Bluetooth module for the data transmission and a Raspberry board as a server. The same in [64], but with a Wi-Fi communication module. A different configuration is proposed in [65], where the concept of a central unit is replaced by distributed supervision units present in the individual smart plugs. In this case, a communication protocol is defined where the information about the consumption, movements, brightness, temperature, and humidity are transmitted between the smart plugs after specified queries. Therefore, depending on the connected loads, different sensors can be included in the smart plugs to optimize management efficiency. The proposed smart plug prototype uses also deep learning algorithms to foresee if the user will be connecting a specific load or not. Therefore, the smart plugs try to anticipate when there will be power consumption. In [66], machine learning algorithms have been used to classify the connected loads. In this case, power consumption data are used to determine if the load is a continuously operating load, meaning that in a 24 hour time window the load is continuously active, a discontinuous load, or a ghost load (stand-by). This classification is used to foresee planning actions, such as from which source the load should be powered (solar PV, battery, PG network, etc.), and to foresee the battery SoC over time.

The characteristics of the different prototypes, and the commercially available smart plugs, are necessary but not sufficient for smart consumption management [67]. For the NG proposed in this work, a solution with DC/DC conversion is necessary. The concept is similar to the USB Type-C protocol with PD, widely used in the market. By integrating a USB-C PD device with a Wi-Fi connection capability, the power profiles in relation to the load request and NG power availability can be determined. With this protocol, the load and the power source (i.e. the smart plug connected to the DC bus) exchange information about the voltage and current ratings and determine the power absorption profiles. For example, a fast or a low charge of an electric vehicle could be contracted depending on the solar PV modules production or the battery SoC. In table 3.1 the main characteristics of a smart plug for smart consumption management are shown.

A retrofit of existing electrical local networks can be done with the implemen-

Table 3.1: Smart plug characteristics.

Consumption monitoring	The user is able to be aware of the energy consumption, but also to detect some anomalies or efficiency drops of a connected device.
Load identification	The system is able to know which loads are connected in order to plan and efficiently control the loads. In this case, machine learning techniques can be useful to recognize the loads and their management by the power absorption profiles.
Control and planning	Load turn-on can be planned depending on the available energy, or when the electrical energy on the market is cheaper.
Inhabited detection	Information about the living spaces can be registered to reduce unnecessary energy consumption such as for electronic devices, but also thermal plants or air conditioning systems.
Standby power killer	Standby devices can be recognized and turned off with a programmed algorithm to reduce energy consumption. This function can use the inhabited detection for smarter management.
Thermal protection	Electrical system safety can be increased with a thermal or overloading detection function.
Indoor localization	The smart plugs communicate between themselves to identify load iterations between the same rooms or environment.

tation of smart plugs instead of classical wall sockets. This means that smart plugs have to be small, compact, and compatible in dimensions for a retrofit. Moreover, the first commercial solutions could include both classical AC sockets and DC ones. This results in strict space constraints, meaning harsh electrical and thermal management requirements. From the electrical point of view, sensors and communication boards have to be considered as well, such as Wi-Fi, Zigbee, or Bluetooth. Interference between power electronic switching boards and communication modules has to be avoided. Therefore, some precautions should be considered with the layout design. Moreover, the costs of the device should be reasonable for a commercial retrofit, considering, in particular, the number of smart plugs needed in a NG network. Another consideration can be done on security issues, as explored in [68]. In fact, the increased number of interconnected devices and data exchange rate leads to higher cyber-attack risks.

3.1.1 USB Type-C Power Delivery

To better understand the smart plug protocol concept, this subsection is dedicated to the USB Type-C protocol. The USB-C standard is based on a reversible 24 pin connector. Data can be exchanged with a 40 Gbit/s rate, while electrical power up to 15 W with 5 V and 3 A maximum ratings. However, with the power delivery standard, the same connector can achieve up to 100 W, with 20 V and 5 A maximum ratings. These characteristics allow supplying a wide range of electronic devices, such as laptops, TVs, smartphones with fast charging capability, etc. For market integration, the standard is compatible as well with the USB 2 and USB 3 protocols, but also for audio and video data transmission replacing HDMI connectors. In figure 3.3, the USB Type-C connector pin-out is shown.

Ground pins A1, A12, B1, B12, and V_{bus} pins A4, A9, B4, B9 are used for the PD power transfer protocol. The orientation of the cable is interchangeable and detected by the pins CC1 and CC2, which are used as well for the data exchange between source and sink. Therefore, the voltage and current levels, i.e. the power profile definition, are defined through a two-pin (CC1 and CC2) physical layer. SBU1 and SBU2 are used for the low power supply, always active for the control and PD protocol acti-

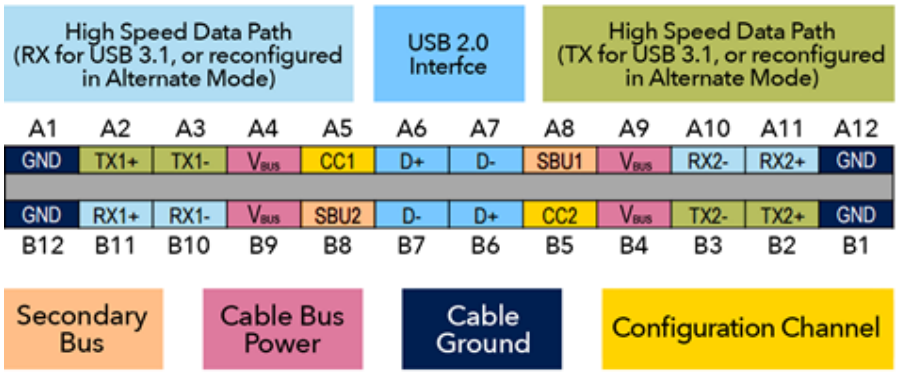


Figure 3.3: USB Type-C connector pin-out.

vation. The other pins: TX, RX, D+, and D-, are used for the USB 3 and USB 2 data transmission protocols. An overview of the operation modes and maximum rating is shown in table 3.2.

Table 3.2: USB protocol characteristics.

Mode of operation	Nominal voltage	Maximum current	Maximum power
USB 2.0	5 V	500 mA	2.5 W
USB 3.1		900 mA	4.5 W
USB Type-C		3 A	15 W
USB PD	up to 20 V	up to 5 A	100 W

Respect to previous USB standards, the Type-C PD protocol includes some necessary features for the design of a smart plug. The first characteristic of this protocol is the negotiation capability of the power role, meaning that the devices can both supply or absorb power depending on the application. Then, the power profile can be negotiated. Information about maximum ratings and possible voltage and current values of the source and the sink are exchanged and the desired power profile is defined. The reversible cable can be connected in the two orientation mode through a hardware detection obtained by a pull-up/pull-down resistor in the plug. Moreover, the cable for the USB Type-C protocol has to be electronically marked. The devices read the type and characteristics of the cable which is connected to define maximum

ratings of power transfer and data bitrate. Finally, the protocol allows an alternate-mode negotiation. The information transferred with other protocols can be redirected through the USB Type-C configuration pins (i.e. video information). The USB Type-C PD protocol is divided into different levels, as shown in figure 3.4.

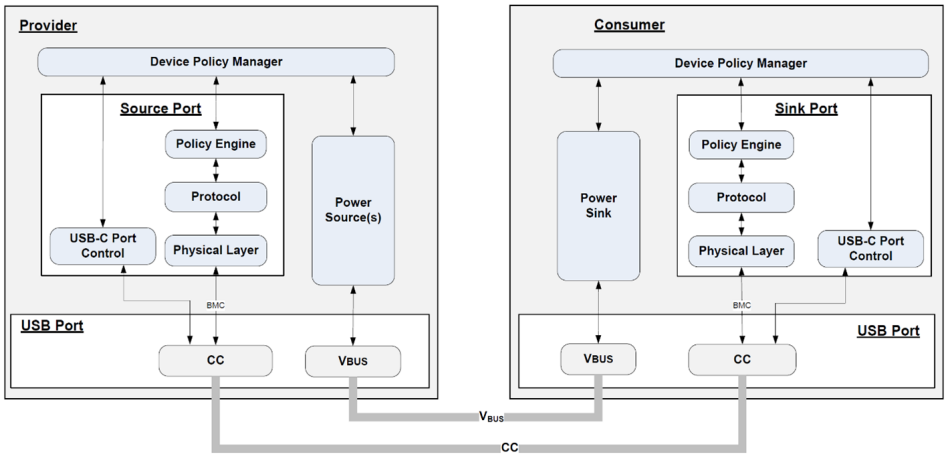


Figure 3.4: USB Type-C PD protocol layers.

When considering the PD protocol, the devices can take three power roles: source (provider), sink (consumer), or dual-role. In the dual-role mode, the source and sink roles can be exchanged and controlled by software. The whole protocol is defined by a multi-level architecture: Physical Layer (PHY), protocol layer (PRL or PRT), Policy Engine (PE), and Device Policy Manager (DPM). The PHY transmits and receives the messages through the configuration channels (CC1-CC2). It includes error detection, such as data collision, with a cyclic redundancy check. The PRL reconstructs the messages and controls the transmission and reception. The PE coordinates the message sequence to define the PD agreement. At the same time, it contains the information on the policy condition through a finite state machine. This information can be used to control the DC/DC converter of the source in order to supply the defined voltage. The DPM coordinates the USB PD resources of the device. One or more power ports can be used and addressed on the USB connector.

At the beginning of each power profile negotiation, a 5 V voltage is applied to the V_{bus} pins. The source provides a message of its profile capabilities, and the sink responds with its desired choice. This exchange can be repeated in case the power profiles capabilities of the source change. Afterward, the reference signal for the source DC/DC converter is set and a ready message is sent, requiring sink acknowledge response, in order to connect the V_{bus} to the desired voltage. A graphical representation of the PD protocol communication message exchanges is shown in figure 3.5.

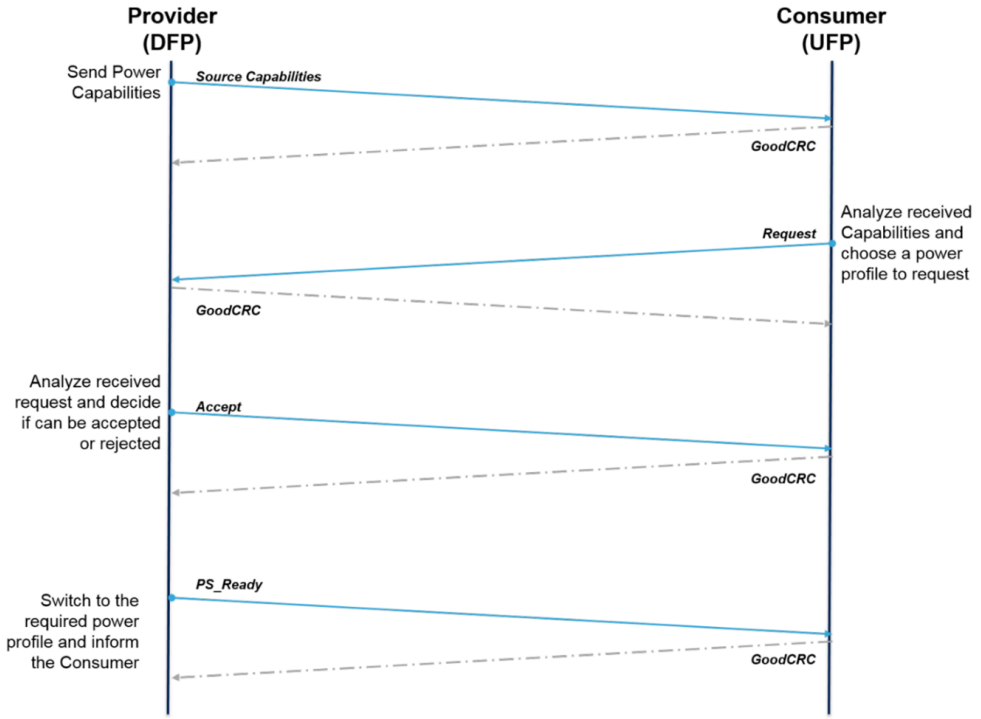


Figure 3.5: USB Type-C PD protocol communication graphical representation.

The power profile messages that are sent between source and sink are called Power Data Object (PDO). The PD protocol provides different types of PDO: fixed, variable, or battery supply. With fixed supply PDO, the source and the sink define the voltage in between a 20 % error range. With variable supply, a minimum and a max-

imum voltage are defined. Finally, with battery supply, the minimum and maximum voltage are defined for optimum battery charging. Each PDO profile contains the current value information. For the source, it consists of the maximum current supply capability, for the sink the minimum required current. The algorithm compares therefore the PDO between sink and source. Starting from the PDO with higher priority, the voltage and the current are compared with the following conditions:

$$V(SNK\_PDOi) = V(SRC\_PDOj);$$
$$I(SNK\_PDOi) \leq I(SRC\_PDOj).$$

where $V(SNK\_PDOi)$ and $I(SNK\_PDOi)$ are namely the voltage and current values of the i-th feasible sink PDO, $V(SRC\_PDOj)$ and $I(SNK\_PDOi)$ are namely the possible voltage and current values of the j-th feasible source PDO.

3.1.2 Smart Plug Prototype

To design a smart plug prototype in line with the optimal smart plug characteristics described in section 3.1, a first prototype has been developed to be compatible with the USB Type-C PD protocol. The prototype consists of two main parts: a DC/DC buck converter for the voltage regulation from V_{bus} to the load required voltage and a logic control board for the protocol implementation. The prototype block diagram is shown in figure 3.6.

The decision to use the PD protocol has been made to speed up the development times, and separate the DC/DC converter analysis from a possible ad-hoc communication protocol definition. Moreover, the development of a PD protocol compatible solution is of great advantage if the smart plug has to be connected to already commercially available devices. On the other side, the USB-C PD doesn't allow to transfer power profiles higher than 100 W, therefore, future development is needed to define a compatible communication protocol.

Nevertheless, the buck converter has been designed to keep low dimensions, high power density, and good thermal behavior. For this purpose, GaN transistor devices have been used. The DC/DC converter is controlled by an ST Microelectronics MCU,

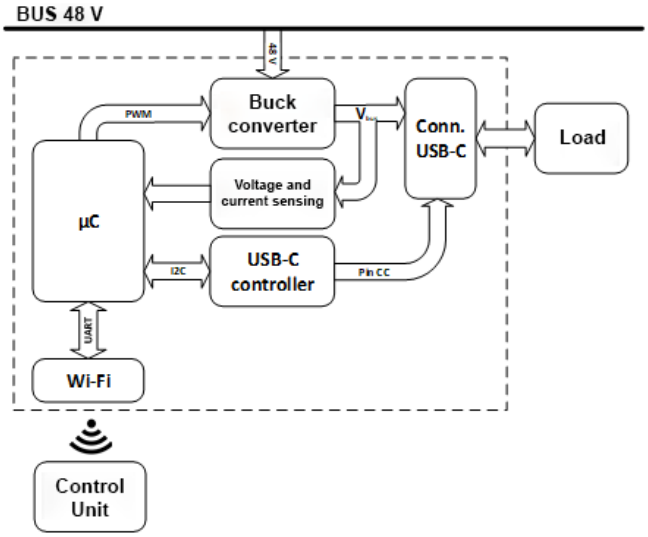


Figure 3.6: Smart Plug prototype block diagram.

the NUCLEO STM32F446RE board. The board uses the PWM generation function through a peripheral TIMER, and the analog to digital conversion function through the ADC peripheral unit. Moreover, the MCU controls the USB Type-C PD status and allows communication between the smart plug and the supervision unit over a Wi-Fi network. The USB Type-C PD protocol with the different control layers is controlled by two ST Microelectronics evaluation boards: the STEVAL-ISC004V1 with source role, and the STEVAL-ISC005V1 with sink role.

The STEVAL-ISC004V1 board uses the STUSB4710 integrated circuit for the PD protocol controller. On the same board, a synchronous buck converter is provided up to 60 W maximum power deliver, which is not enough for the desired power ratings. For this reason, the converter is bypassed and substituted with the ad-hoc designed external DC/DC converter. Communication with the NUCLEO board is provided through the I2C standard. The USB controller STUSB4710 allows up to 5 power profiles (PDO). The feedback loop for the output voltage control is provided by a resistor network.

A requirement of the DC/DC converter that substitutes the on-board buck con-

verter for the PD protocol integration, is the maximum step response of 300 ms. Therefore, the control should be fast enough to reach the output voltage ±20% in between the declared 300 ms. Simulations for the component sizing and stability analysis are carried out with MATLAB/Simulink software. In figure 3.7, the MATLAB/Simulink model of the buck converter is shown.

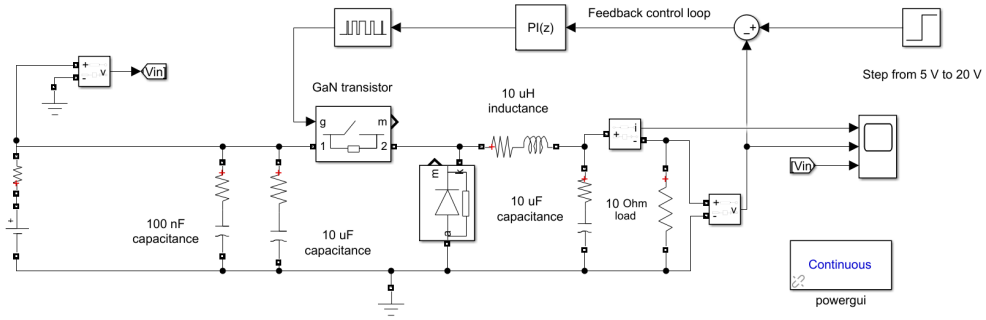


Figure 3.7: Buck converter simulation model for the smart plug prototype.

PI control is used for the output voltage regulation loop. The converter has a 48 V input voltage and provides from 5 V to 20 V as output voltage. The switching frequency is set to 1 MHz, which allows very small passive components. The maximum allowed output current I_{out} is set to 10 A, which is a higher rate than the maximum allowed current for the USB Type-C PD protocol. However, future works can replace the PD standard and the smart plug could be used also for higher power transfer (up to 200 W). The output voltage ripple requirement is defined below 0.1 V, which is 2 % in the case of 5 V voltage output, but it is kept as a limit also for higher voltage values to improve the power quality. For simulations, a 10 Ω resistor as load has been set.

The PI block parameters fit has been done through the MATLAB system identification toolbox (SISOTool). The voltage transfer function is related to the PWM duty-cycle (ρ):

$$\frac{V_{out}}{V_{bus}} = \rho \times \eta \tag{3.1}$$

where η is the efficiency of the converter. Therefore, for a 48 V to a 5 V maximum step-down ratio, a minimum ρ of approximately 10 % is used. Efficiency decreases with a high step-down ratio, and the inductor (L) and capacitor (C) should be sized for a proper small voltage ripple. The following equations can help to define a first converter sizing, then values can be optimized based on the application [69]:

$$L = V_{out}\frac{(V_{bus} - V_{out})}{\Delta I_L f_{sw} V_{bus}} = \frac{215}{2 \times 10^6 \times 48} = 2.24\mu H \tag{3.2}$$

where f_{sw} is the switching frequency (1 MHz), ΔI_L is the inductor ripple current, which is considered 20 % of the maximum output current, I_{out} equal to 10 A, therefore, ΔI_L = 2 A.

$$C_{out} = \frac{\Delta I_L}{8 f_{sw} \Delta V_{out}} = \frac{2}{8 \times 10^6 \times 0.1} = 2.5\mu F \tag{3.3}$$

where ΔV_{out} is the maximum allowed output voltage ripple.

The DC/DC converter passive components have been defined exceeding the minimum calculated values and with commercially available devices. The inductor L has been defined to be 10 μH, characterized at 100 kHz, and with a resonant frequency of 6.25 MHz. As for the capacitor, a 10 μF capacitor has been used. A smaller 100 nF SMD capacitor has been connected in parallel to the output and input ports as well, with low parasitic inductance and resistance, for a good DC voltage by-pass function.

Figure 3.8, shows the simulation results with a step from 5 V to 20 V of the output voltage reference. This could be a possible requirement of the attached load, after the negotiation phase with the smart plug.

After simulation analysis, a prototype of the DC/DC converter has been developed. The GaN transistor used for the buck converter is the GS61004B of GaN System ($V_{ds(MAX)}$ = 100 V, $I_{ds(MAX)}$ = 38 A, R_{on} = 16 mΩ). As for the GaN driver, the LMG1205 of Texas Instruments with an integrated bootstrap diode has been used. Considering the switching frequency of 1 MHz, the maximum voltage and current ratings, and the fast switching dynamics of the GaN transistor, the MUR820G diode of Onsemi has been chosen accordingly (V_R = 200 V, I_{FM} = 16 A, V_F = 975 mV). This diode has a maximum reverse recovery time of about 35 ns. Voltage sensing

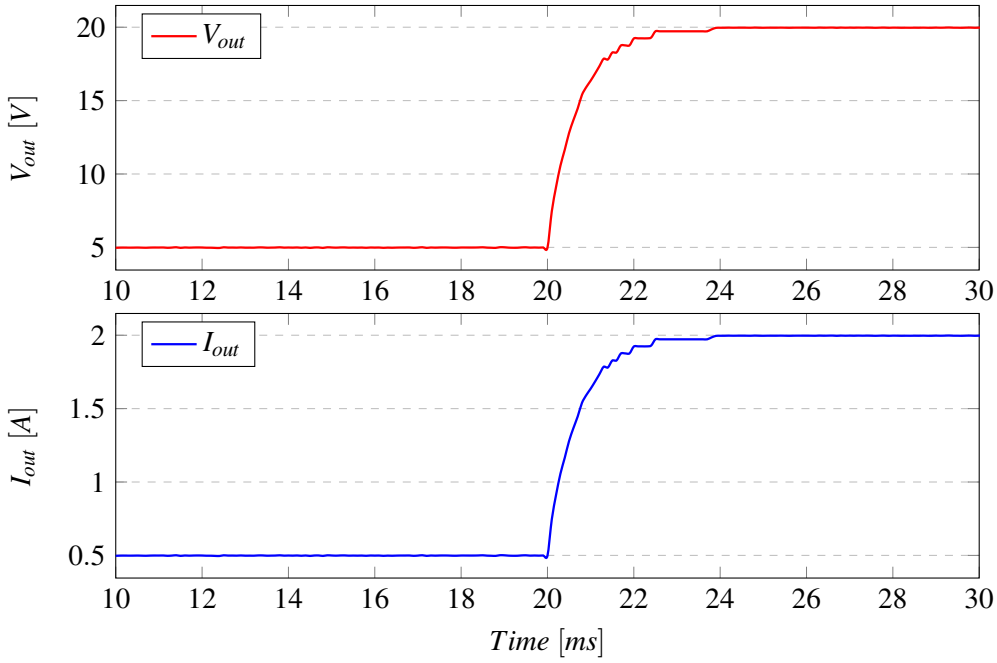


Figure 3.8: Simulation results of buck converter circuit: response to voltage reference step signal from 5 V to 20 V.

has been provided through a resistor network, connected to the NCS2333 operational amplifier. The NCS2333 has been chosen for its single supply property, allowed from 1.8 V to 5.5 V, and the low output offset. These characteristics enable a direct connection to the MCU ADC peripherals. As for the current sensing, the INA240A1DR integrated circuit has been chosen. This amplifier has a high PWM rejection voltage output, ideal for low voltages sensed on shunt resistors. The schematic circuits of the buck converter prototype are shown in the appendix. Figure 3.9, shows the buck converter prototype layout.

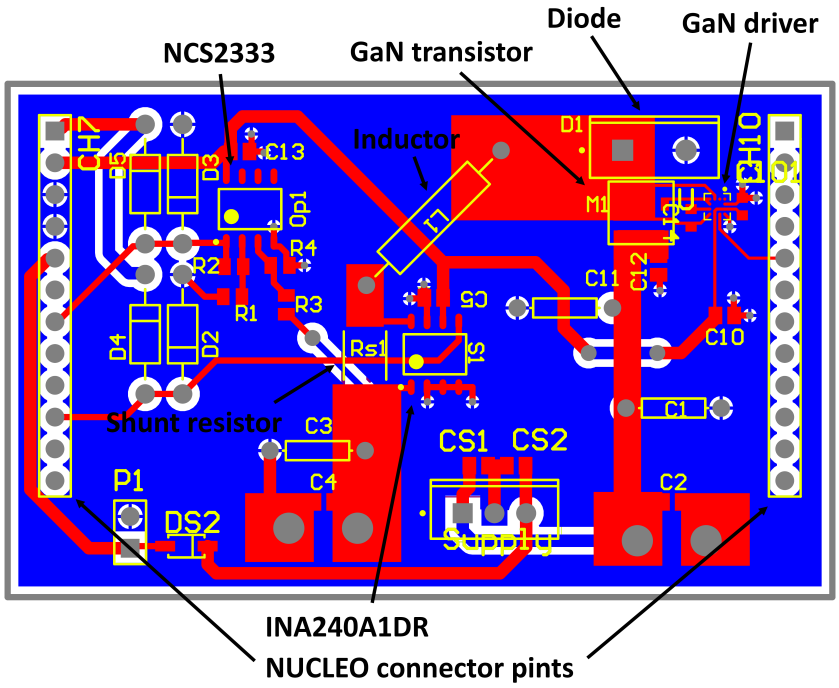


Figure 3.9: Buck converter board layout.

The buck converter board layout needed some design carefulness on both signal integrity and thermal management. On the other hand, the use of small size and number of components helped to obtain a very compact and small converter, therefore, reducing parasite inductance and resistance. The power signal path can be recog-

nized by the appositely large tracks from the input pads (C4) to the output pads (C2). M1 is the GaN power device, D1 is the power diode, and L1 is the buck converter inductance.

Finally, the smart plug prototype has been realized with the different boards (buck converter and USB Type-C evaluation boards). The USB-C PD protocol has been tested and the buck converter response is registered in the case of power profile negotiation of 20 V, starting from a 5 V power supply. In figure 3.10, the output voltage V_{out} is shown.

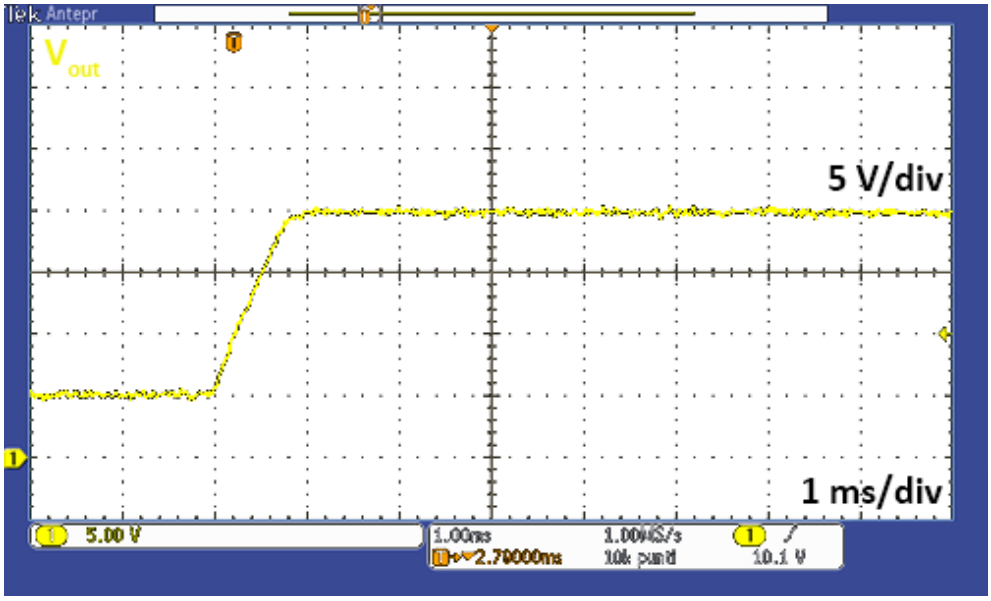


Figure 3.10: V_{out} voltage output of the buck converter after a 20 V power profile negotiation.

3.2 Active Load

The research activity on DC/DC converters, batteries, and solar PV modules with the nanogrid focus, needs an electronic programmable active load for electric tests.

Therefore, a board has been designed that emulates different loads that can be attached to the 48 V V_{bus} or the lower voltages that are provided by the smart plug. Moreover, the active load can be used to extract battery characteristics. Therefore, the requirements of the active load board for the NGs related circuits are:

- Input current I_{in} up to 10 A;
- Input voltage V_{in} up to 48 V;
- Maximum input current ripple ΔI_{in} of 0.2 A (2 % of the input current);
- Maximum input voltage ripple ΔV_{in} of 0.96 V (2 % of the input voltage);
- Maximum power absorption P_{in} up to 300 W.

The principle of the active load can be described as a variable resistor, where a PWM, generated by a general purpose microcontroller, modulates the resistor value. In figure 3.11, a block diagram represents the interconnection between the active load and the source under test.

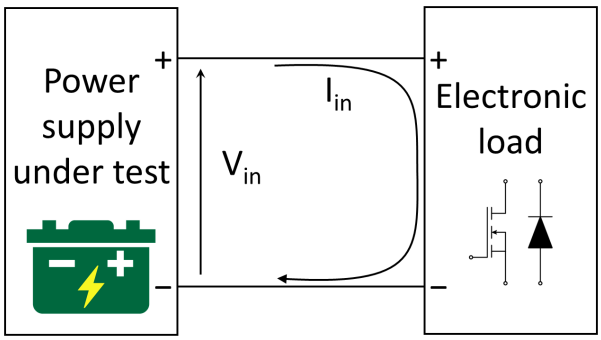


Figure 3.11: Active load block diagram.

The optimal characteristics of the active load should include: a large range of input impedance control, high resolution for current and power absorption, modularity achievable with multiple active loads in parallel, low input signal distortion, and low electromagnetic emissions. Different topology solutions can be designed to emulate

electronic loads. The easier solution can be the use of power resistors connected in series or parallel through pass transistors. However, only discrete power profiles can be obtained and the complexity of the circuit rises in relation to the required resolution and maximum power ratings. Generally, a very high number of power devices have to be implemented. Therefore, the temperature strongly influences the power absorption due to the resistance changes. A different solution is represented by the use of MOSFET transistors in the saturation zone [70]. Different MOSFETs can be connected in parallel and controlled by the same gate bias voltage. Considering a current control loop, the input output relation is due to the classical MOSFET characteristics. Therefore, the conditions are:

$$V_{GS} > V_{TH} \tag{3.4}$$

$$V_{DS} > V_{GS} - V_{TH} \tag{3.5}$$

$$I_{DS} = \frac{\beta}{2} \left(V_{GS} - V_{TH}\right)^2 \cdot \left[1 + \lambda \left(V_{DS} - V_{DSsat}\right)\right] \tag{3.6}$$

where $\beta = \mu C_{OX} \frac{W}{L}$ depends on the fabrication technology. In fact, μ is the charge-carrier effective mobility, C_{OX} is the capacitance of the oxide layer, W is the gate width, L is the gate length, λ is the channel-length modulation parameter, $V_{DSsat} = V_{GS} - V_{TH}$. In this case, the drain current I_{DS}, therefore, the input current of the active load I_{in}, is almost constant in relation to V_{DS}, and mostly depends on V_{GS}. However, second order effects due to temperature, carrier speed saturation, etc. can't be neglected. In fact, the gate to source voltage and drain current relation is influenced and leads to more complexity in the current control. The possible schematic realization (a), and working ranges (Safe Operating Area) (b) are shown in figure 3.12.

A different solution can be achieved with DC/DC converters such as with buck, boost, or buck-boost topology [71]. A power resistor can be used as load and the duty-cycle of the PWM control signal changes the absorbed power. Resolution of the power absorption is strongly related to the duty-cycle resolution, and the choice of the passive components to the switching frequency. A relatively good efficiency should

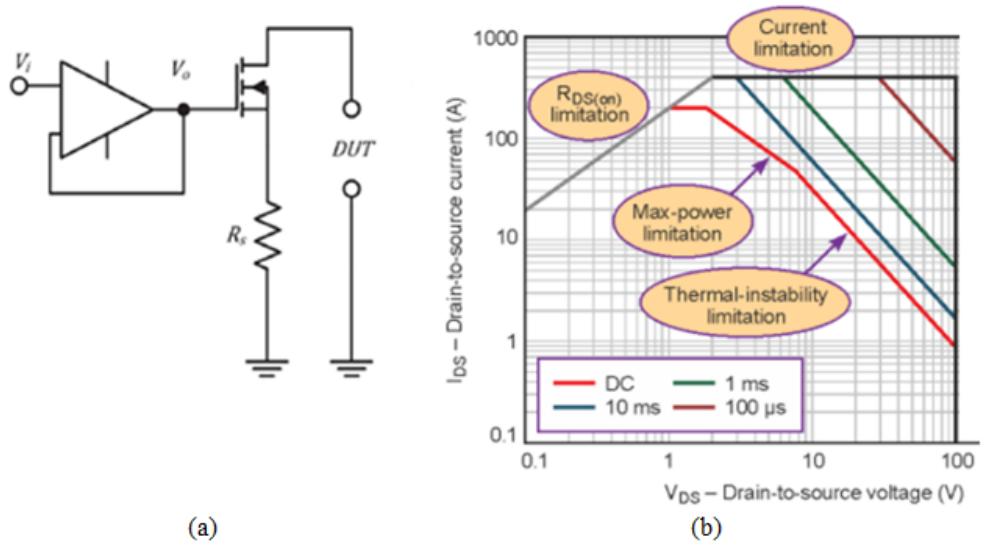


Figure 3.12: Active load schematic realization through MOSFET (a) and I_{DS} over V_{DS} characteristic with Safe Operating Area (SOA) representation (b).

be achieved in order to maintain the temperature dissipation on power devices under acceptable limits. Maximum current rating should be considered in the design and the component choice as well. Moreover, input signal distortions have to be considered due to the switching behavior of the circuit. Based on converters, a possible active load with energy recycling to the power grid can be designed [72, 73]. In this case, a DC/DC converter is interfaced with an inverter connected to the power grid, which absorbs the desired power. Figure 3.13, shows the working principle of an active load with energy recycling.

The energy recycling active load solution enables high power ratings without relevant power dissipation on the circuit. Board volumes can be reduced and in case of prolonged tests, an economic benefit can be obtained. However, reactive power control and feeding the AC grid should be considered. From the network management point of view, having feeding power from the user has to be controlled accordingly, as is it for solar PV modules with AC grid connection. Therefore, the power exchange should be negotiated and defined between the user, or prosumer in this case, and the

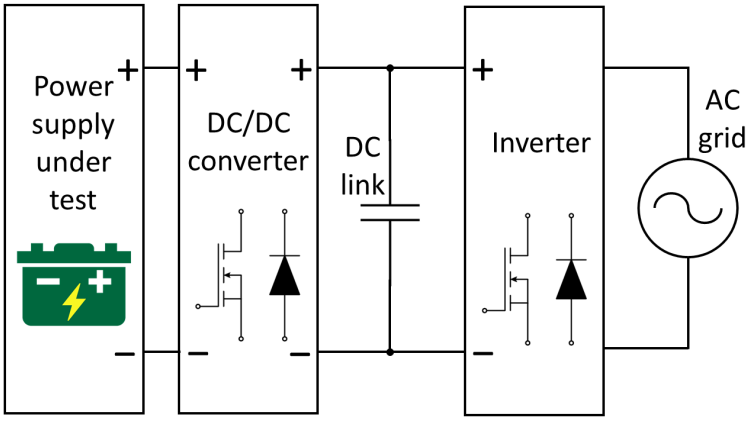


Figure 3.13: Active load with energy recycling block diagram.

power seller.

3.2.1 Active Load Prototypes

Starting from the different possible solutions, the electronic programmable active load for NG device tests has been defined through DC/DC converter-derived circuits. Two ad-hoc active load circuits have been designed to meet the application requirements. A first circuit solution consists of a buck-derived topology, where power resistors and power MOSFET are both used for power dissipation depending on the desired current and voltage values. The principle of work is the use of a PWM signal with duty-cycle modulation for the power profile definition. Respect to a buck topology, a power resistor is inserted as input of the circuit, together with capacitors for a good Low Pass Filter (LPF). On the other side, the load is not filtered for a low voltage ripple, but only to reduce harmonic distortions on the input. The power dissipation resolution is determined by the PWMs duty-cycle signal, which has a frequency of 100 kHz. The schematic of the active load circuit is shown in figure 3.14.

Also in this case, the main buck equations can be used:

$$V_{out} = V_{in} \times \rho \times \eta \tag{3.7}$$

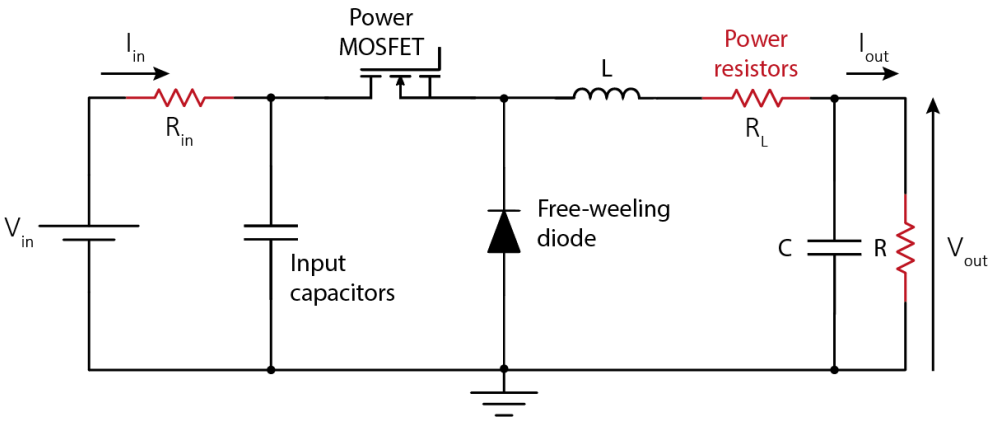


Figure 3.14: Active load schematic circuit: first proposed solution.

$$I_{out} = \frac{I_{in}}{\rho} \tag{3.8}$$

From these two:

$$\frac{V_{out}}{I_{out}} = \frac{\rho \cdot V_{in} \cdot \eta}{\frac{I_{in}}{\rho}} = \rho^2 \cdot \frac{V_{in}}{I_{in}} \cdot \eta \tag{3.9}$$

If the load of the buck converter is a resistor R, the circuit can be seen from the source point of view as a variable load R_{VAR} and defined with the equation:

$$\frac{V_{in}}{I_{in}} = R_{VAR} = \frac{R}{\rho^2 \cdot \eta} \tag{3.10}$$

Therefore, the dissipated power is controlled from the lowest value with duty-cycle equal to 0, and the highest power can be obtained with a duty-cycle equal to 1. In the first case, R_{VAR} tends to be infinitive. In the second case, R_{VAR} is equal to R over the efficiency η of the converter, which represents the input resistance, power MOSFET on-state resistance, parasitic resistance, etc. However, this is true in the case of continuous conduction mode, which can be reached with a minimum amount

of output current and a certain value of L, defined as:

$$L = V_{out} \frac{(V_{in} - V_{out})}{\Delta I_L f_{sw} V_{in}} \tag{3.11}$$

where the output voltage V_{out} is limited by the output power that the resistor R can dissipate. Therefore, $V_{out(MAX)} = \sqrt{P_{out} \cdot R}$. The same for the ΔI_L. Considering that the inductor ripple current should be greater than 20 % of the maximum output current I_{out}, the value of I_{out} is limited by the output power that the resistor can dissipate, calculated as $I_{out(MAX)} = \sqrt{\frac{P_{out}}{R}}$. f_{sw} is the switching frequency, defined at 100 kHz.

As for the output capacitor, the voltage ripple ΔV_{out} is not a relevant issue in this case and is only used to reduce signal integrity and electromagnetic interference issues. Normally, buck converters have low impedance nodes, and the principal radiation sources are generated by the high-frequency currents on small circuit loops. Therefore, the design should consider the areas of the current loops, in particular where small circuit loops with high current influence long interconnections. Figure 3.15, represents the two different current loops of a classical buck converter. The blue arrows represent the loop in on-state mode, where the MOSFET is on and the source provides current. The green arrows represent the loop in off-state mode, where the MOSFET is off and the free-wheeling diode determines the current path.

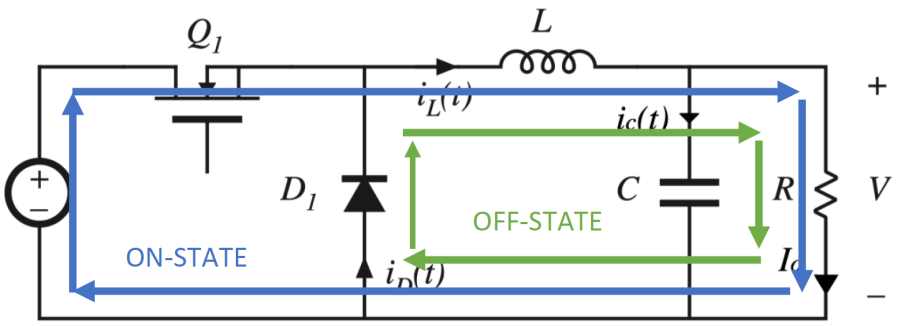


Figure 3.15: Buck converter schematic with current loop representation for EMI considerations.

The two loops share the inductance, the capacitor, and resistor components, where

the effects are summed and the high-frequency harmonics are compensated. Therefore, the critical area is the connection between the load and the MOSFET. The proposed buck-derived active load uses an R-C LPF with multiple capacitors to sensibly reduce the EMI emissions. Moreover, the input resistor helps to dissipate power with a linear relation to the input current and reduces the V_{DS} voltage of the MOS transistor with the increase of the I_{DS} current, therefore, compensating second order effects and giving more stability and control resolution to the circuit.

The proposed active load solution has been simulated with MATLAB/Simulink to evaluate the power dissipation contribution of the three resistors, and the MOSFET with the two limit cases: high voltage/low current input and low voltage/high current input. Parasitic components have been added to the model to evaluate non-ideality effects. This is useful as well to define the different values and types of input capacitors to be used. Considering the aim of the circuit, the output filter should be sized only to achieve better control on the dissipated power, which is easily reached in continuous conductive mode, and to reduce high-frequency noise. Therefore, low capacitor values have been used without reducing the output voltage and current ripple. At the same time, the output filter capacitors are normally the most stressed components in buck converters, due to the high current ratings. Therefore, thermal issues are as well reduced and higher reliability can be achieved. The duty-cycle of the PWM signal is defined with a proportional integral block with the error obtained by the difference between the input power and the required dissipated power (set-point). The simulation model is shown in figure 3.16.

Finally, the different values of the passive components have been defined, and the semiconductor devices have been chosen. The input resistor value has been defined considering the maximum allowed input current I_{in}, equal to 10 A. Therefore, with a 100 W power resistor, a resistance value of 1 Ω is necessary, based on $P_{R_{in}} = R_{in} \cdot I_{in}^2$. However, in the case of 10 A input current, the resistor must be cooled with forced air. The output resistor R has to be calculated considering that V_{out} is always lower than the input voltage V_{in}, and the desired power dissipated on the resistor should be maximized at both low and high input voltage values. Therefore, a power resistor R of 1 Ω has been chosen, with a 200 W maximum power rating. The resistor in

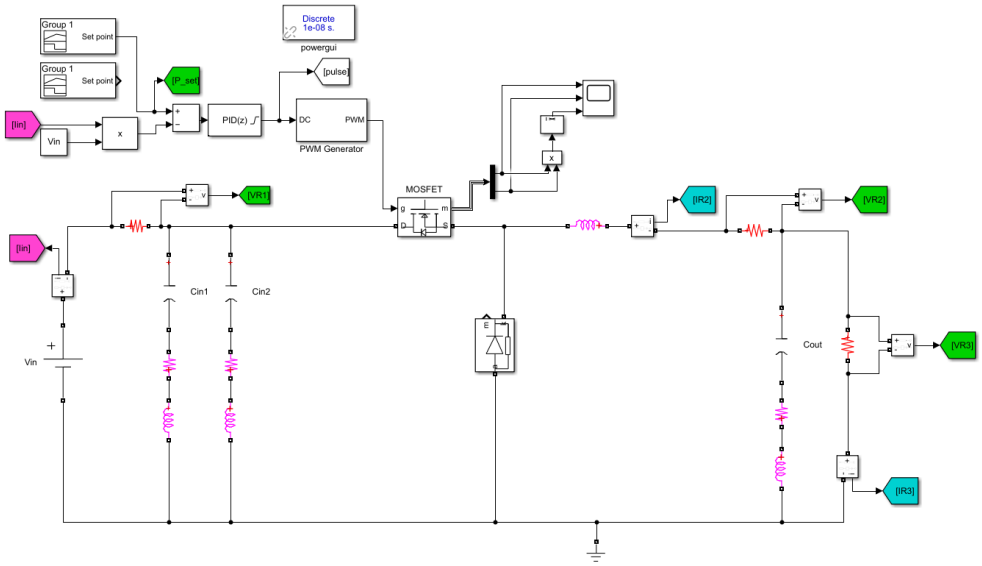


Figure 3.16: Buck-derived active load simulation model.

series to the inductor before the output voltage filter, R_L, has been used to help the power dissipation regulation with high input voltage values and low power set-point reference. In fact, in these cases, the circuit tends to work in discontinuous conduction mode, and the noise is maximized. The power resistor R_L helps to reduce high voltage variations on the output branch. Also in this case, a power resistor of 1 Ω with a 200 W maximum power rating has been chosen. Simulation results with a 48 V input voltage are shown in figure 3.17, where the total power dissipation and the distributed powers on the three resistors are shown. In this scenario, the set-point is changed every 20 ms, with the following sequence: 400 W, 100 W, 50 W, 300 W, 0 W.

Simulation results show that the reference power is set with a control response of about 2 ms, and the power absorbed by the circuit is distributed between the three power resistors.

The active load prototype has been realized with an ad-hoc Altium Designer PCB. Starting from the simulation model, a bootstrap circuit has been added for the MOSFET gate signal control. Input voltage sensing V_{in} is provided through a volt-

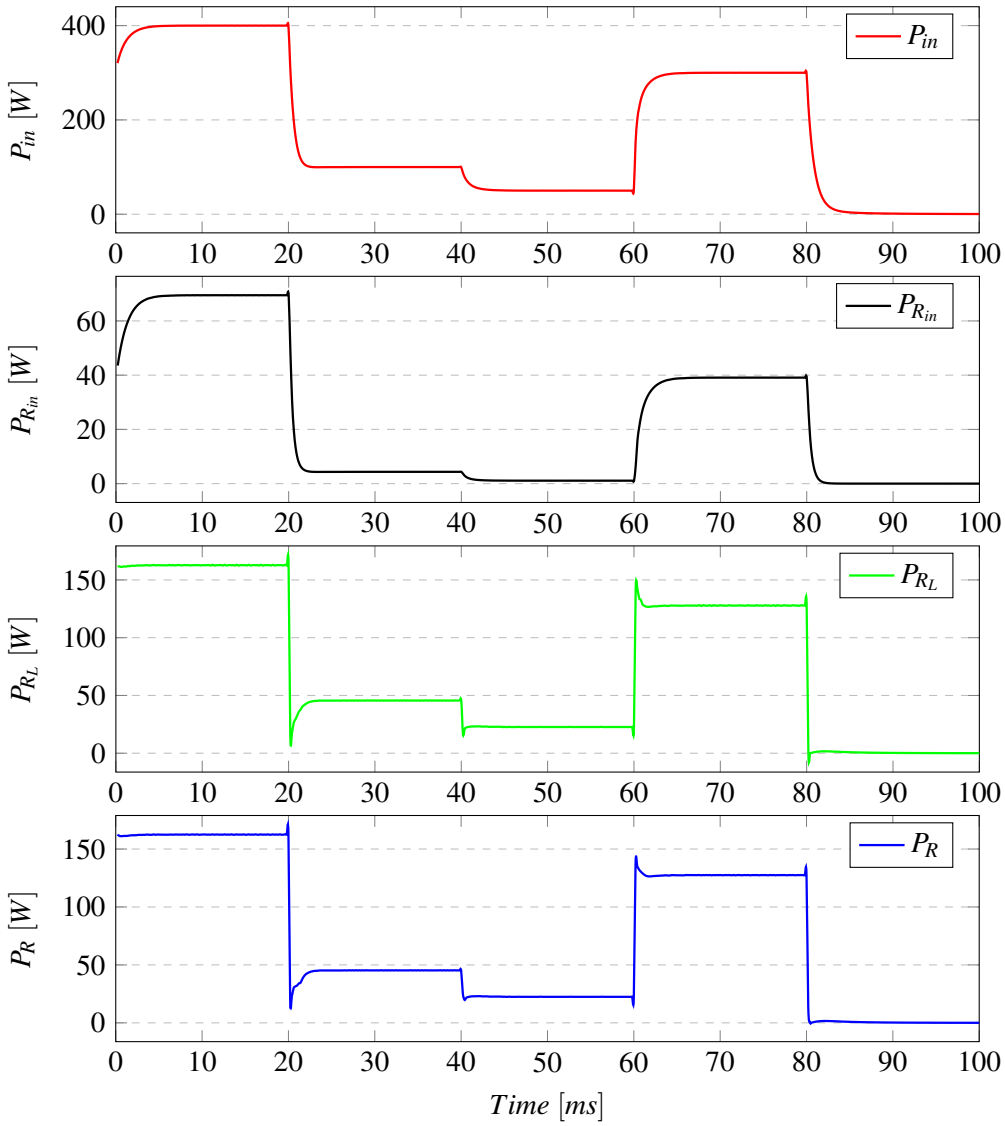


Figure 3.17: Simulation results of the buck-derived active load with V_{in} = 48 V. The figure shows the total power dissipation P_{in} (red), the input resistor power $P_{R_{in}}$ (black), the second resistor power P_{R_L} (green), the third resistor power P_R (blue).

age divider circuit. The input current sensing I_{in} circuit uses a shunt resistor and the INA240A integrated circuit of Texas Instruments for the low voltage measurement with PWM noise rejection capability. Figure 3.18, shows the 3D view of the first active load prototype layout, with the board size indications.

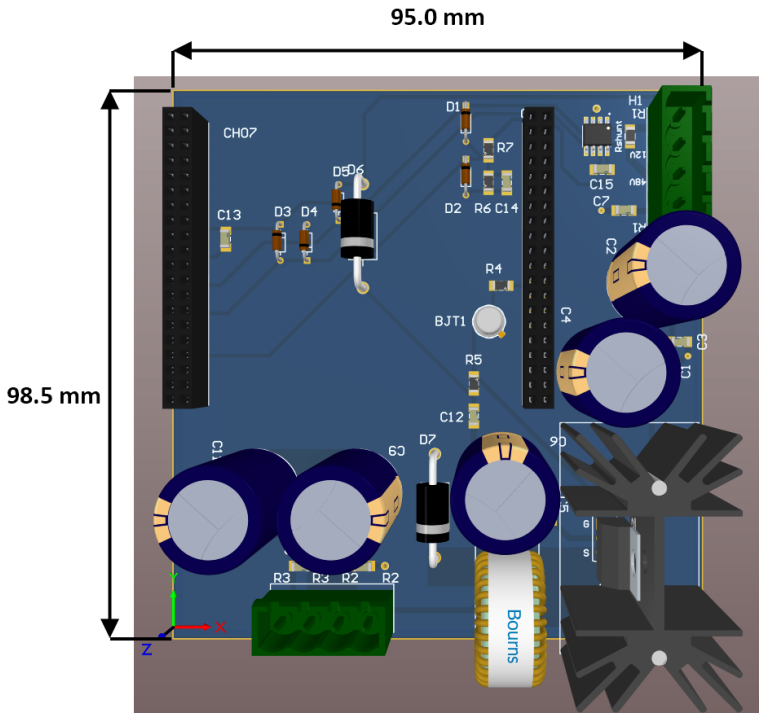


Figure 3.18: Active load first prototype layout.

The prototype has been realized and tested electrically and thermally in the laboratory with different power profiles. The simulation results have been verified and thermal results are shown in chapter 5. However, this first prototype presents an important drawback. In particular, at low input voltages such as the 12 V of a battery, the maximum power absorption considering duty-cycle equal to 100 % is defined as:

$$P_{in} = \frac{V_{in}^2}{R_1 + R_2 + R_3} = \frac{144}{3} = 48W \tag{3.12}$$

Due to these considerations, a different active load solution has been designed with a buck-boost-derived topology. The schematic circuit of this second solution is shown in figure 3.19.

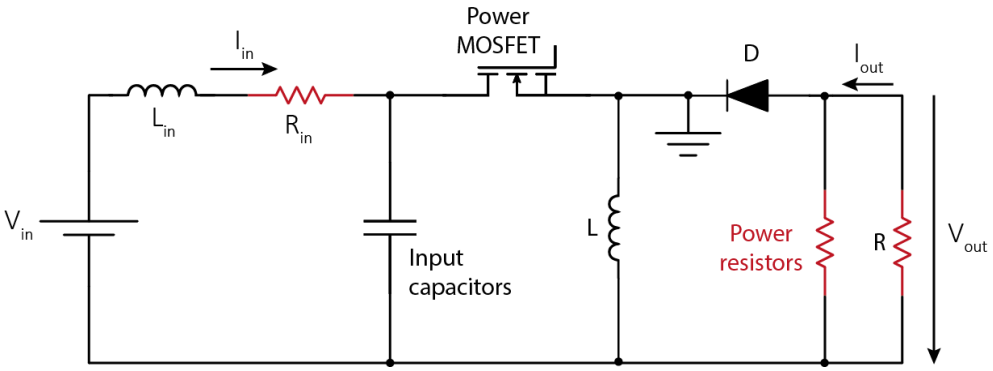


Figure 3.19: Buck-boost-derived active load schematic.

This circuit topology allows to increase the current absorption with low input voltages, by increasing the duty-cycle values. Respect to the first prototype, the grounding reference for the logic circuitry is positioned on the source of the power MOSFET. Therefore, a bootstrap circuit is not necessary. On the other side, two PCB polygon planes are necessary to provide a good connection between the ground of the input voltage, and the capacitors, inductor, and output resistors, allowing high current ratings. An input inductor has been inserted as well, allowing a smoother input current and better current sensing, which facilitates the MCU power absorption control. The power resistor values have been maintained the same as in the buck-derived topology. However, due to the voltage boost ability and the parallel of the output resistors, at low input voltages, the maximum power absorption has increased significantly. Starting from the theoretical buck-boost topology equations:

$$V_{out} = -\frac{V_{in} \cdot \rho \cdot \eta}{1-\rho} \tag{3.13}$$

$$I_{out} = -\frac{I_{in} \cdot (1-\rho)}{\rho} \tag{3.14}$$

The output power and the input absorbed power relation can be written as:

$$\frac{V_{out}}{I_{out}} = \frac{V_{in} \cdot \rho^2 \cdot \eta}{I_{in} \cdot (1-\rho)^2} \tag{3.15}$$

Considering two parallel output resistors with value R, the circuit can be modeled with the equation:

$$\frac{V_{in}}{I_{in}} = \frac{R \cdot (1-\rho)^2}{2 \cdot \rho^2 \cdot \eta} \tag{3.16}$$

Therefore, with a ρ of 0, the relation $\frac{V_{in}}{I_{in}}$ tends to be infinite, meaning the lowest power dissipated value. With a ρ that tends to 1, the power dissipated is maximized, and the relation $\frac{V_{in}}{I_{in}}$ tends to 0. In practice, non-ideal effects don't allow to increase the dissipated power over approximately 90 % of the duty-cycle. Therefore, the minimum resistance seen by the source can be written as:

$$\frac{V_{in}}{I_{in}}(min) = \frac{R \cdot 0.012}{2 \cdot \eta} \tag{3.17}$$

A drawback of this solution compared to the previous one is a reduced full-scale of the duty-cycle and higher complexity of the control. In order to maintain a fast step response to the power set-point, a control with dynamic proportional and integral constants has been defined. By decreasing the input voltage, the control parameters are increased. Vice versa, with high input voltages, control parameters values are decreased. Simulation results with an input voltage of 12 V are shown in figure 3.20. Here, the set-point is changed every 20 ms, with the following sequence: 50 W, 120 W, 20 W, 100 W, 0 W.

The simulations show a good response of the power absorbed in relation to the imposed set-point. The response time with this topology is about 10 ms.

3.2.2 Experimental Results

The active load prototypes have been tested both electrically and thermally. Both low and high input voltage conditions have been tested and the control parameters have

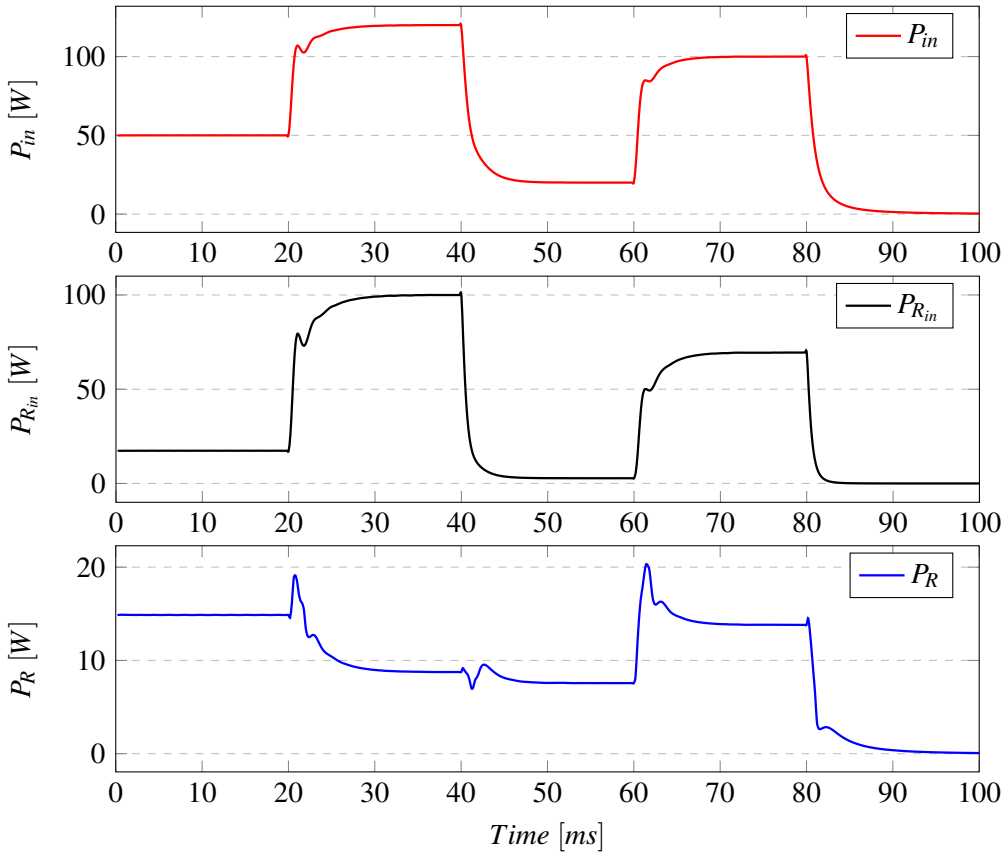


Figure 3.20: Simulation results of the buck-boost-derived active load with V_{in} = 12 V. The figure shows the total power dissipation P_{in} (red), the input resistor power $P_{R_{in}}$ (black), the power on one of the two output resistors P_R (blue).

been proved. Experimental results of the buck-boost-derived topology prototype will be shown in this subsection. The active load setup is shown in figure 3.21.

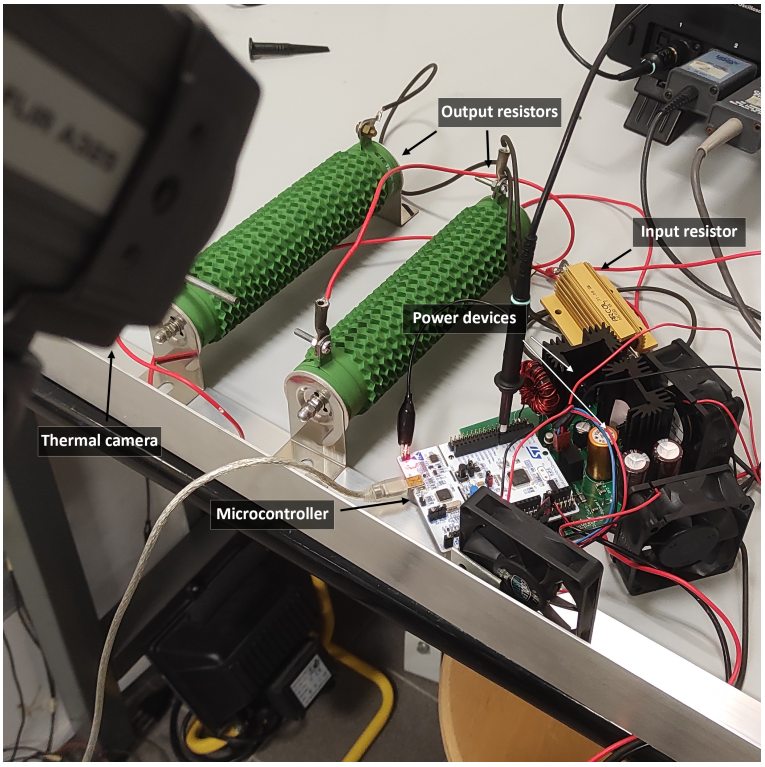


Figure 3.21: Active load test bench for experimental measurements.

A first experimental result is shown with a battery connected as the input source. The conditions can be compared with the simulation results in figure 3.20. In this case, the power dissipation of 140 W has been imposed, reaching the 10 A maximum allowed input current. Figure 3.22, shows the experimental results.

A second test has been done with a voltage generator as power source. The input voltage V_{in} has been fixed at 48 V. In this case, the power dissipation of 320 W has been imposed. This power rating has been set as a limit due to thermal issues on the power devices, as it will be shown in chapter 5 with thermal analysis. Figure 3.23, shows the experimental results.

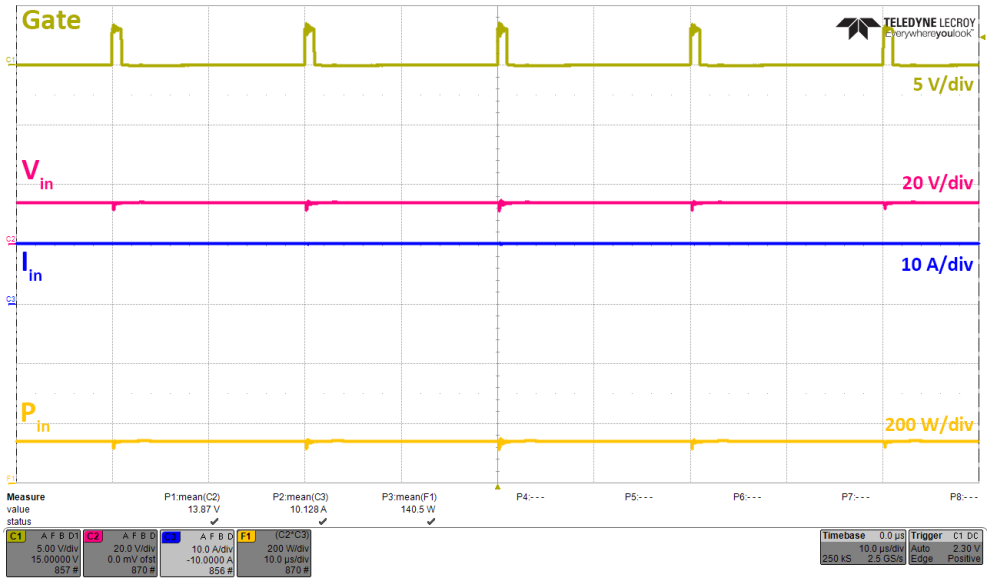


Figure 3.22: Experimental results of the buck-boost-derived active load prototype with a battery as the source. The oscilloscope capture shows the gate control signal (yellow); the input voltage V_{in} (magenta); the input current I_{in} (blue); the calculated absorbed power (orange).

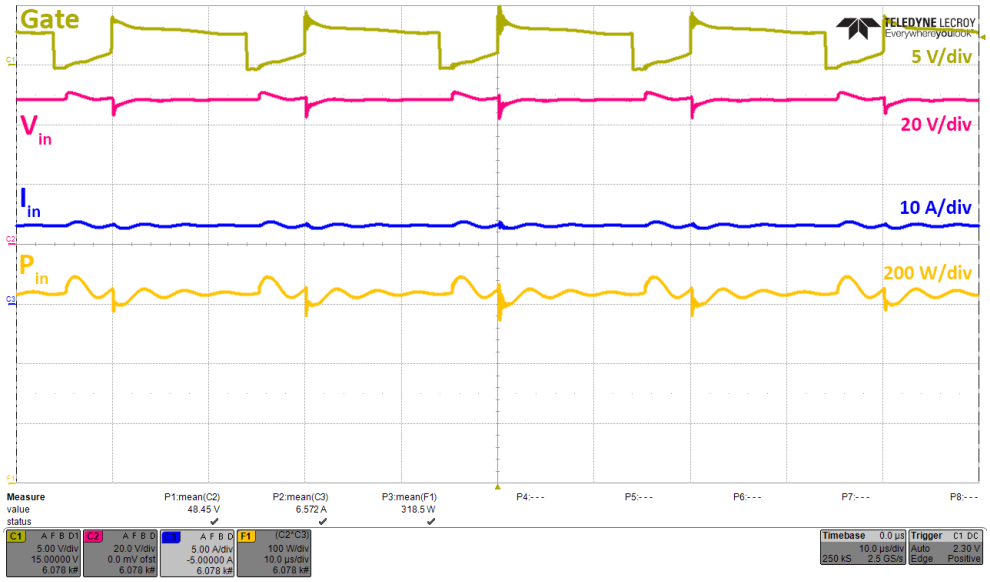


Figure 3.23: Experimental results of the buck-boost-derived active load prototype with a voltage generator (V_{in} = 48 V) as the source. The oscilloscope capture shows the gate control signal (yellow); the input voltage V_{in} (magenta); the input current I_{in} (blue); the calculated absorbed power (orange).

Chapter 4

PV Modules Soiling Monitoring

NG DC architectures are promising compared to AC ones for the improvement of features like flexibility, controllability size, efficiency, and self-sufficiency [3]. However, many problems have to be solved to allow major implementation, e.g. in buildings. Monitoring systems and the applications for automated maintenance still need research activity. Related policies have to be determined in order to improve power production, and reduce costs and waste.

In this chapter, solar PV module monitoring and cleaning will be discussed. The cleaning of PV arrays has to be managed in relation to the installation site and meteorological conditions [74, 75].

In figure 4.1, the proposed NG architecture with a focus on the PV array monitoring system is shown.

In [76], the PV module performance impacts of the shadow due to deposited dust have been analyzed. Different energy losses can be found, starting from the reduced irradiance, but also thermal conditioning of the cells. Finally, the meteorological condition contributes to dust deposition and removal. Among the main influences of the deposition of dust or dirt, there are the material properties such as dimensions, compositions, forms, weights, and also the site environment and cells inclination angle. Therefore, different types and severities of shading can occur, which can affect the production of current or, in the case of strong shading, the voltage values can also

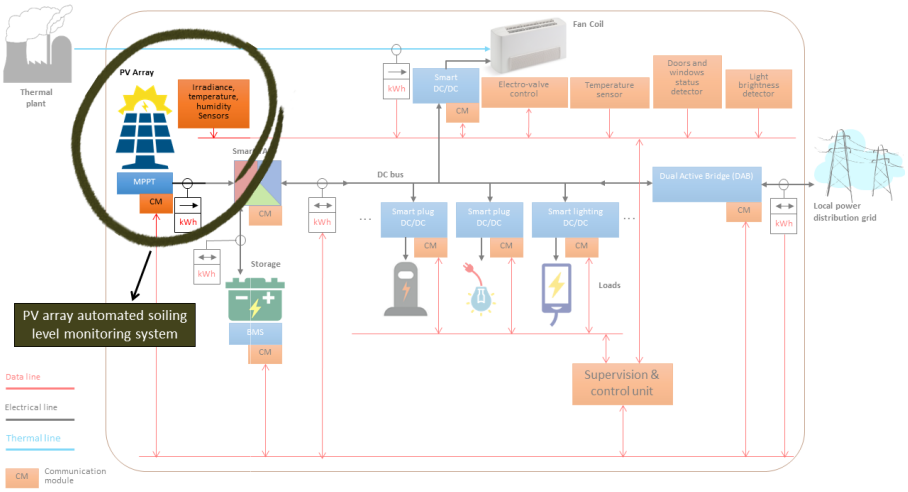


Figure 4.1: Proposed NG with a focus on PV array monitoring system.

drop.

In [77], a collection and analysis of the published scientific papers on PV superficial dust accumulation have been carried out. Two categories of analysis types have been defined: electrical-based performance studies, and optical-based ones. An interesting proposal of the authors consists in the definition of a photovoltaic soiling index (PVSI), to be included in datasheets, to define maximum soiling ratings of a specific module to work reasonably.

In [78], the I-V characteristic changes of the PV modules have been analyzed under different soiling conditions. Tests are carried out both indoor and outdoor, with two identical PV modules at the same place, one kept clean, and one with deposited dust. Results show how the soiling conditions have the main impact on short circuit current, while the voltage isn't strongly influenced. Moreover, temperature increases with higher soiling conditions, leading to lower power performances.

Quantifying the power losses due to dust deposition has been studied in [79]. An irradiance reduction estimation has been defined by considering clean and dirt modules. Results show how the irradiance incident angle increases up to 75° degrees,

leading to higher irradiance losses. Over this maximum angle value, the losses decrease. This is due to the diffused irradiance, which has a higher influence on dirt modules.

In [80], an image processing technique has been proposed to analyze the soiling level of PV modules. The technique is based on a comparison between an acquired picture with a library of pictures with different soiling levels and brightness. A decision making algorithm shows the non-uniformity and critical soiling levels in order to request maintenance.

In this section, an automated system is considered to allow the monitoring of the soiling level on the front glass of solar PV modules. Two techniques are combined to quantify the soiling level, and classify it based on the type and covered area, namely, optical inspection and I-V curve analysis. Typically, ordinary procedures on scheduled days are proposed for the PV array cleaning. Otherwise, power plant losses are monitored to organize the cleaning procedures. However, the causes for loss variations are not considered in these cases, meaning that the maintenance of PV arrays may be wasteful and unnecessary cleaning can occur. Therefore, automatic procedures and targeted interventions can be cost-effectiveness due to a trade-off between cleaning costs and power losses. The proposed system uses a soiling sensor, that allows the detection of dust deposition, concentrated dirt, or malfunctions. Moreover, smart data management is necessary and a predictive technique should be included based on actual and historical data, and weather forecasts [81, 82]. Therefore, it can be decided when and what kind of cleaning is required.

4.1 Nanogrid Model with Soiling Evaluation

In figure 4.2, the MATLAB/Simulink model of a DC nanogrid is shown.

This model has the aim to manage the energy flow among solar PV modules, a battery, and DC loads of an office powered by a PV plant. A dust soiling parameter has been added to the model to evaluate PV power generation losses. For this purpose, a Soiling Factor (SF) is determined, affecting the power output of a PV array. The SF

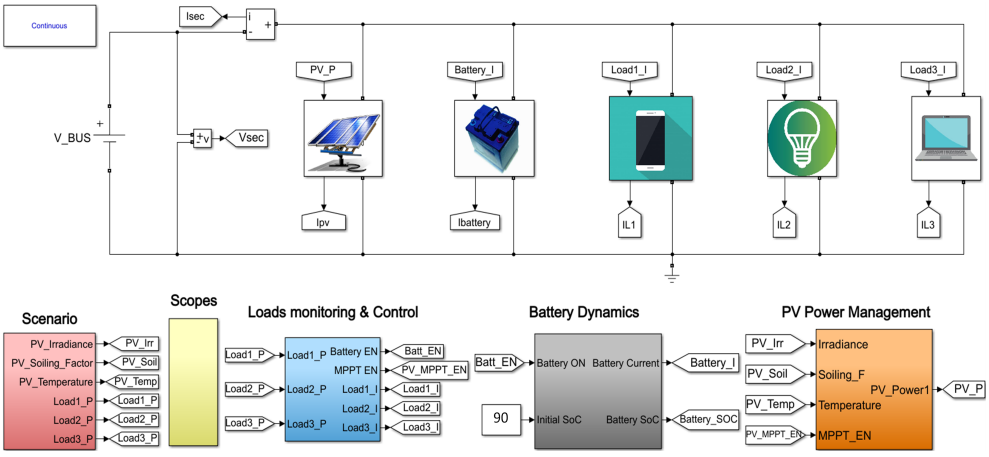


Figure 4.2: DC nanogrid MATLAB/Simulink model for dust soiling effect simulation analysis.

considers the following mathematical model [83]:

$$PV'_{Irr} = PV_{Soil} \cdot PV_{Irr} \tag{4.1}$$

where PV_{Irr} is the irradiance measured by the irradiance sensor, PV_{Soil} is the current SF, and PV'_{Irr} is the resulting effective irradiance on the solar PV modules. The SF PV_{Soil} can be calculated from:

$$PV_{Soil} = \frac{V_{oc}}{V_{oc\_ref}} \tag{4.2}$$

where V_{oc} is the current open circuit voltage, and V_{oc_ref} is the open circuit voltage of a reference module kept clean.

The simulation considers the energy consumption of typical loads, such as lamps, laptops, and smartphones. These loads are modeled by current sources in series with resistors. The scenario subsystem represents the load profiles. V_{bus} is fixed at 48 V by an ideal voltage source. As for the solar PV plant, irradiance in combination with temperature and SF data are used as input of an MPPT block in the PV Power Management subsystem. PV current is then defined by the PV power divided by the bus

voltage and applied to a dependent current source. The current delivered or absorbed by the battery is calculated in the Battery Dynamics subsystem, which models the charge and discharge profiles. SoC is displayed and in case of full load, MPPT is switched off to avoid battery overcharging. The Loads Monitoring & Control subsystem uses the load consumption values and the SoC to define whether the battery charge and MPPT should be enabled. Details of the PV Power Management subsystem are shown in figure 4.3.

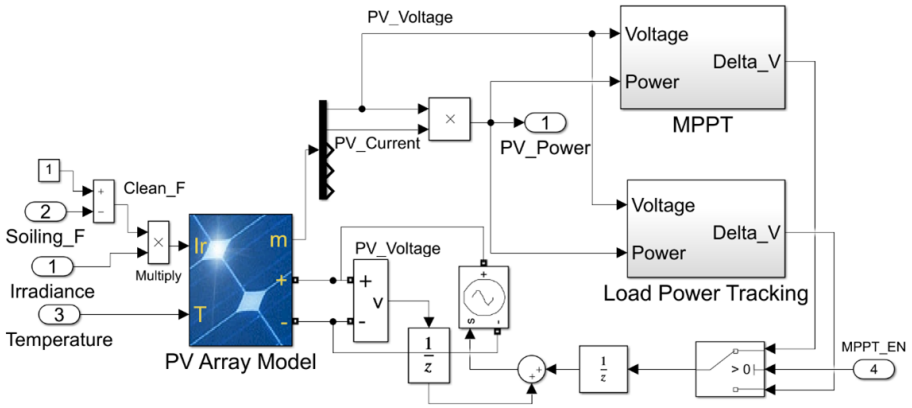


Figure 4.3: PV Power Management subsystem with MPPT and power demand control.

Two different control strategies have been implemented, namely MPPT, and Load Power Tracking (LPT). Depending on the MPPT enabling signal, one of the two strategies is used to adjust the stimulus delta_V. MPPT uses a perturb and observe algorithm, considering PV voltage and PV power values. The LPT algorithm defines the stimulus delta_V following the load required power. LPT is activated when the battery is fully charged. The effective irradiance used by the PV array model is obtained by the multiplication of the irradiance with the cleanness factor ($Clean\_F$), which is calculated as:

$$Clean\_F = (1 - PV_{Soil}) \tag{4.3}$$

Therefore, the effect of the dust deposition is modeled as a reduction of the ir-

radiance. A simulation result of the model with three different scenarios is shown in figure 4.4. In the first case, the SF PV_{Soil} is 0 %, supposing completely clean PV modules. In the second case, a 10 % SF is applied. Finally, in the third case, a 30 % SF is applied. The irradiance profile is kept equal in all the simulation cases.

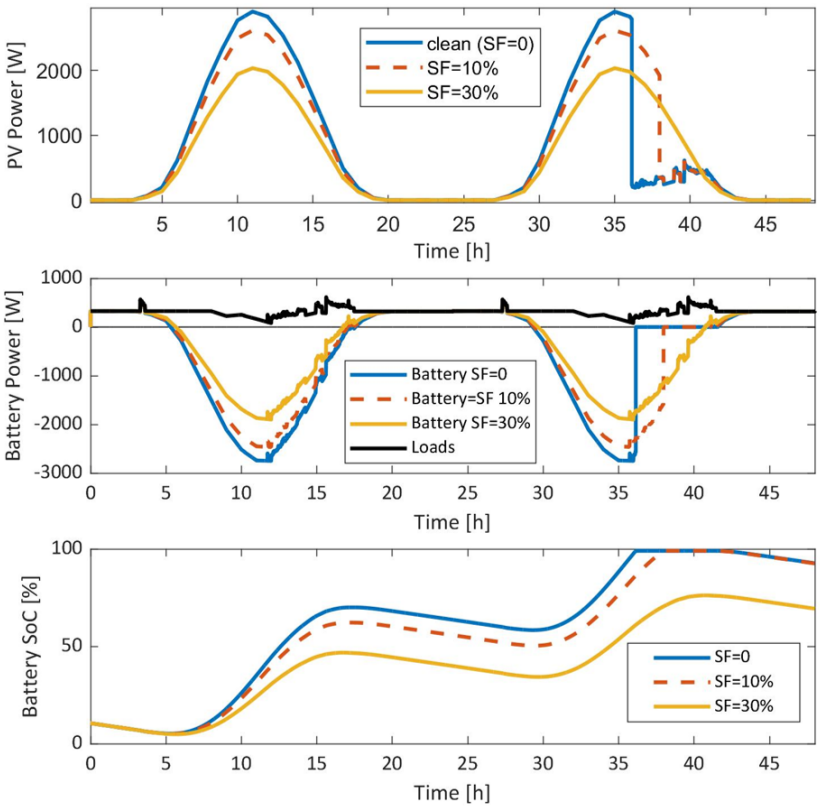


Figure 4.4: Simulated power profiles and SoC of the battery during two days: June 21-22 in Parma (Italy), with a mono-crystalline PV array of 3 kWp, Azimuth = 0°, Slope = 30°. First case (blue): SF = 0 %; second case (red - dotted): SF = 10 %; third case (yellow): SF = 30 %.

Considering the boundary conditions, in the first simulated scenario, the MPPT algorithm is disabled at approximately 35 h working time, and the LPT is enabled.

In the second case, the algorithm changes at approximately 37 h. While in the third case, MPPT is applied during the hole 48 h simulated time, due to the battery SoC never reaching the fully charged value.

The simulation results show the effects of the solar PV soiling in a simple defined DC NG. However, the determination of the SF is not an easy task. A proper sensor has been defined and is described in the following section.

4.2 Soiling Sensor

The soiling sensor aims to evaluate the type and distribution of dust or dirt on PV modules. The concept combines two techniques, namely, I-V curve analysis [84] and optical inspection [84, 85]. In the proposed NG architecture, the sensor is connected in parallel to the PV modules and works whenever the TAB disables the PV port due to low power production. In this case, the sensor extracts the I-V curves, which are analyzed and compared to the irradiance value, to understand if there is dust deposited, dirt, or cells malfunctions. Figure 4.5, shows the block diagram of the soiling sensor system.

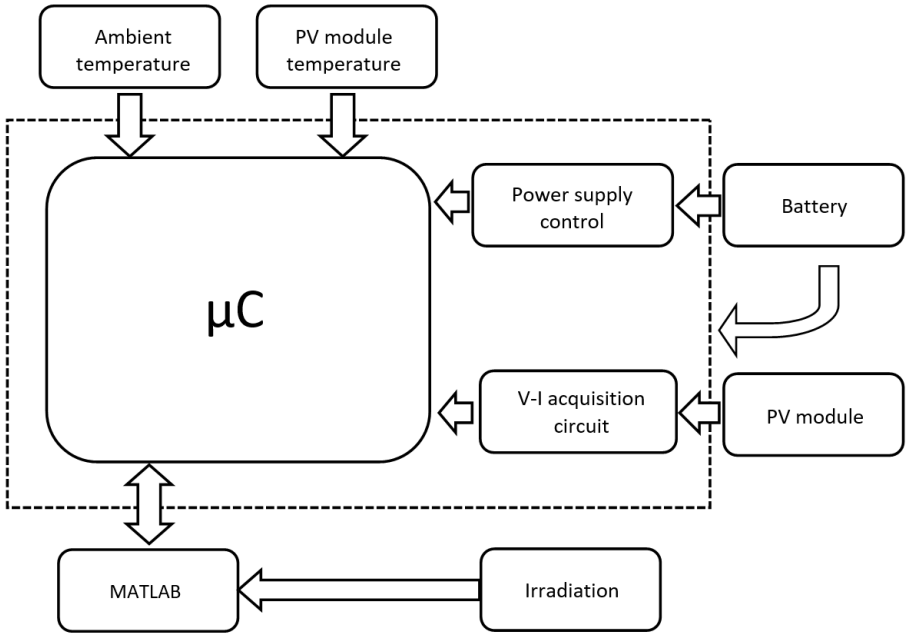


Figure 4.5: Block diagram of the soiling sensor system setup.

The V-I acquisition circuit is designed with a power MOSFET as active load and controlled by a microcontroller (μC) to modulate the voltage and current of the PV modules. The bias voltage of the MOSFET gate is the output of a filtered PWM waveform. The duty-cycle of the PWM signal, conditioned with a LPF, determines

the gate voltage and varies from below threshold to a fully-on MOSFET (V_{GATE} = 12 V). The I-V curve is therefore slightly limited on the short circuit I_{SC} value, due to the MOSFET R_{on} resistance. In figure 4.6, the schematic diagram of the I-V curve acquisition circuit is shown.

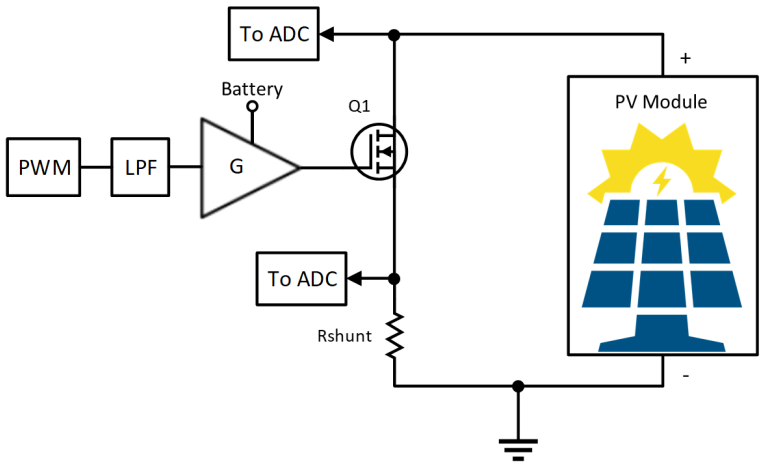


Figure 4.6: Schematic of the I-V curve acquisition circuit.

The STMicroelectronics NUCLEO-F446RE board has been used, with the relative MCU, TIMER, and ADC peripherals. The PWM filtering circuit has been designed with an active LPF. The TIMER peripheral uses a 100 MHz clock, generated by an external quartz of 20 MHz, which signal has been accordingly conditioned (frequency multipliers). The counter period has been set to 2000, meaning that the PWM frequency has a value of 50 kHz. Therefore, the cutoff frequency of the LPF has been defined with the value of 100 Hz, with a resistor of 10 kΩ and a capacitor of 1 μF. For this purpose, the operation amplifier NCS2333 of ON Semiconductor has been used, with a non-inverting circuit topology.

Considering the 3.3 V maximum output voltage value of the MCU, the output of the LPF with a duty-cycle of the PWM from 0 to 100 %, will be from 0 V to 3.3 V. The resolution of the duty-cycle is determined by dividing the 3.3 V scale over the 2000 counter steps, therefore a 1.65 mV minimum step resolution can be obtained. The

filtered signal is then amplified by a bipolar transistor. The BJT is connected in a pull-down configuration, supplied by the battery (12 V), to drive the MOSFET gate from 0 V to 12 V. Therefore, with a duty-cycle value of 100 %, the MOSFET is turned-off, and with a duty-cycle value of 0, the MOSFET gate is polarized with a 12 V voltage. The acquisitions have been taken controlling the MOSFET by changing the PWMs duty-cycle from 100 % (off state) to 0 (fully-on state), due to the higher rise-time respect to the fall-time of the MOSFET. After each acquisition, the duty-cycle changes with a dynamic step, strictly related to the difference between the current I_{PV} last acquired value and the present one. In this way, more samples are taken during the I-V characteristic knee than near the open circuit voltage or short circuit current values. The algorithm of the I-V acquisition software is represented in figure 4.7.

Voltage sensing has been designed with a resistor divider circuit, while current sensing uses shunt resistors. Both circuits are connected to NCS2333 operation amplifiers with a differential amplification topology, which outputs are connected to the NUCLEO ADC inputs. The ADC peripheral works triggered by a second TIMER, synchronous to the first one for the PWM generation. The acquisition frequency of this TIMER is set to 10 kHz. Interactions between the ADC and the CPU are managed through the Direct Memory Access (DMA) so that the CPU doesn't saturate by the many data memorization operations. All the acquired data, at the end of a I-V curve acquisition, are saved in a dedicated file that can be opened by MATLAB. This method allows a very rapid acquisition, below 200 ms, which increases the likelihood that the values of irradiance and temperature will not change during acquisition. The sensor is equipped with a 12 V battery as a power supply. This allows major flexibility and autonomy to the system in case of an off-grid acquisition. A simple software control is provided as well to monitor the battery status, and a switch is inserted on the board to recharge the battery directly from the PV modules in case of a low battery. However, if the system is related to the TAB, the same 12 V power supply can be used for all the logic circuitry. The I-V acquisition board prototype is shown in figure 4.8.

In order to add a dirt classification, the soiling sensor uses an image processing technique performed by an ad-hoc MATLAB script. A mask has been defined on the

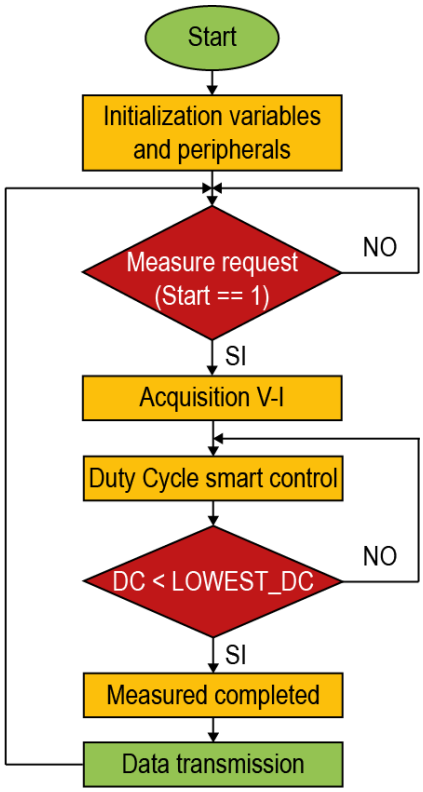


Figure 4.7: I-V acquisition algorithm.

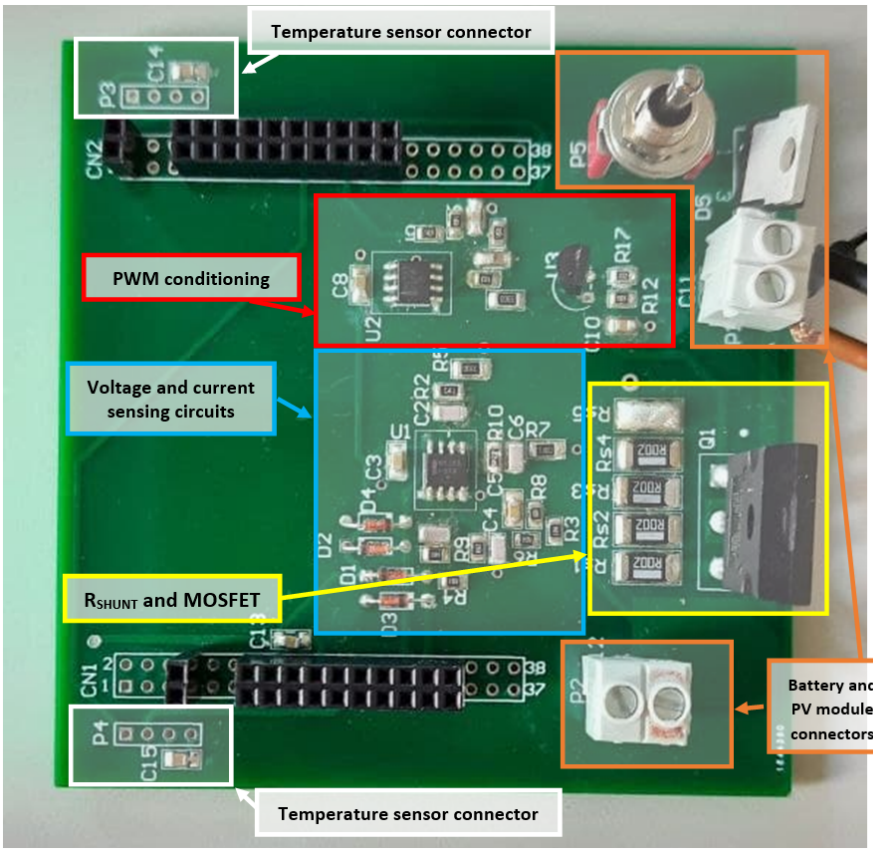


Figure 4.8: I-V curve and temperatures acquisition board.

PV modules and used for the original image frame removal. Then, the photographic images are processed only on the working PV area, starting from a clean PV picture as a reference. Each photo is scaled and centered for the area analysis. Red paper square references on the corners of the module help to crop and shape the image. The perspective effect is adjusted starting from the reference papers with a geometric transformation. The picture is then binarized, where black color indicated the PV module, and white the deposited materials. A MATLAB pixel analysis determines the area covered by heavy dust. This one is divided by the total working area and used to compute the fraction of the dusty area. Figure 4.9, shows the image processing workflow.

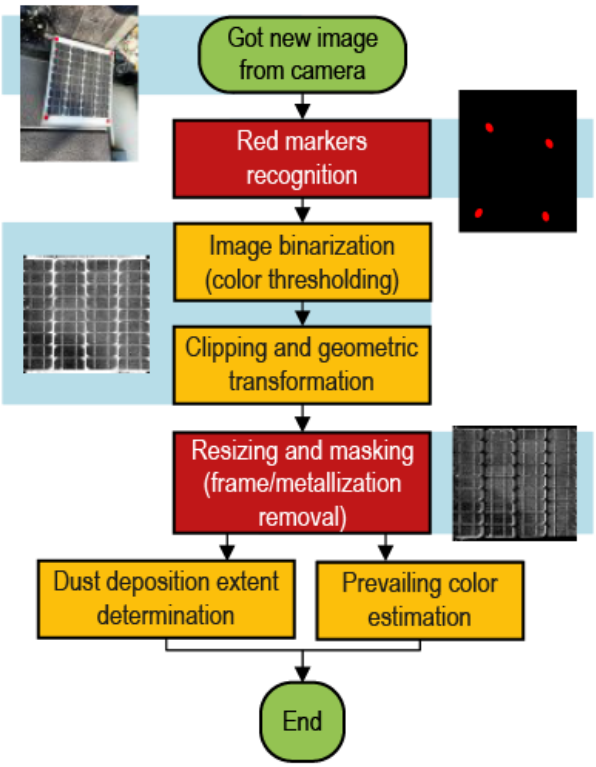


Figure 4.9: Flow-chart of the image processing.

Two small solar PV modules have been used to test the soiling sensor and the ad-hoc designed acquisition board. Tests have been carried out with the deposition of dust measured with a precision (1 mg) scale. Dry soil has been collected, sieved (0.5 mm maximum diameter holes), and weighted to obtain the desired dust. Different I-V curves are then acquired for two selected modules: a thin-film and a mono-crystalline silicon module. The thin-film ICO-SPT-40W module has a 24 V open-circuit voltage (V_{OC}) and 2.88 A short-circuit current (I_{SC}). The monocrystalline silicon 25 W S.E. Project SEM25M/12 module has a V_{OC} equal to 21.3 V and a I_{SC} equal to 1.6 A. The PV modules were located both in horizontal or 28°-tilted (Azimuth = 0°) positions. Starting with the clean condition (used as a reference), the amount of dust is gradually increased on the front glass. Irradiance and temperature have been monitored during the acquisitions, and photos of the modules have been taken for the covered area analysis, then correlated with the corresponding I-V curves. Figure 4.10, shows the test bench setup.

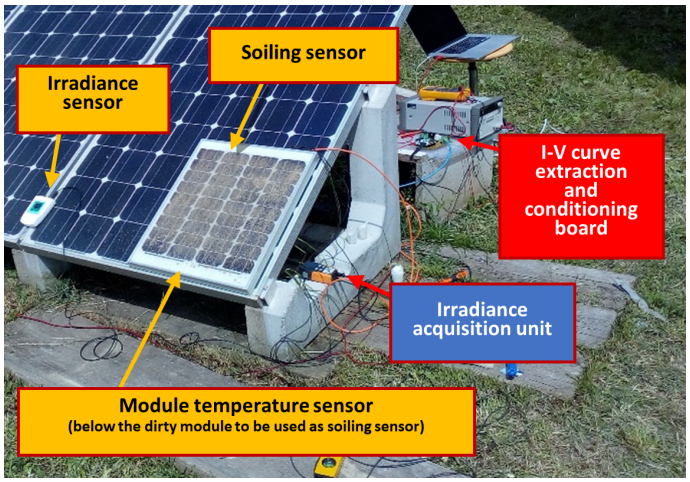
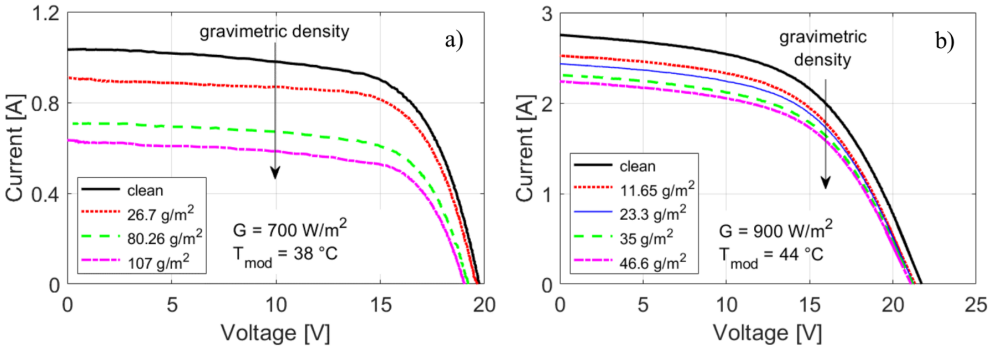


Figure 4.10: Test bench setup of the soiling sensor.

Tests with a thin-film module have been carried out with 900 W/m^2, while during the tests with the monocrystalline module, a 700 W/m^2 irradiance value has been measured. In both cases, different amounts of dust were deposited uniformly. The



(a) ICO-SPT (b) SEM25

Figure 4.11: I-V characteristics measured in the horizontal position. Tests with thin-film ICO-SPT (a) at 900 W/m^2 irradiance; monocrystalline SEM25 (b) at 700 W/m^2 irradiance.

experimental results with the I-V characteristics are shown in figure 4.11.

Starting from the voltage and current values depending on the different gravimetric dust densities, the measured normalized maximum power can be extracted. The experimental results are shown in 4.12. Tests have been carried out with as equal as possible irradiance and temperature conditions.

The results allow some considerations between maximum power point depending on the gravimetric density. For the thin-film solar PV module, a linear slope of around $1.9 \cdot 10^{-3}$ $(g/m^2)^{-1}$ is obtained. Therefore, nearly 9% losses have been measured with the maximum gravimetric density of 46.6 g/m^2 applied in the tests. A fairly linear dependence, with a slightly gentler slope of $1.7 \cdot 10^{-3}$ $(g/m^2)^{-1}$, was found also for the monocrystalline silicon module. In this case, nearly 18 % losses with the maximum gravimetric density applied in the tests of 107 g/m^2.

The image processing technique has been tested with different dust depositions. In one case, a uniform soiled PV moduled is compared with the case of a non-uniform dust deposited PV module. Figure 4.13, shows both the thin-film PV module with 5 g non-uniform dust deposition and the monocrystalline silicon PV module with 20 g uniform dust.

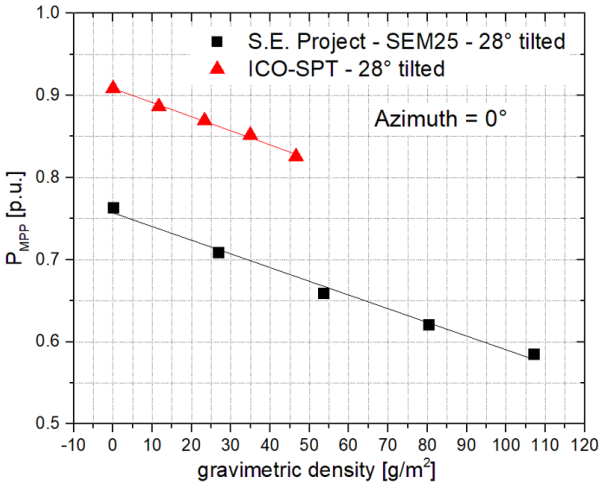
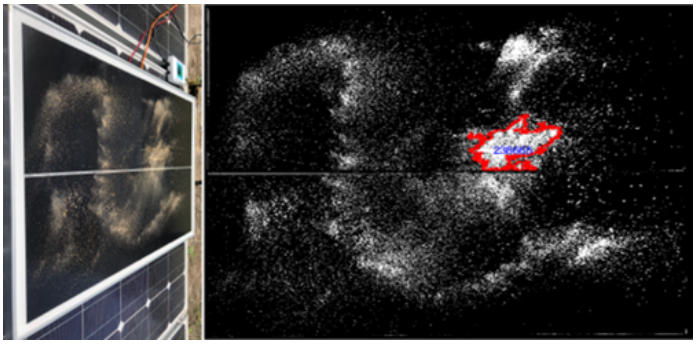


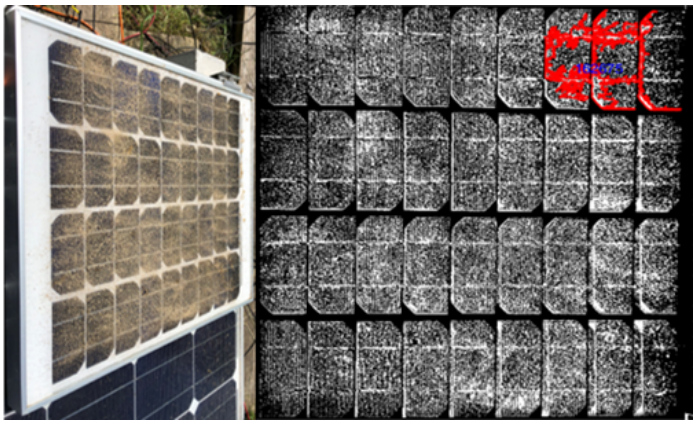
Figure 4.12: Normalized measured maximum power vs gravimetric dust density with an irradiance of approximately 1000 W/m^2, and a PV module temperature of approximately 40° C.

The combination of the two electrical and optical techniques enables a good evaluation of the quantity and quality of the PV module soiling. Therefore, an adequate cleaning strategy can be implemented with the use of information obtained by the soiling sensor. However, as far as soiling is concerned, some environments (e.g., desert zones) are more critical than others. PV module cleaning is more often necessary because dust can severely reduce the output. Unless, dust deposition is a slow process and self-cleaning occurs on PV modules thanks to the rain, the front glass properties, and the PV modules tilt (typically > 10°).

Experimental results have been carried out on small PV modules. The soiling sensor applied to the proposed NG architecture could obtain major reliability due to greater area evaluation of the PV modules. Moreover, the data processing function plays a very important role. Meteorological data, irradiance, temperature, historical electrical, and soiling sensor output have all to be taken into consideration before programming a solar PV array cleaning session. In the case of smart NG, supervision, and monitoring are mandatory, and these data have to be managed considering the



(a) Non-uniform dust deposition: the estimated covered area is 10 % of the whole active area.



(b) Uniform dust deposition: the estimated covered area is 36 % of the whole active area.

Figure 4.13: (left) image taken by the camera; (right) MATLAB processed image.

whole system working conditions. More details of this work can be found in [A3, A6].

Chapter 5

Thermal Management

The NG devices, such as the Smart Plugs and the TAB, work with high power density rates, due to the space requirements. Therefore, natural air convection is a strict constraint. Circuits should be provided with specific electrical and thermal protection, and control based on temperature sensing can be included to avoid failures. Thermal management considerations have to be done during the device design phases. For high power density circuits, thermal behavior is a critical reliability issue for the board design, and FEM analysis could be used to model the different components. Higher temperatures not only affect electrical behavior but also reduce the lifetime of the devices.

For the board design, literature research helps to define the device characteristics in relation to the temperature, as well as their technological processes. Then, measurements on simple test circuits can be used to fit FE models, used to simulate the devices under different conditions. In this chapter, thermal analysis are described on discrete GaN FETs, capacitors, and the PCB prototypes of the NG devices. However, the proposed thermal analyses method can be used as well for inductors, transformers, or for the design of cold plates.

Physical modeling in power electronic devices, such as the GaN transistors, is of interest due to the complexity and thermal characteristics of commercially available devices [86, 87]. The increase in power density requires a good thermal manage-

ment design. Typically, the thermal components are over-sized due to the lack of information about the structure and thermal behavior of the devices [88]. However, materials and space could be wasted. Working with FEM simulations helps to reduce the over-sizing design of heat spreading solutions. GaN FETs near chip scale package available on the market allows a vertical thermal flow [89]. The layout optimization needs a trade-off between electrical improvements, such as reducing the interconnection copper pads and traces, and thermal ones, such as increasing the copper area. FEM simulations help to find this trade-off, without the need for multiples prototypes, saving time and costs. Verification and validation simulation steps are introduced as well to evaluate the error parameters and provide improved accuracy of the FEM solutions. The method applied for FEM analysis is shown in figure 5.1.

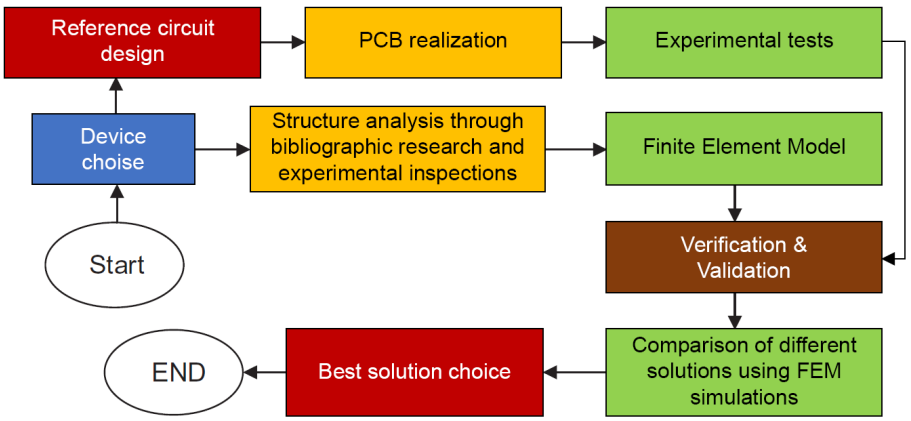


Figure 5.1: FEM modeling workflow for the thermal design optimization.

This method allows to improve the board layout and highlights the critical parameters. Once the device has been defined, information about geometries, materials, and physical properties are needed for the model. For this purpose, datasheets, literature research, but also direct inspections can be done. However, not always is reasonable to design and simulate the entire 3D model. As for the case of capacitors, simulating a large number of thin layers leads to huge numbers of degrees of freedom in FEM analysis. Therefore, simplification must be made and approximation should be val-

idated in order to have acceptable errors in the simulation results. For this purpose, a reference circuit has to be defined. In this work, in relation to the device studied, different benchmark circuit has been realized. Measurements have been used for both fitting and validation purposes.

Finally, once the model has been validated, equivalent Foster thermal networks can be extracted through the FEM analysis. Then, the thermal step response can be evaluated on the analyzed devices or circuits. The point at maximum temperature has to be considered, and the thermal network can be extracted with previously validated methods [90]. In figure 5.2, the FEM analysis workflow method with transient analysis is shown.

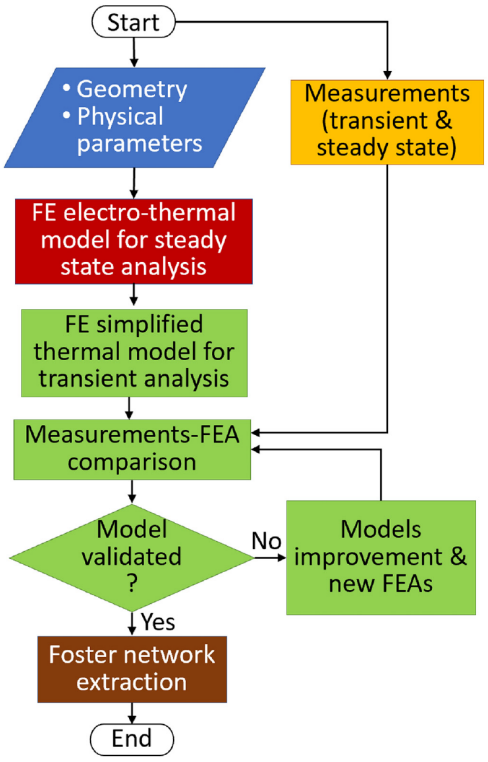


Figure 5.2: FEM modeling workflow for the thermal design optimization with transient analysis.

In figure 5.3, the elements and prototype boards of the proposed NG architecture on which a thermal analysis has been carried out are shown.

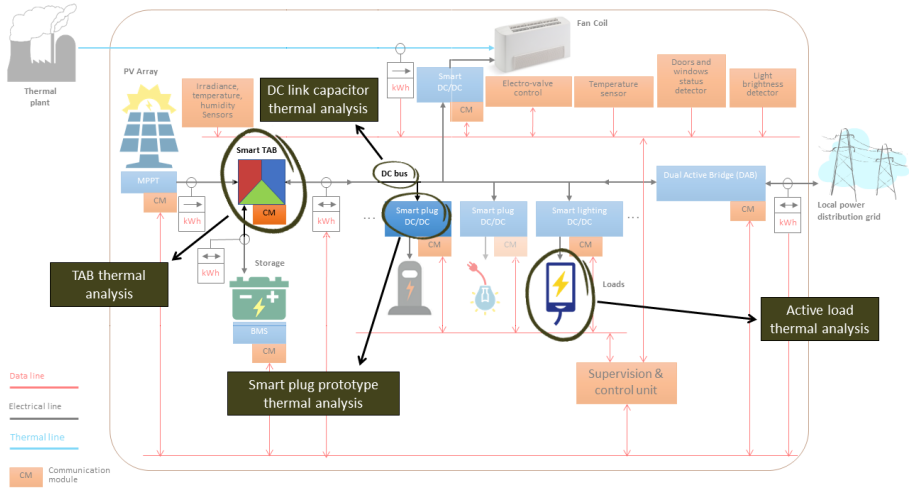


Figure 5.3: Proposed NG with a focus on the element and prototype boards on which thermal analysis has been carried out.

5.1 Power GaN FET Boards Thermal Optimization

Due to the promising electrical and thermal features, the GaN Systems GS61004B has been taken into analysis. Electrical characteristics of the transistor are: $V_{ds(MAX)}$ = 100 V, $I_{ds(MAX)}$ = 38 A, $R_{ds(on)}$ = 16 mΩ. This transistor uses a package solution design, called GaNPX, for improved thermal performance keeping low the parasitic inductance [91]. The transistor top and bottom views are shown in figure 5.4.

The choice of the transistor is due to the NG application requirements, thus low voltage high current ratings. The geometry has been defined through bibliographic research. In [91], the embedded GaNPX packaging is shown with a cross-section and exploded view of the product. Moreover, an inspection of the device has been carried out. Starting from the top layer, the device has been studied layer by layer

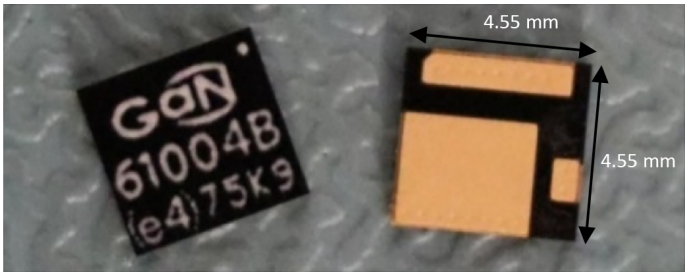


Figure 5.4: Two GaN Systems GS61004B: top view (left); bottom view (right).

to obtain multiple planar views. The GS61004B transistor consists of three bottom pads, with different areas starting from the huge source pad, a smaller drain pad, and a small gate pad. Cylindrical copper connectors allow contacting the pads to metallic dedicated layers. These are then connected to the thin GaN layer on the top, where the device is working with the horizontal concept. The GaN layer is attached to a Si bigger layer, which bulk is connected directly to the source pad. Figure 5.5, shows an exploded view of the geometry, where the source and drain copper pads have the most important role in thermal dissipation.

5.1.1 Experimental Test Bench

For the model verification and validation, a simple PCB reference circuit has been designed. The manual assembly has been reduced to the minimum possible devices and connections to avoid reliability issues related to soldering. The simple PCB structure helps as well to design an equivalent 3D geometry to be simulated with a good fitting to the measurement and to verify the different parameters more easily. In figure 5.6, the PCB is shown with the soldered GS61004B GaN transistor.

Particular attention during thermal acquisition has been paid to the board emission coefficient, in order to avoid incorrect readings. For this purpose, a transparent matt has been painted on the board and the infrared camera has been positioned at a distance of around 30 cm from the circuit.

For simplicity, a DC biasing of the FET has been chosen, with a 10 Ω resistor on the power loop, used both as load and shunt resistance. For the gate resistance,

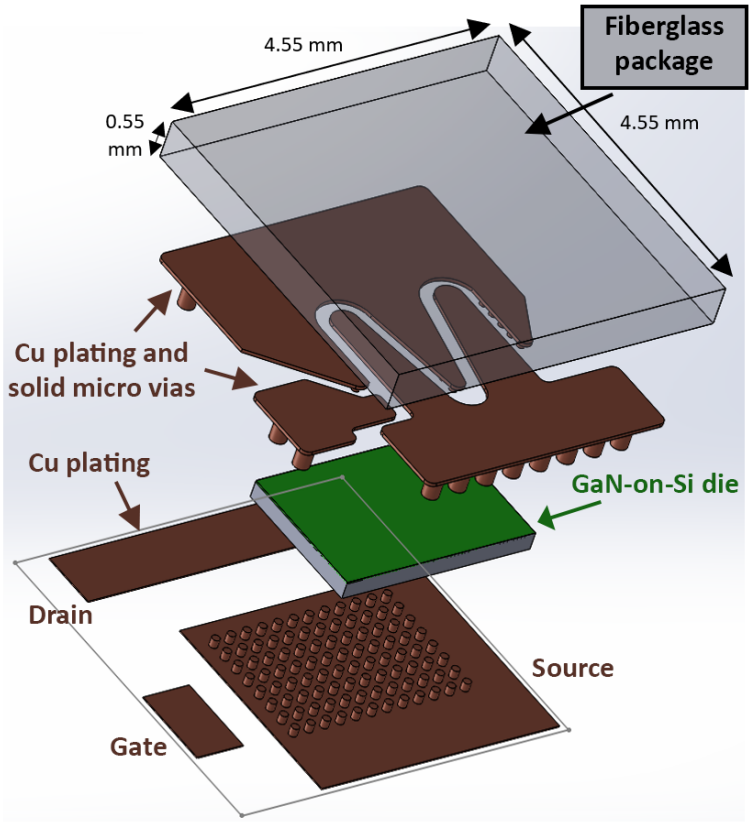


Figure 5.5: GaNPX package structure: 3D geometry with exploded view.

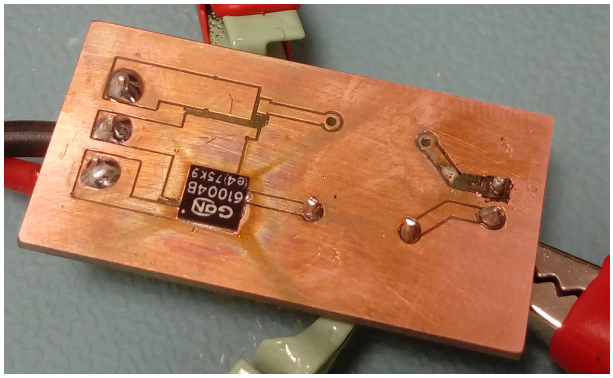


Figure 5.6: PCB for model verification. An optically transparent matt paint with a know emission coefficient ($\varepsilon = 0.96$) is used to cover the PCB and avoid light emission issues.

a value of 810 Ω has been chosen. This value limits the device dynamic behavior of the GaN device, limiting how quickly the capacitance of the FET can be charged or discharged. Considering that for isolating the gate, oxide growth is not an option with GaN, the gate leakage current of GaN transistors is higher than that of silicon MOSFETs. Therefore, a gate leakage current on the order of 1 mA is expected, and a voltage drop on the resistor of approximately 820 mV is expected. Two ammeters have been used, one for the drain current, and one for the biasing gate current. Considering the fixed voltages, the total power dissipated by the FET can be evaluated with both the gate and the drain currents absorption. Finally, an infrared camera is used for the thermography images and step response monitoring. In figure 5.7, the schematic diagram of the test bench is shown.

The PCB has been tested with different electrical conditions. For steady-state analysis, thermal records have been acquired once the temperature is stable on the top device surface. As reference, thermal measurements have been acquired with a gate power dissipation of 6.91 mW, and a power absorbed by the GaN device on the drain side of about 0.884 W. From these values, the total device power dissipation can be calculated with the value of 0.891 W. Considering these electrical conditions and a room temperature of 23.4 °C, a top device surface temperature of 101.5 °C has

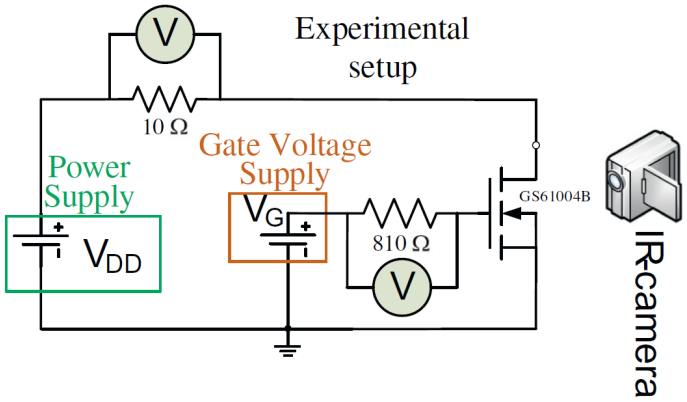


Figure 5.7: Schematic diagram of the test bench.

been measured. Figure 5.8, shows the thermal image measurement.

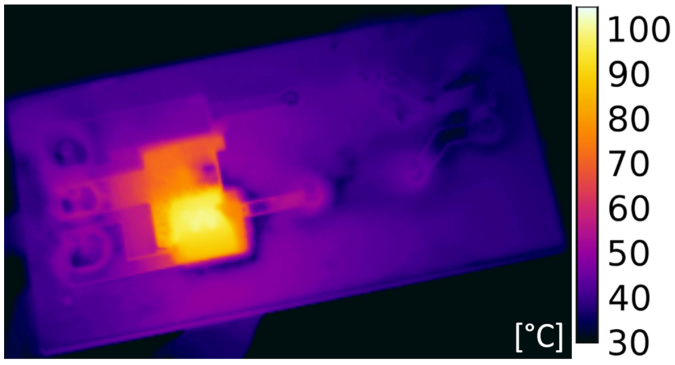


Figure 5.8: IR image with steady state conditions of power dissipation (0.891 W) at ambient temperature (23.4 °C).

5.1.2 Simulation Modeling and Results

Starting from the geometry of the reference PCB, the FEM model defines each domain of the 3D geometry. COMSOL Multiphysics 5.3 software has been used for the simulations, with the Heat Transfer in Solids study. The GaN layer domain of the

power device has been used as a heat source, with the rate of 0.891 W. For the heat flows boundary conditions, each edge of the board has been set with different heat fluxes due to the diverse convection rates. In particular, the bottom heat transfer coefficient has been set as $hbottom = 4\frac{W}{m^2 \cdot K}$, while the heat flux on the top surface of the board has been used as the fitting parameter. Physical properties have been set using the COMSOL library, such as heat capacity, material density, electron mobility, etc. However, the thermal conductivity of the GaN and the Si layers have been set with the following temperature dependent equations [92, 93]:

$$k_{GaN} = 160 \cdot (\frac{300}{T})^{1.4} [\frac{W}{m \cdot K}]; \tag{5.1}$$

$$k_{Si} = 148 \cdot (\frac{300}{T})^{1.65} [\frac{W}{m \cdot K}]. \tag{5.2}$$

The geometry mesh has been defined with COMSOL physics-controlled extra fine mesh. Other meshing densities have then been used for the validation steps, in order to understand how the meshing density conditions the steady-state temperature results. Finally, the temperature values obtained by thermal simulations have been compared to the measurements on the reference board. The convection coefficient on the top surfaces, used as fitting parameter, has been tuned to find a temperature matching and finally defined as $htop = 34\frac{W}{m^2 \cdot K}$. Figure 5.9, shows the simulated thermal map, and a good matching with the one obtained by infrared measurement at the same operating conditions has been found (figure 5.8).

Through simulations, respect to measurements, the internal temperature of the power GaN FET component can be evaluated. In the simulation results of figure 5.8, where the maximum surface temperature is 101.5 °C, the internal maximum temperature of the device is 101.86 °C. Therefore, with this specific package, the evaluation of the surface temperature can be considered accurate enough for a comparison between different board layouts or technologies.

However, the simulation model needs a verification and validation process. This has been carried out considering 5 points of the top surface of the device. These points are chosen near the four midpoints of the vertices, and the central point of the top surface. Figure 5.10, shows the points of interest.

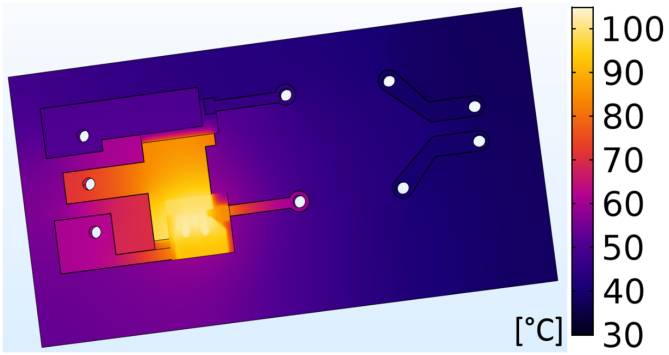


Figure 5.9: Simulated thermal map results with extremely fine mesh, $htop = 34 \frac{W}{m^2 \cdot K}$, power heat source set at 0.891 W, and ambient temperature equal to 23.4 °C.

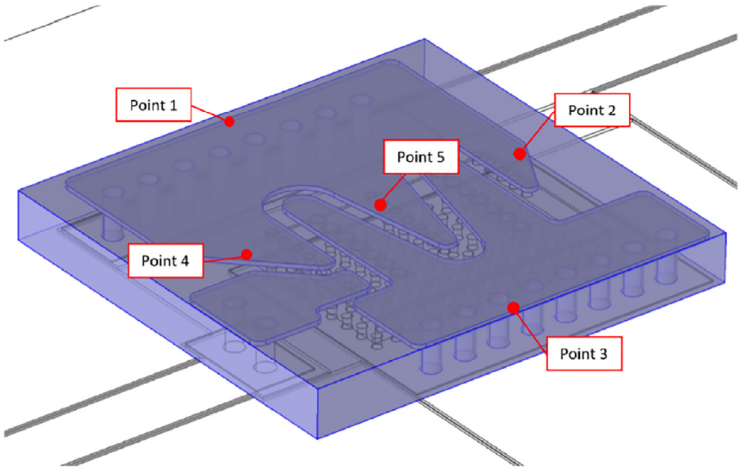


Figure 5.10: Top surface points of interest for verification and validation steps.

Measurements have been compared with simulation results with different meshing accuracy. Therefore, a verification of the mesh sizing effects on simulation results can be obtained. The variation of the temperatures on the 5 point of interest in relation to the mesh size is shown in figure 5.11. As can be expected, the meshing grid influences sensibly the temperature results. The accuracy of the simulation results can be improved through the homogenization meshing technique, as well as non-matching grid techniques [94].

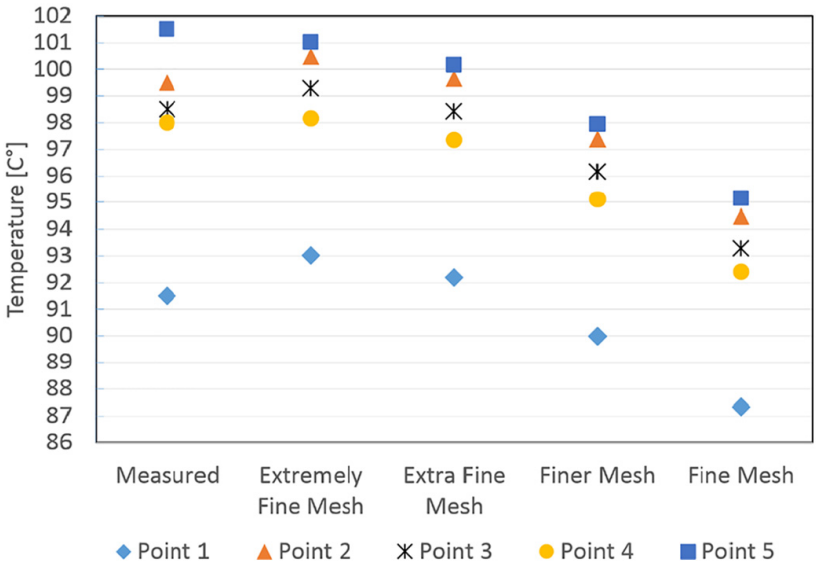


Figure 5.11: Verification of mesh sizing at the 5 points of interest, with a power dissipation of 0.891 W, the ambient temperature of 23.4 °C, $htop = 34 \frac{W}{m^2 \cdot K}$. Measured and simulated temperatures in comparison.

Starting from the reference simulation, a second layout solution has been defined and simulated. To maximize the power dissipation, larger drain and source pads have been designed and simulated with the same electrical characteristics. Improvements in the thermal design can be obtained also in relation to the board material chosen. In fact, with a board solution with Insulated Metal Substrate (IMS), the maximum simulated temperature results 53.6 °C by using the reference layout.

Another consideration has been done on the PCB fabrication steps for the copper traces isolation. A different choice can be made for the exceeding copper that is electrically floating: a board rub-out of the copper, or leaving the dead area copper as it is. From the electrical point of view, it can be considered irrelevant, but from the thermal point of view, an increase of almost 50 °C with the board cut-out solution is obtained. In fact, the thermal resistance between the FET's case and the ambient is greater if the copper area is reduced.

Finally, a multi-layer board has been considered. Simulations with two interleaved 35 μm copper layers have been done, and a good thermal improvement has been recorded. Finally, comparisons with a 2 GaN FETs layout (2) and the reference 1 GaN FET layout (1) are provided. Table 5.1, reports all the thermal simulation results.

Table 5.1: Comparison between simulated maximum temperatures of different board solutions. Power dissipation on the heat source is set to 0.891 W, ambient temperature to 23.4 °C.

	Natural air convection		Forced air convection	
	Without rub-out	With rub-out	Without rub-out	With rub-out
Reference layout (1)	101.5 °C	150.9 °C	76.4 °C	97.7 °C
Layout (1), 2 GaN FETs	139.8 °C	202.6 °C	92.5 °C	117.9 °C
Layout (1), IMS board	53.6 °C	54.4 °C	-	-
Revised layout (2)	101.5 °C	116.7 °C	78.2 °C	97.4 °C
Layout (2), 4 layers	72.3 °C	77.6 °C	57.6 °C	61.7 °C
Layout (2), 2 GaN FETs	102.1 °C	125.2 °C	72.7 °C	83.1 °C
Layout (2), IMS board	39.1 °C	43.7 °C	-	-

Results show that boards with IMS technology, 1.5 mm thick aluminum, without rub-out are the most promising solutions.

Considering the nanogrid application, simulations of the board have been done by designing a $7 \times 6 \times 3$ cm^3 box, with a still-air environment, thermally insulated walls, and 40 °C room temperature. This simulation environment represents the standard electrical sockets, where DC/DC converters are inserted, like the ones used for smart plugs. Figure 5.12, shows the 3D simulation model with the boundary condi-

tion parameters.

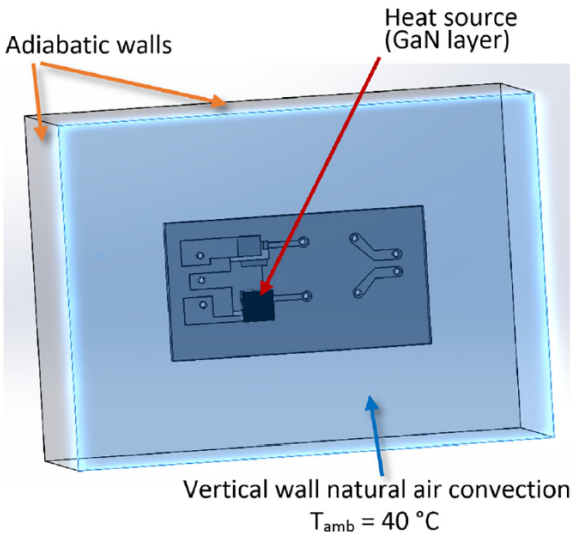


Figure 5.12: 3D simulation model of an electrical box with the related boundary conditions.

With boundary conditions representing a close environment, a dissipated power of 0.891 W on one GaN FET device, and the reference layout board, higher temperatures than the allowed 150 °C maximum operating junction temperature have been reached. Considering a solution with IMS technology, and lowering the dissipated power to 0.35 W, the simulated temperature reaches 124.5 °C with the reference board, and 99.5 °C with the layout revised board. Therefore, the board design has huge importance, in particular, because the GaN transistor does not have a flange for a heat sink and the heat flows mainly through the bottom electrical contacts. More details about the power GaN FET boards thermal optimization can be found in [A2].

5.1.3 Smart Plug Buck Converter Prototype Thermal Results

These thermal results help to obtain a correct design implementation of the GaN Systems GS61004B transistor, that has been used for the smart plug buck converter

prototype, as shown in chapter 2. Large source and drain pads have been provided, and the GaN transistor has been inserted so that it has space on almost all sides. The PCB prototype of the buck converter is shown in figure 5.13.

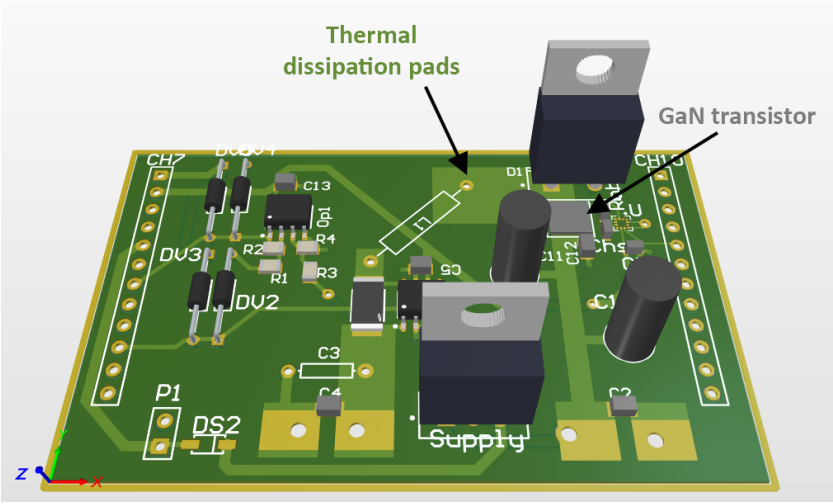


Figure 5.13: 3D model of the buck converter prototype for the smart plug.

Thermal tests of the smart plug buck converter prototype have been carried out. The worst case from the thermal point of view is when the GaN transistor dissipated more power. For this reason, efficiency can be extracted and the power dissipated can be calculated in relation to the power delivered to the load. Figure 5.14, shows the buck converter efficiency.

With an input voltage of 48 V, an output voltage controlled at 5 V, and a load resistor equal to 1 Ω (I_{out} = 5 A), the efficiency η of the DC/DC buck converter has been measured with the value of 0.71. In this case, the converter dissipated 8.78 W. With an output voltage controlled at 20 V, and a load resistor equal to 4 Ω (I_{out} = 5 A), the measured efficiency η has been equal to 0.94. Therefore, the converter dissipated 6.38 W. From these considerations, it is clear that the worst case from the thermal point of view is with an output voltage controlled at 5 V, and high power transfer.

With the case of V_{in} = 48 V, V_{out} = 5 V, I_{out} = 5 A, the GaN transistor reaches 108.5 °C. The related thermal map is shown in figure 5.15.

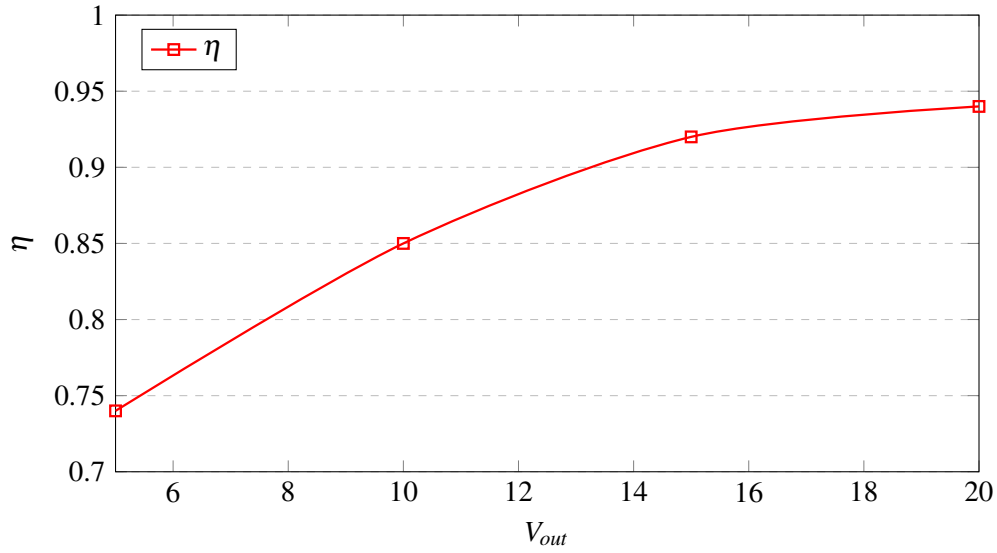


Figure 5.14: Buck converter prototype efficiency for the smart plug. Tests with output current I_{out} equal to 5 A, V_{in} equal to 48 V.

It has to be noticed that also the GaN transistor gate driver reaches very high temperatures. Considering that the package of the driver is a die-sized ball grid array (DSBGA) package and that it has been soldered manually, a possible non optimal thermal connection is provided, which results in a high temperature gradient.

Figure 5.16, the thermal map with the case of V_{in} = 48 V, V_{out} = 20 V, I_{out} = 5 A is shown. In this case, the efficiency is higher, and the power dissipated by the converter is lower (6.38 W). The GaN transistor reaches a temperature of 75.3 °C.

Thermal measurements show that with an I_{out} equal to 5 A, temperatures are in between acceptable ranges. However, it is clear that with higher power transfer, the buck prototype needs further improvements from the thermal point of view. Considering the study on the GS61004B transistor, improvements can be applied by enlarging the drain and source pads, avoiding manual soldering, and using an IMS board.

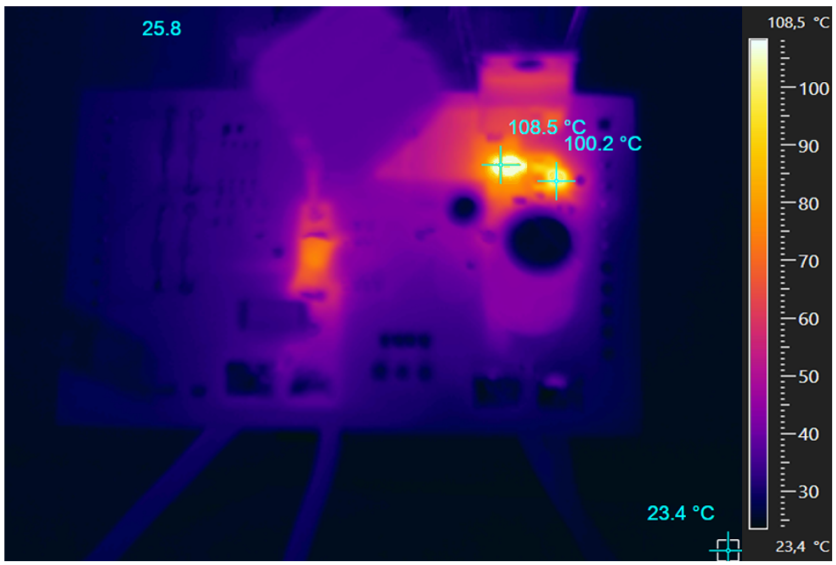


Figure 5.15: Thermal map of the buck converter prototype with V_{in} = 48 V, V_{out} = 5 V, I_{out} = 5 A. T_{amb} = 23.4 °C, and power dissipated by the converter P_D = 8.78 W.

5.2 Thermal Networks of Capacitors for Reliability Oriented Design

Unexpected failures of power converters can derive also from the over-temperature of capacitors [95]. Many applications require strict constraints on the reliability of capacitors (e.g. automotive [96]). Even if the self-heating of the capacitors does not exceed the maximum operating temperature, an over-temperature can be obtained by a harsh environment (such as for the TAB or smart plugs), or circuits where capacitors have to be close to other power dissipating devices, e.g. for EMC constraints or parasitic restrictions (TAB). Therefore, the features and performances of the capacitors, such as the Mean Time To Failure (MTTF), may not be guaranteed. However, signal integrity, stability, or protection of circuit devices features must be supported.

For applications like snubbers and DC-links, capacitors play very important roles. Typically, metallized film and electrolytic capacitors are used, and their aging is af-

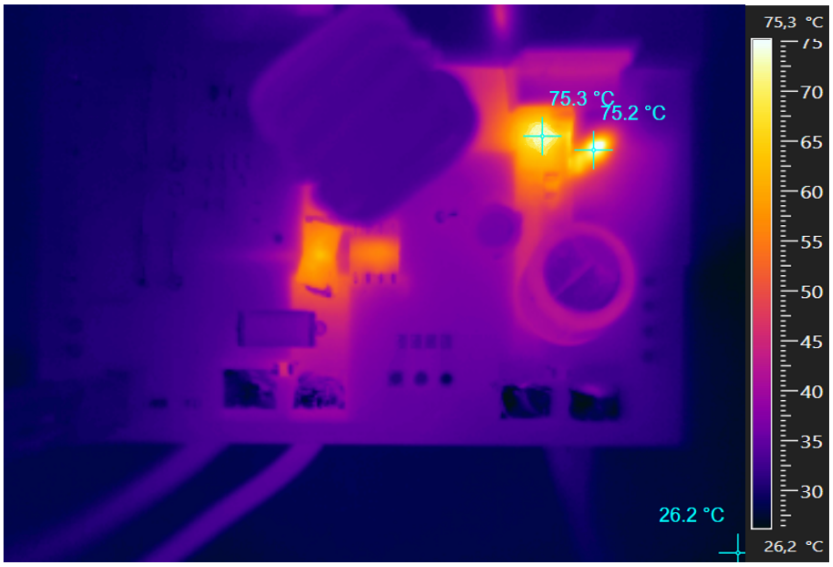


Figure 5.16: Thermal map of the buck converter prototype with V_{in} = 48 V, V_{out} = 20 V, I_{out} = 5 A. T_{amb} = 26.2 °C, and power dissipated by the converter P_D = 6.38 W.

fected by the temperature. This problem affects to greater degree electrolytic capacitors [97]. However, it cannot be neglected for metallized film ones [98, 99, 100, 101]. In literature, studies can be found on the electro-thermal analysis to evaluate the mission profile of DC-link for power converters [102]. Other works are focused on the MTTF evaluation with different kinds of dielectrics, for example in [103] with film capacitors for RCD snubbers. Commonly, the Arrhenius law is used for the capacitor lifetime prediction. The temperature-dependent stresses are therefore analyzed, both for the metallized film [104] and electrolytic capacitors [105]. The exponential Arrhenius law uses the stress-dependent activation energy (E_a) of a thermal process to determine the temperature-related aging (reaction rate R) of metallized plastic capacitors [106]:

$$R(temp) = \gamma_0 \cdot exp(\frac{-E_a}{k \cdot temp}) \tag{5.3}$$

where temp is the temperature in Kelvin, k is either Boltzmann's constant or the universal gas constant, γ_0 is the product or material characteristics. However, the Arrhenius relationship does not apply to all temperature acceleration problems and is adequate over only a limited temperature range (depending on the particular application). Experimentally, concurrent stresses typically can't be represented from a simple multiplicative model, and the Arrhenius law can be generalized with the Eyring theory [107]. More factors are therefore included for the lifetime estimation. Moreover, the interactions of thermal stress with other stress factors are considered (e.g. voltage, relative humidity, etc.).

Therefore, the equation can be rewritten as follows [108]:

$$T_{Eyring} = A \cdot T^{\alpha} \cdot exp[\frac{E_a}{kT} + S_V \cdot (B_V \cdot \frac{C_V}{kT}) + S_{RH} \cdot (B_{RH} \cdot \frac{C_{RH}}{kT})] \tag{5.4}$$

where S_V is the stress function in relation to the capacitor applied voltage, S_RH is the stress function in relation to the relative humidity, k is the Boltzmann constant, T is the temperature in Kelvin, E_a is the activation energy, α, A, B_V, C_V, B_{RH}, and C_{RH} are constants to be heuristically determined, independent of time, temperature and stresses. The heuristic models can be different in relation to the dielectric materials

of the capacitors. The lifetimes of metallized film capacitors are widely explored in the literature ([109, 110, 111]) and the most used empirical model uses temperature and voltage stresses as shown in the following equation [103]:

$$L = L_0(\frac{V}{V_0})^{-n} \cdot exp[(\frac{E_a}{k})(\frac{1}{T} - \frac{1}{T_0})] \tag{5.5}$$

where: L is the lifetime, V the voltage, and T the temperature in Kelvin under actual operating conditions, while L_0 is the lifetime, V_0 the voltage, T_0 temperature in Kelvin measured during reference tests conditions. n is the voltage stress exponent to be heuristically evaluated. E_a and n are the key parameters to be determined to evaluate the capacitor lifetime. However, the temperature has to be known (measured or simulated). Therefore, failures and rapid aging can be prevented by the evaluation of the expected maximum operative temperature of capacitors.

5.2.1 Reference Capacitor and Experimental

FE simulations to compute a lumped-parameter thermal model of capacitors can be used to extract Foster or Cauer networks. These can be coupled to the electrical model to evaluate the temperatures of capacitors in circuit simulators such as SPICE or MATLAB/Simulink. In this section, the workflow shown in 5.1 is used for the design of snubber capacitors for a medium power (60 kW) high-frequency AC/AC converter [112], shown in figure 5.17.

The snubber film capacitors are used in this converter to filter the power signal on the rectified lines. Due to filtering requirements, these capacitors are placed near the switching devices. Therefore, thermal management is a very critical issue. In particular, the capacitor sizing considers not only self-heating but also heat transfer between copper bus bars, power devices (diode rectifiers and IGBTs), and the capacitors themselves. Figure 5.18, shows in detail the copper bars, snubber capacitors, diodes, and IGBTs of the converter.

Early tests of a first prototype of the converter without thermal design precautions show how these devices failed shortly with clear damages in the capacitors. In figure 5.19, cracks can be seen on the capacitor packages, where the plastic film is damaged.

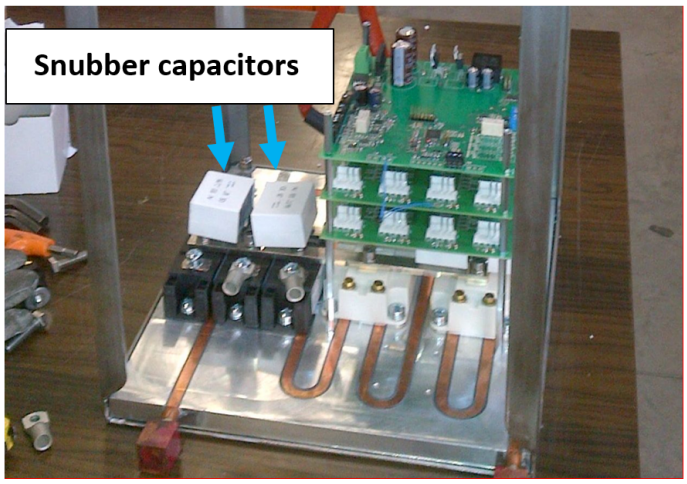


Figure 5.17: Medium power (60 kW) high-frequency AC/AC converter with snubber capacitors.

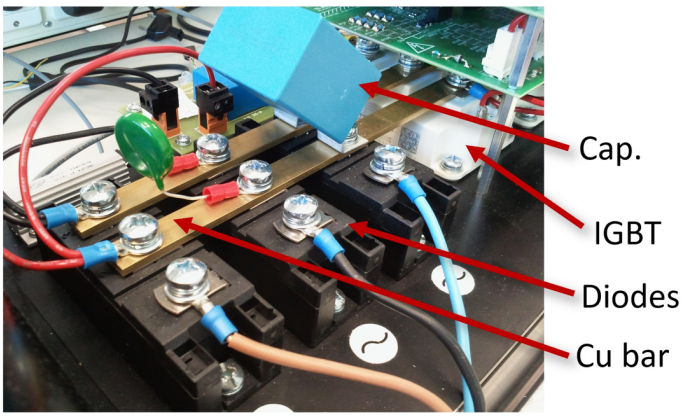


Figure 5.18: Copper bars, snubber capacitors, diodes, and IGBTs of the converter.

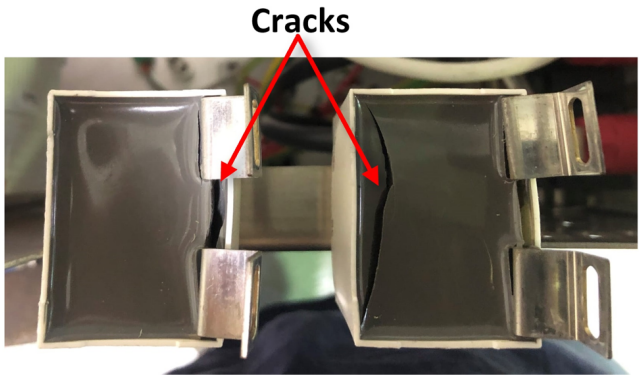


Figure 5.19: Damaged capacitors after early tests of a first converter prototype: the packages are cracked, and the plastic film is damaged.

5.2.2 Simulation Modeling and Results

To avoid failures, a compact thermal model for capacitors has to be developed and simulated. To define the 3D model, in particular when the capacitor has many layers and a huge area, a simplified single electrode-dielectric-electrode structure with a limited area can be used. In fact, this enables to reduce the degrees of freedom in FEM analysis. Figure 5.20, shows the simplified Metal-Insulator-Metal (M-I-M) structure, from which an homogeneous thermally equivalent block has been extrapolated.

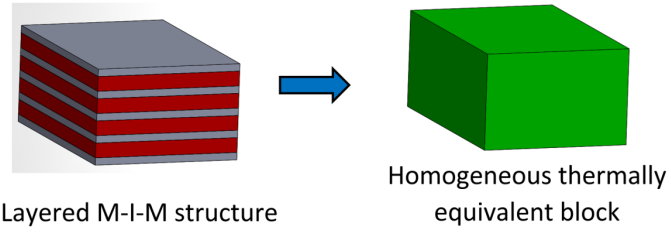


Figure 5.20: Approximation of the M-I-M stack with a homogeneous thermally equivalent block for transient simulations.

A first model with different M-I-M layers has to be defined for a coupled electro-

thermal analysis. With this first model, the dissipated power density is evaluated to set a power step in a simplified 3D model for thermal transient analysis. The simplified 3D structure considers a domain of the stack built to obtain the specific capacitance as a unique volume of homogeneous material. The thermal properties of the equivalent block are evaluated as follows:

$$p_{hom} = \frac{\rho_m V_m p_m + \rho_d V_d p_d}{\rho_m V_m + \rho_d V_d} \tag{5.6}$$

where p_m and p_d are the thermal properties (e.g. thermal conductivity or heat capacity), ρ_m and ρ_d are the material densities, V_m and V_d are the volumes of the metal electrodes and dielectric, respectively.

The FE model has to be verified and validated through experimental tests as shown in figure 5.2. The capacitor used as the test device is a metallized polypropylene (PP) capacitor. Parameters are a capacitance of C equal to 1 μF, a rated AC voltage of 305 V, a maximum continuous DC voltage VDC of 630 V, and a maximum rating temperature Top of 105 °C. An inspection has been carried out to measure the thickness of the metal (2 μm) and the dielectric (10 μm) layers. Moreover, a LCR meter has been used to measure the dissipation factor tanδ at 100 kHz. The same frequency has been used for electro-thermal characterization. A sinusoidal voltage has been applied to the capacitor using a classic RLC series circuit. Figure 5.21, shows the schematic circuit used for the electro-thermal characterization.

To generate the square wave signal, a half-bridge circuit with two power TPH3212PS GaN transistors by Transphorm ($V_{ds(MAX)}$ = 650 V, $I_ds(MAX)$ = 27 A, $R_{ds(on)}$ = 72 mΩ) has been used. The devices on-resistances R_{on} have been used as the series resistance of the RLC circuit. Therefore, the damping ratio is negligible. A ST Microelectronics NUCLEO board has been used to generate the logic input signals, and a FLIR A325 IR camera has been used for the thermal map measurements. The ad-hoc realized test bench is shown in figure 5.22.

Figure 5.23, shows the electrical experimental results. Tests have been carried out with the sinusoidal frequency of 100 kHz, the voltage amplitude on the capacitor of 8 V, and the input DC power supply voltage of 35 V.

From the electrical point of view, the capacitor can be modeled with lumped

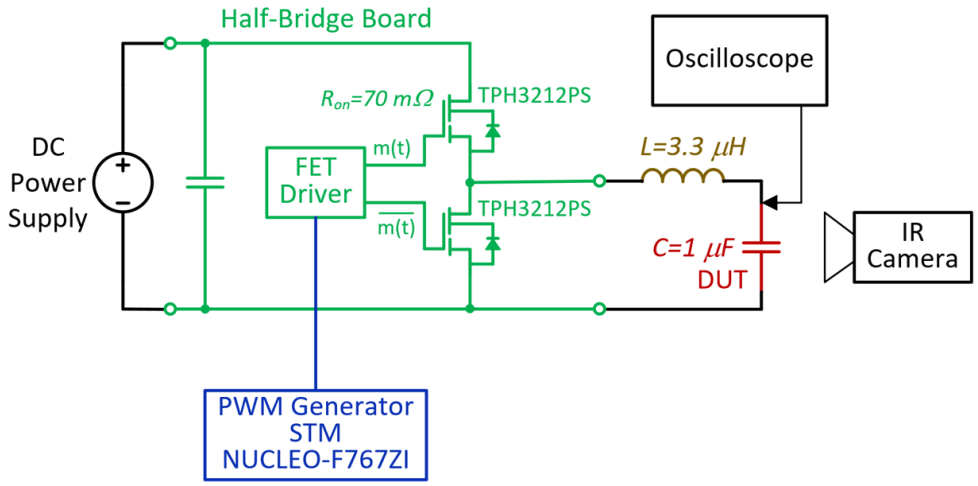


Figure 5.21: Schematic of the RLC series circuit used for eletro-thermal characterization. The circuit generates a sinusoidal voltage on the capacitor C, which is the Device Under Test (DUT).

elements. Therefore, the Equivalent Series Resistance R_s (ESR), the Equivalent Series Inductance L_s (ESL), and the insulation resistance R_p have to be defined. Moreover, the dielectric losses due to absorption and molecular polarization can be represented by a resistance R_d, with series a capacitor C_d representing the inherent dielectric absorption, both in parallel to the capacitor C [113]. The general lumped element model of the capacitor is shown in figure 5.24.

The values of the lumped elements are dependent on the operating conditions. Frequency, voltage, temperature, and time should be taken into consideration [103]. Therefore, if the relations are not properly considered, the lifetime prediction could easily differ from the real one.

For less precise simulations, the capacitor with a series resistance R_s can be used as simplified model, where the dissipation factor $tan\delta = \omega R_s C$ represents the capacitor losses. A thermal lumped-parameter network can be added to evaluate the temperature behavior. However, it could be very difficult to have a thermal behav-

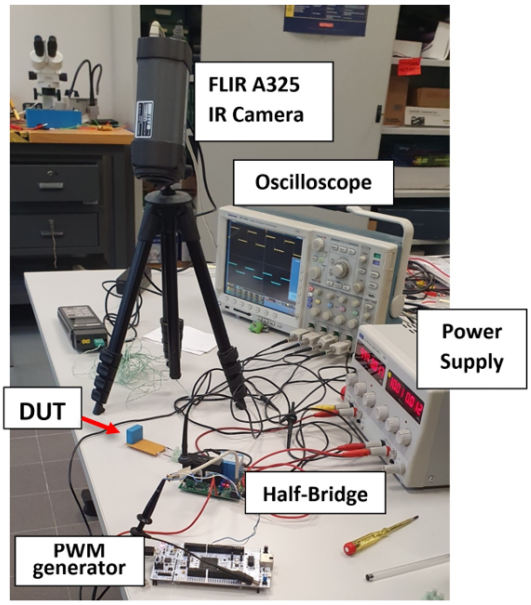


Figure 5.22: Test bench used for electro-thermal characterization.

ior fully coupled to the electrical one. Therefore, FEM simulations could be a good solution to this issue.

In this work, the software COMSOL Multiphysics 5.3 has been used. For stationary electro-thermal simulations, the wrapped metallized layers have been modeled as a simpler stack, and the terminals have been removed. Therefore, symmetry has been obtained, and the simulation study has been applied to a quarter of the whole capacitor. Electrically, a sinusoidal and a ground signal have been alternatively applied to the metal layers with, in between, a dielectric layer where the measured dissipation factor was set as the dielectric $tan\ \delta$. Figure 5.25, shows the FE model of the capacitor for stationary electro-thermal analysis.

The thermal boundary conditions have been defined with natural air convection coefficients, with different values depending on the vertical and horizontal surfaces. A good matching between simulation results and measurements requires fine meshing. However, for transient study, the fully coupled electro-thermal model needs very

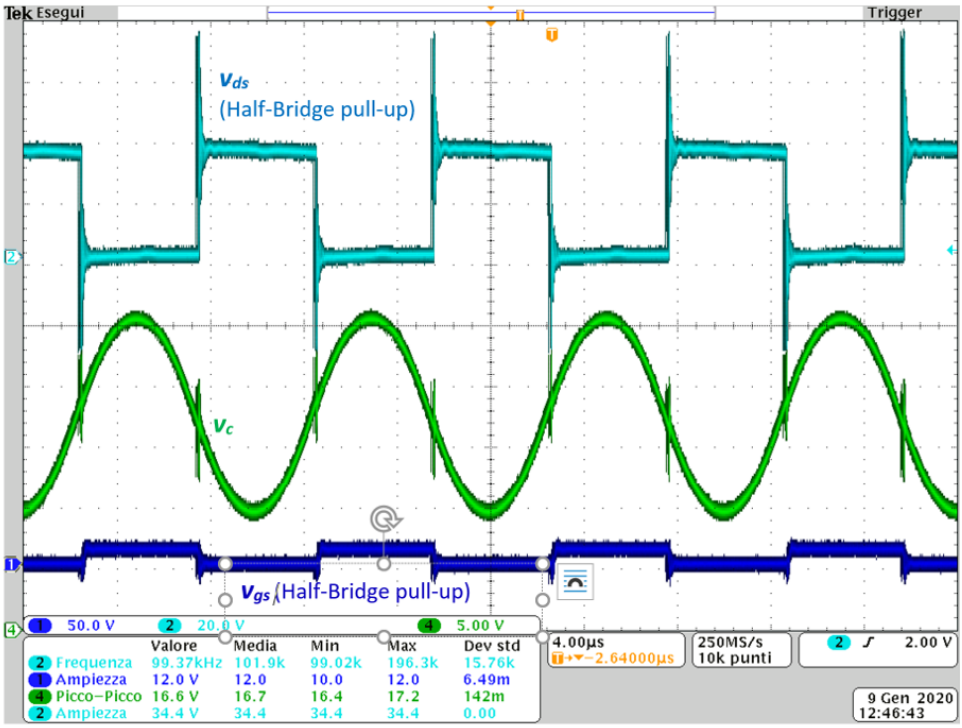


Figure 5.23: Traces acquired by the oscilloscope. Cyan trace: drain to source voltage of the half-bridge pull-up transistor; blue trace: gate to source voltage of the half-bridge pull-up transistor; green trace: capacitor voltage.

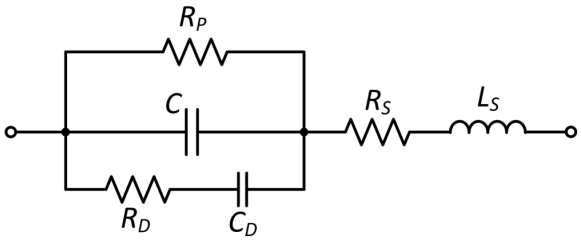


Figure 5.24: General lumped element model of the capacitor.

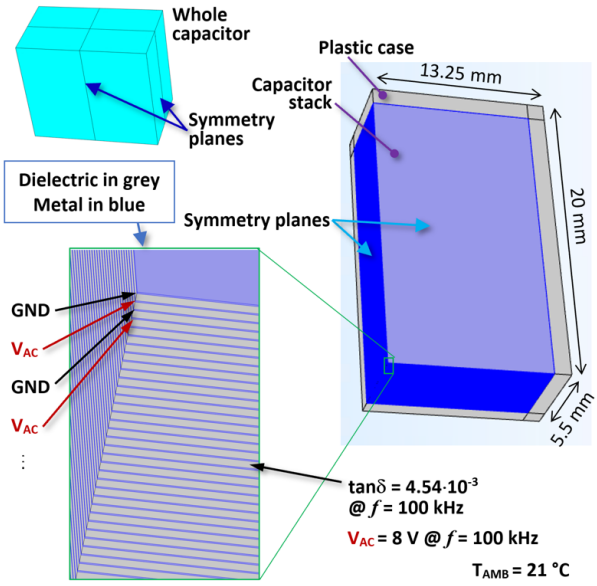


Figure 5.25: FE model of the capacitor for stationary electro-thermal analysis.

high computing power. Therefore, further approximations of the model have been provided to obtain a homogeneous thermally equivalent block, as shown in figure 5.20. Here, the heat generated in the steady state study has been used as the value to be applied as a power step. Figure 5.26, shows the thermal map of the simplified structure with steady state conditions, where a good matching with measurements has been achieved. A specific point on the capacitor surface has been identified for measurement and simulation comparison. This point is shown with a marker on the measured thermal map.

The transient behavior on the identified point of interest has been analyzed with measurements and simulations. Figure 5.27, shows the response of temperature value on the point of interest. The difference in steady-state conditions is less than 0.3 °C.

Considering the good matching between measurement and simulations, the temperature at the center of the capacitor can be estimated directly from the simulations, which is the maximum temperature operating point. Once the thermal power step

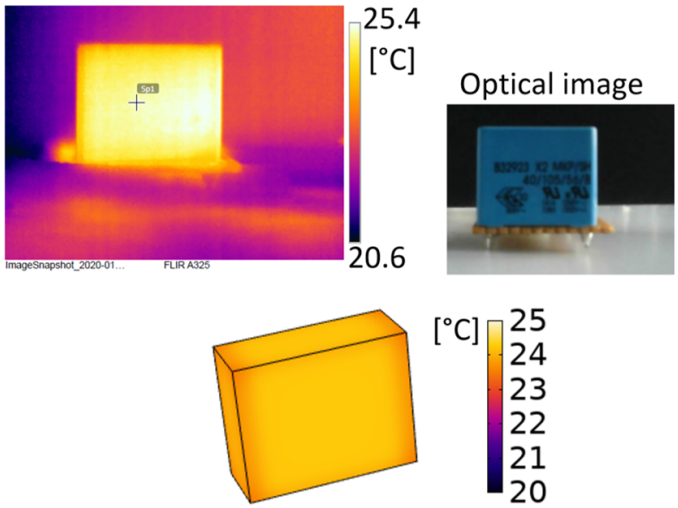


Figure 5.26: Measured (top-left) and simulated (bottom) surface thermal map at steady state conditions, with V_{AC} = 8 V, f = 100 kHz.

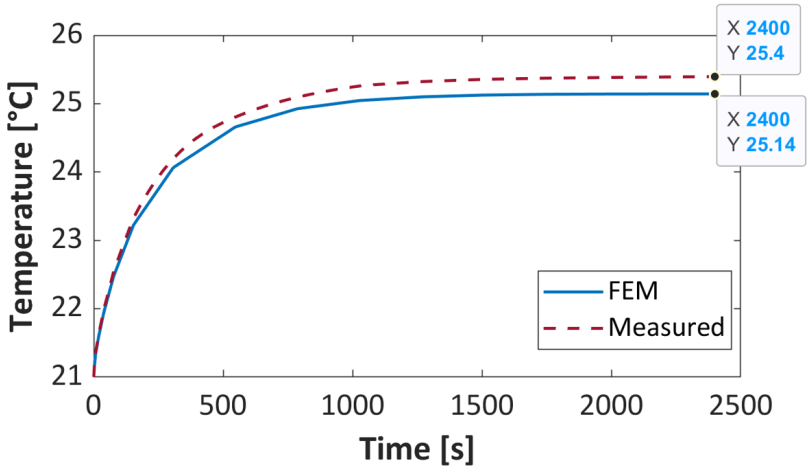


Figure 5.27: Simulated and measured temperatures at a specific surface point during a power step response with V_{AC} = 8 V, f = 100 kHz.

response is obtained, the Foster network can be extracted [114]. Figure 5.28, shows the network that models the capacitor, where the ground is the ambient temperature and P_d is the dissipated power. $T_{centercap}$ represents the temperature at the capacitor center.

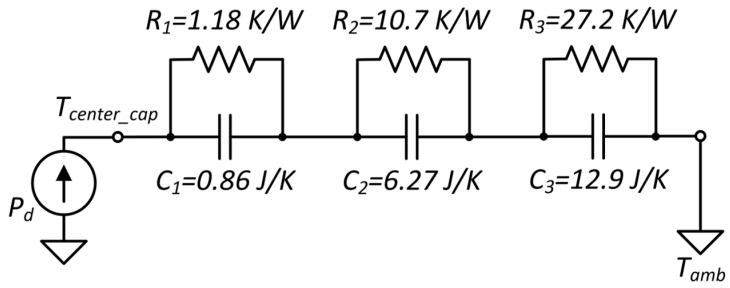


Figure 5.28: Foster network extracted for the reference capacitor.

Three stages are the result of a trade-off between network complexity and good simulated thermal impedance matching. The relative error between the simulation results of FEM and the Foster thermal network depends on the following relation:

$$RelativeError = |\frac{Z_{thFEM} - Z_{thFoster}}{Z_{thFEM}}| \cdot 100 \tag{5.7}$$

where Z_{thFEM} and $Z_{thFoster}$ are the thermal impedance evaluated by the FEM simulation, and by the Foster network, respectively. Each thermal impedance is evaluated as follows:

$$Z_{th}(t) = \frac{P_d(t)}{T_{centercap}(t) - T_{amb}} \tag{5.8}$$

where $P_d(t)$ is the dissipated power during the power step, and T_{amb} is the ambient temperature, kept constant during the power step response.

From these considerations, the maximum relative error between FEM simulation results and the thermal impedance during the power step response is around 3 %. Figure 5.29, shows the relative error during time, with the power step response. The point of reference is the center of the capacitor in relation to the ambient temperature.

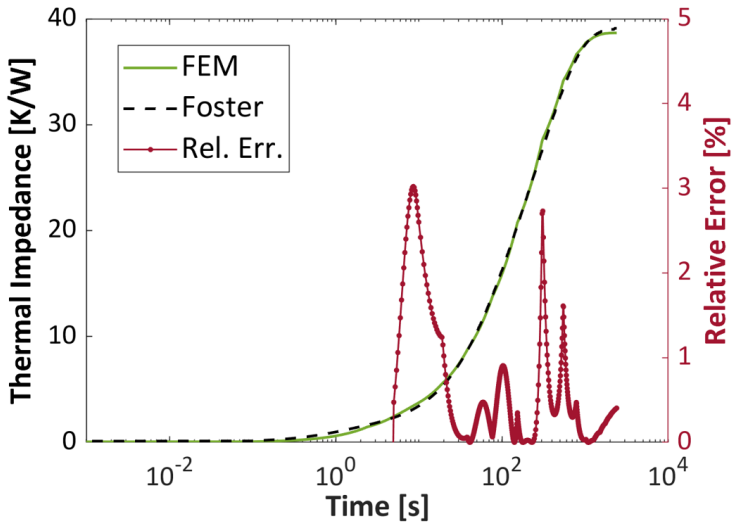


Figure 5.29: Comparison between simulation results of FEM, and Foster network thermal impedance. The red trace represents the relative error during a power step response with V_{AC} = 8 V, f = 100 kHz.

To take into account the mutual influence of the other power devices present in the circuit, multiple inputs as heat sources can be added to the lumped element thermal network. In particular, they can be added at ambient temperature, but also in other points of interest [115].

Finally, these simulations give information on the operative temperature of the reference capacitor. Lifetime analysis can be carried out and the circuit design can be optimized to achieve proper robustness and cost-effectiveness. More details about the thermal networks of capacitors for reliability oriented design can be found in [A7].

5.2.3 TAB Thermal Test Results

The TAB converter prototype has been thermally tested as well. The thermal IR camera has been used during all the electrical tests, focusing on the whole converter, including the three EPC9047 half-bridge boards using the EPC2033 transistors ($V_{ds(MAX)}$ = 150 V, $I_{ds(MAX)}$ = 48 A, $R_{ds(on)}$ = 7 mΩ). Good thermal behavior of the circuit has been registered during all tests. In figure 5.30, the thermal map with three parallel solar PV modules, four 12 V batteries in series, a load of two parallel 10 Ω, and a controlled V_{bus} of 48 V is shown.

During the tests, forced air has been provided on the power resistors to keep acceptable temperatures. However, the fans are far from the TAB circuit, therefore, the circuit it-self can be considered with almost natural air convection.

The power dissipated by the TAB (P_d) can be calculated as the sum of conduction loss in each full bridge:

$$P_d = (I_{1RMS}^2 + I_{2RMS}^2 + I_{3RMS}^2) \cdot 2 \cdot R_{on} \tag{5.9}$$

where I_{xRMS} is the RMS value of the current I_x flowing through the first transformer port. The current I_{1RMS}^2 can be calculated as [116]:

$$I_{1RMS}^2 = \frac{V_{PV}^2}{4 \cdot \omega(L_1 + L_{l1})} \cdot [1 + (2 \cdot \frac{V_{PV}}{V_{bus}} \pi\delta_{12} - \frac{V_{BAT}}{V_{bus}} \pi\delta_{23})^2] \tag{5.10}$$

where L_{l1} is the leakage inductance of the transformer winding.

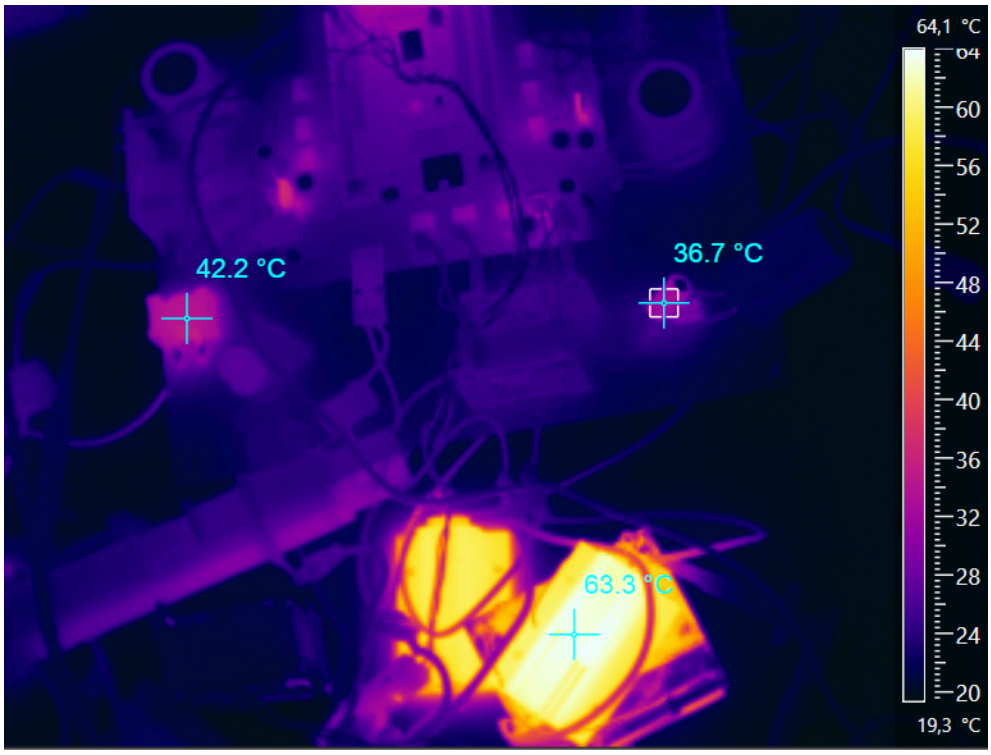


Figure 5.30: Measured thermal map with three parallel solar PV modules, four 12 V batteries in series, a load of 10 Ω, and a controlled V_{bus} of 48 V. Irradiation is 680 W/m^2, battery SoC is approximately 50 %.

Taking for example the experimental results shown in figure 2.23, the three RMS values of the current are measured, and the values are: I_{1RMS} = 6.16 A, I_{2RMS} = 4.65 A, I_{3RMS} = 3.16 A. Therefore, a dissipated power P_d in the order of 1 W is expected. The same value can be calculated with (5.10), considering V_{PV} = 60 V, V_{bus} = 26 V, V_{BAT} = 14 V, and δ_{12} = 0.47, δ_{13} = 0.45.

From these considerations, it is clear that the current on the inductors can reach high values. In particular, the inductor on the primary port, where solar PV modules are attached with the highest voltage. This one has to be kept under control from the thermal point of view. The inductor reaches a temperature of 42.2 °C in the case shown in figure 5.30.

Also, the filter capacitor of the bus port, where the highest reactive current values flow (output current I_{bus} = 9.6 A). A weakness from the thermal point of view can be found if the output voltage is controlled at lower values, e.g. 5 V. In this case, the reactive current on the capacitor increases sensibly.

Conclusions

The main object of this work has been to explore the NGs related research fields, and the power converters suitable for DC NGs architectures. The lack of standardization for NGs leads to multiple approaches for their development. Different issues such as the standard systems retrofit, reliability, efficiency, control strategy, etc. have to be addressed. In literature, different publications can be found with a focus on control strategies, smart management, or system level definition. However, islanded DC NG architectures are less explored than AC, DC, or hybrid architectures with a power grid connection. Moreover, the converter topologies that should be used are strictly related to the NGs architecture, and unused topologies can gain interesting advantages in dependence on the identified architecture.

In this work, a DC NG architecture has been proposed, with a TAB converter as the key element. GaN semiconductor devices have been used both for the TAB and for point of load converters. The TAB interfaces solar PV modules, batteries, and the DC bus for load interconnection. The three DC ports are connected to Full-bridges, controlled with phase-shifted PWM signals. The Full-bridges are then connected to a high-frequency transformer for the power transfer between the ports. A bus voltage control loop with a PI block has been provided for the load power transfer. Then, an MPPT algorithm has been implemented for the phase-shift control between PV and battery, in order to maximize the PV power extraction. Current feed forward has been analyzed to both maintain low ripple on the bus voltage, and to avoid the loss of MPP.

In this thesis, a state of the art on NGs architectures is presented in chapter 1, through literature research and to contextualize the proposed NG. Then, the bidirec-

tional three-port TAB converter has been analyzed, starting from the working principle, then with a simulation model. Both, power electronics on the transistor level, and the control strategy on the system level have been analyzed through ad-hoc simulations. The simulation model has been validated through early experimental results. Then, tests have been carried out with the TAB, interfacing three PV modules, four batteries, and power resistors as load (chapter 2).

The proposed NG includes smart point of load converters (smart plugs) as well. A USB-C PD derived protocol has been thought and a 1 MHz buck converter has been designed with GaN transistors. The smart plugs can reduce or increase the voltage and current ratings through negotiation with the attached loads. At the same time, the SCU can give directives to reduce or increase the power delivered to the loads by smart plugs. Afterward, an ad-hoc active load board through buck-boost-derived topology has been designed for the NG devices tests. Arbitrary power profile absorption is the main object of the active load (chapter 3).

The use of solar PV modules in an off-grid NG prototype requires particular attention to the monitoring and maintenance processes of the PV modules. For this reason, PV monitoring issues have been analyzed and an ad-hoc board with a soiling sensor, irradiation measuring, and I-V characteristic extraction has been developed. Whenever the power output of the PV array reaches low values, an I-V characteristic can be extracted and used to analyze the attached PV modules (chapter 4).

As a relevant issue in power electronics, where high power density circuits have to be designed, thermal analyses on the different components and prototype boards have been done and described in this thesis. FEM simulations have been used to analyze the maximum operating temperatures as the junction temperature of GaN devices, or the center temperature of metal-insulator-metal capacitors. Thermal maps and thermal dynamic behavior have been described in relation to their reliability issues (chapter 5).

The contributions of this work can be summarized as follows:

- A new DC NG architecture has been proposed, with a TAB converter for the PV, battery, and DC bus interface. The results show a necessary trade off between the switching frequency and the power transfer between the ports of the

TAB due to its intrinsic behavior. However, simulations and results show different working conditions of the architecture, demonstrating that the proposed NG could be a suitable solution;

- Smart point of load converters have been developed and a 1 MHz buck converter has been designed for a good retrofit into existing building sockets;
- An ad-hoc active load board has been designed with a buck-boost derived topology. This board could be used for the emulation of different DC loads;
- PV modules monitoring has been investigated and a soiling sensor has been developed. PV maintenance processes could be improved and expensive cleaning actions could be avoided;
- Thermal analyses of different components and prototype boards have been done. A new method for thermal evaluation has been defined for optimal layout design.

The presented work has been used in six scientific publications. Moreover, other marginal activities have been carried out during the PhD period. FEM simulations, for example, have been carried out also for liquid cold plates for power press-pack assemblies. Considering the power size of DC NG, it is very unlikely that a liquid cold plate needs to be used. However, for microgrids or in case of impossibility for air convection, and high working temperatures, liquid cold plates could be the only available solution. Aluminum additive manufacturing technology has been explored to improve the cold plate trade-offs between water pump strengths, sizes, and reliability issues.

Research activities have been carried out also in the automotive application field. FEM simulations have been done for a specific HF coreless transformer, used for Federal-Moguls' Advanced Corona Ignition System (ACIS). The ACIS allows the implementation of complex combustion strategies and can replace the traditional spark plug. A circuit for high efficiency voltage conversion from the 12 V classical car battery voltage to 96 V uses the transformer at a frequency of 5 MHz. Besides, behavioral models of Infineons' discrete smart switches called $PROFET^{TM}$

have been done. System-level simulations have been conducted of mission profiles with different load circumstances. The aim of this work is the study of the behavior of the smart switches in the car NG, considering all the protection functions such as current limitation, under-voltage protection, thermal protection, etc.

Finally, a marginal activity has been carried out with the collaboration of the National Institute of Nuclear Physics (INFN) of Milano. In the context of the CERN facilities, and in particular the DUNE experiment, Power over Fiber (PoF) has been analyzed. The idea is to use the PoF to supply different Silicon Photomultiplier (SiPM) at cryogenic temperatures. Therefore, DC/DC converter solutions have been studied, and discrete electronic devices have been analyzed and characterized at cryogenic temperatures.

Appendix A

List of Publications

A1 N. Delmonte, P. Cova, D. Santoro, A. Toscani, and G. Buticchi, "Development of a GaN based triple-active-bridge for DC nanogrid," in 2018 20th European Conference on Power Electronics and Applications, EPE 2018 ECCE Europe, 2018.

A2 P. Cova, N. Delmonte, and D. Santoro, "Power GaN FET boards thermal and electromagnetic optimization by FE modeling," Microelectronics Reliability, vol. 100-101, Sep. 2019, doi: 10.1016/j.microrel.2019.113466.

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A12 M. Simonazzi, D. Santoro, M. Bernardoni, N. Delmonte, P. Cova, and R. Menozzi, "Behavioral modelling of PROFET™ devices for system-level simulation of mission profiles in automotive environment applications," Microelectronics Reliability, vol. 126, Oct. 2021, doi: 10.1016/j.microrel.2021.114324.

Appendix B

TAB Interface Board: Circuit Schematic and PCB Layout

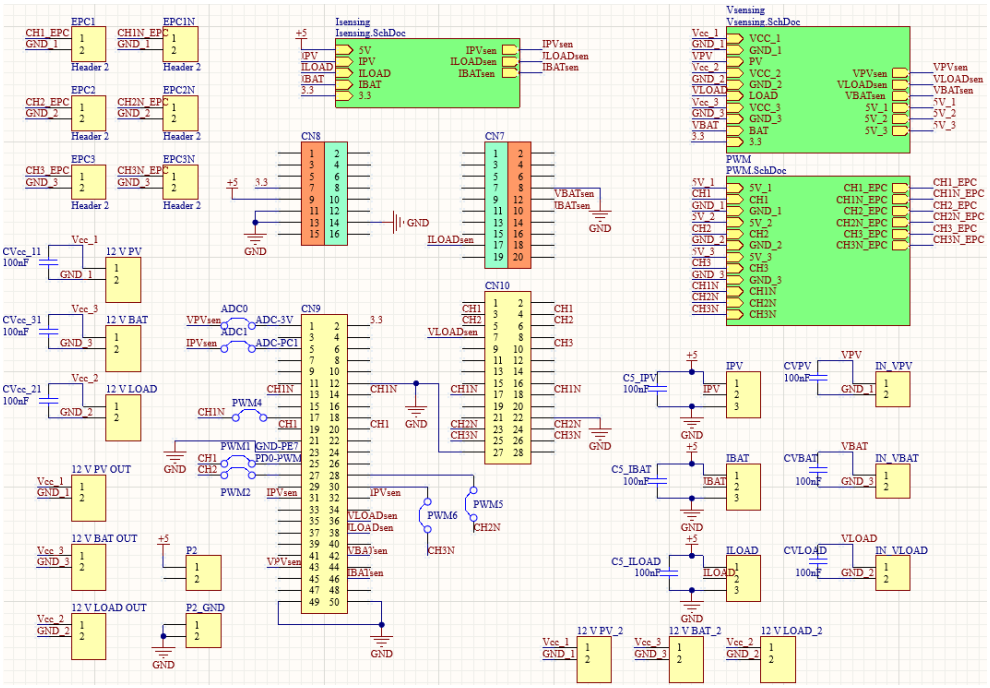

Figure B.1: TAB interface board connectors and sheets entries schematic.

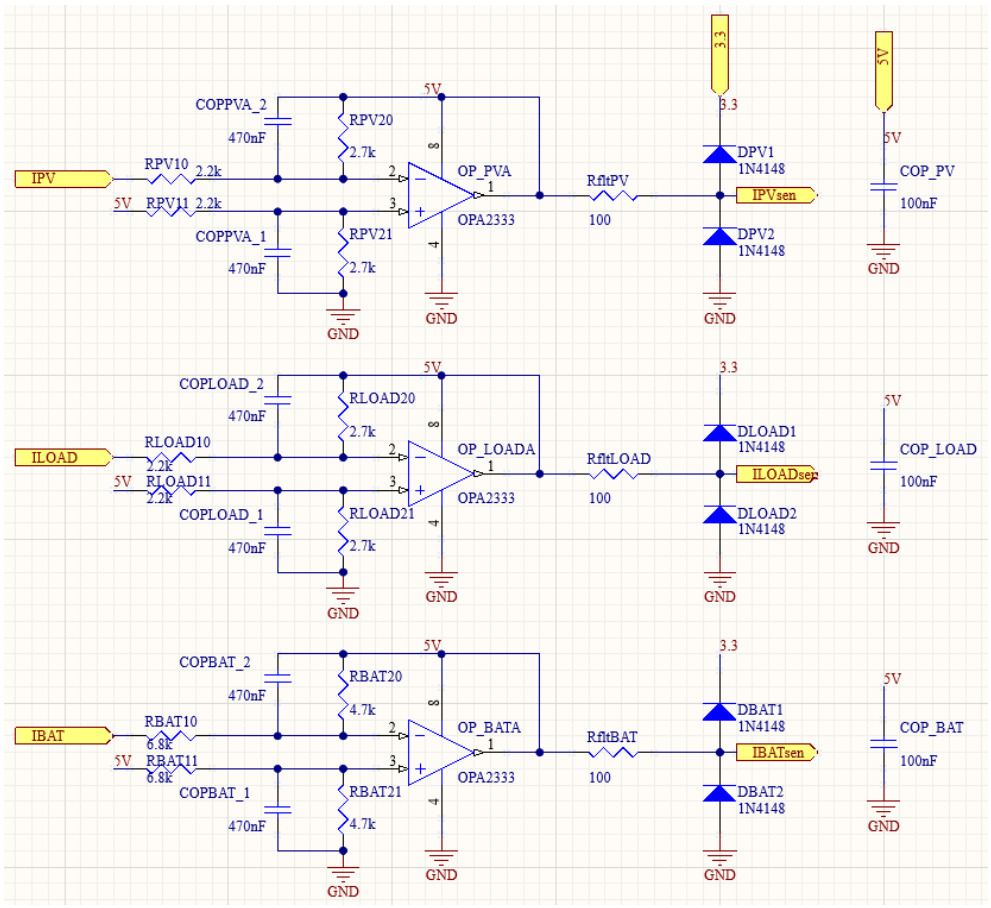

Figure B.2: TAB interface board current sensing schematic.

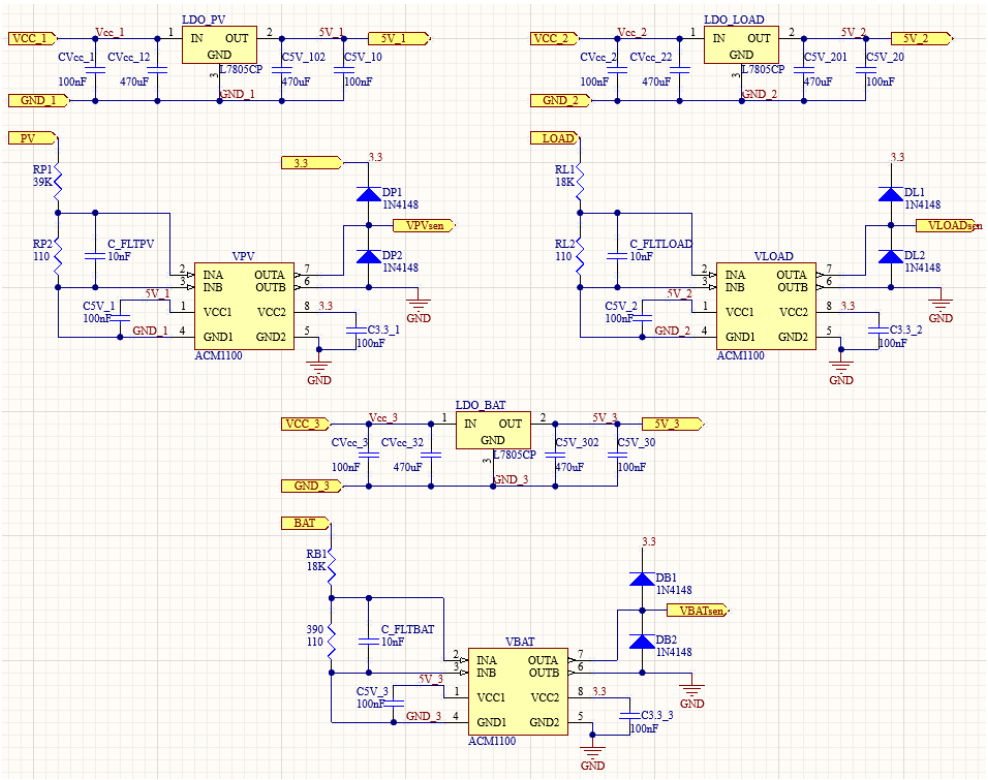

Figure B.3: TAB interface board voltage sensing schematic.

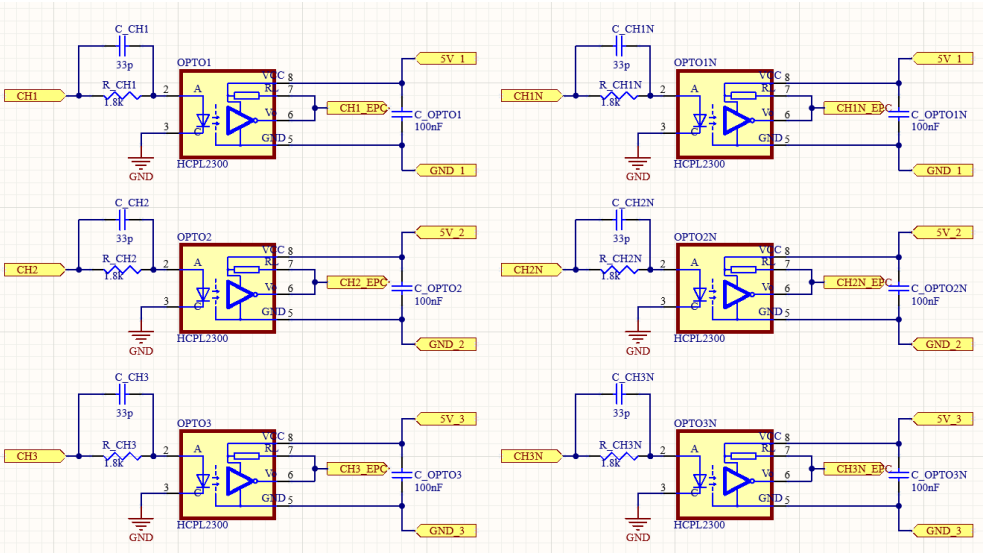

Figure B.4: TAB interface board PWM conditioning schematic.

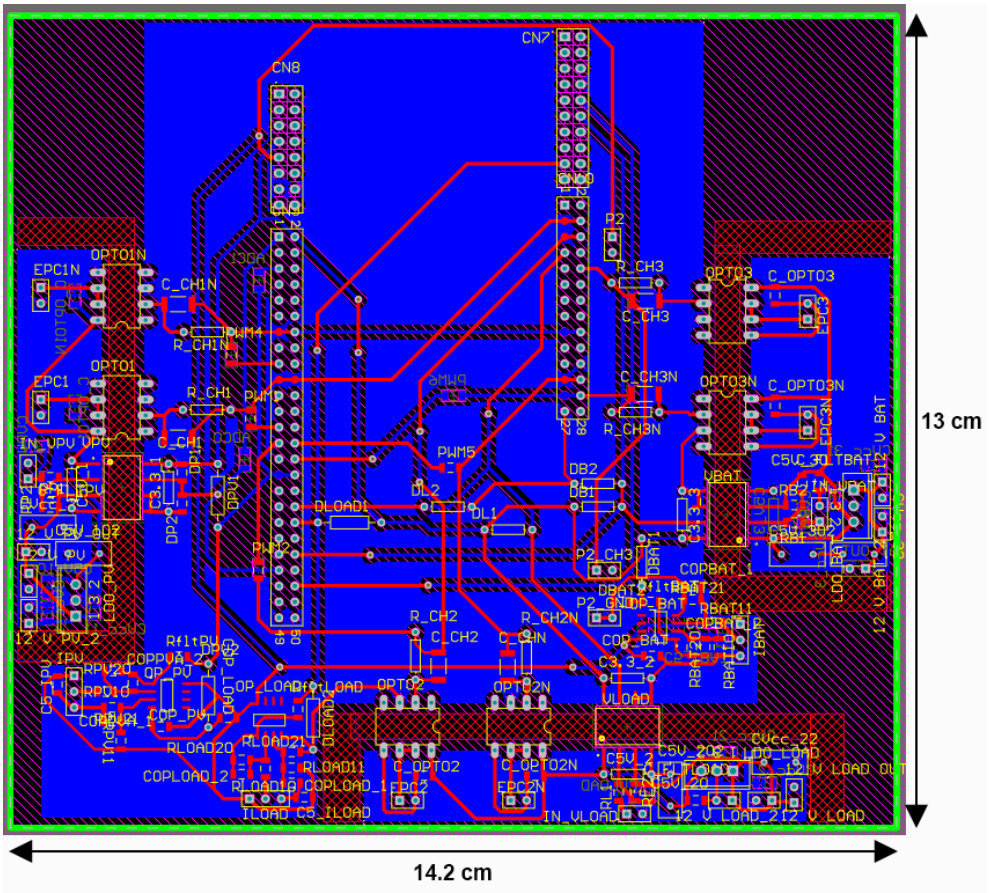

Figure B.5: TAB interface board layout.

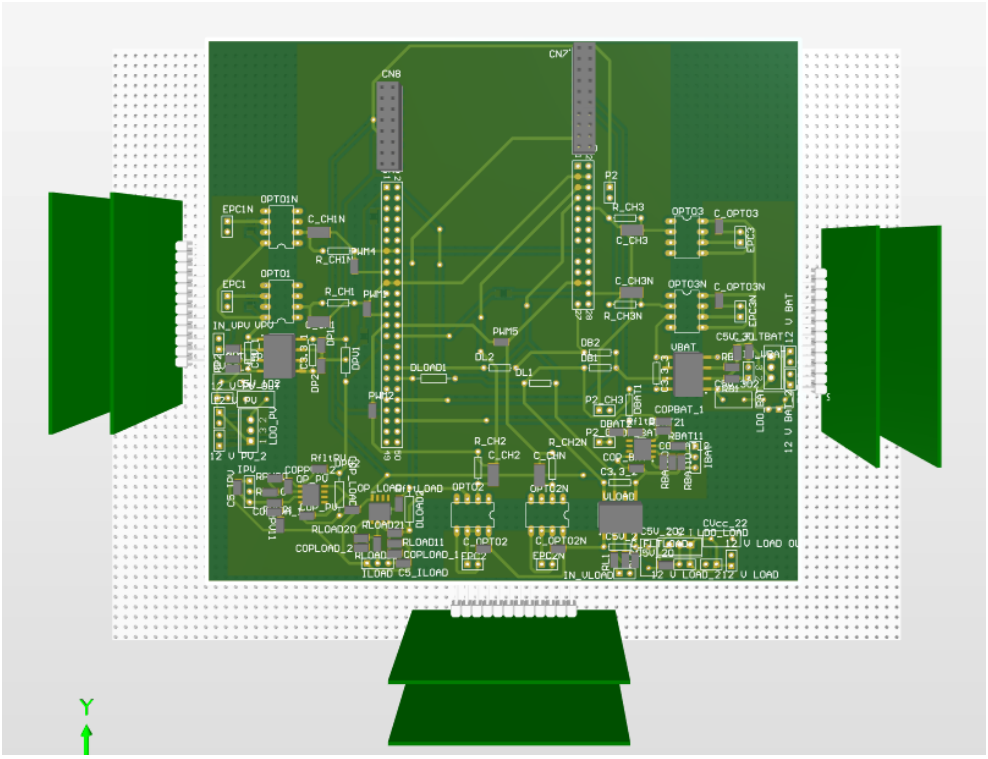

Figure B.6: TAB interface board and EPC boards 3D representation.

Appendix C

Smart Plug and Active Load: Circuit Schematic and PCB Layout

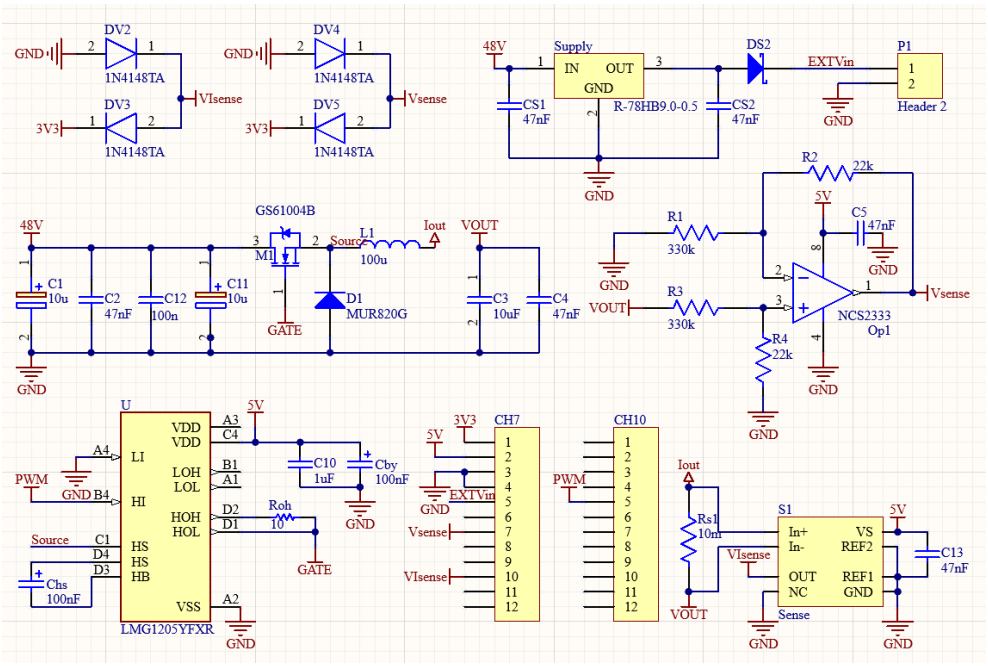

Figure C.1: Smart Plug buck converter schematic.

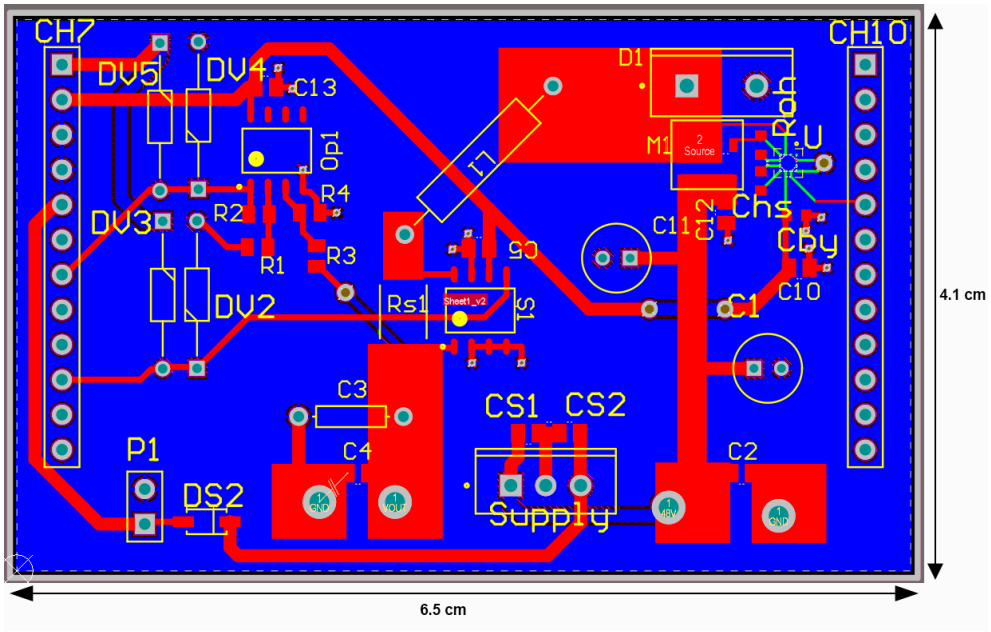

Figure C.2: Smart Plug buck converter board layout.

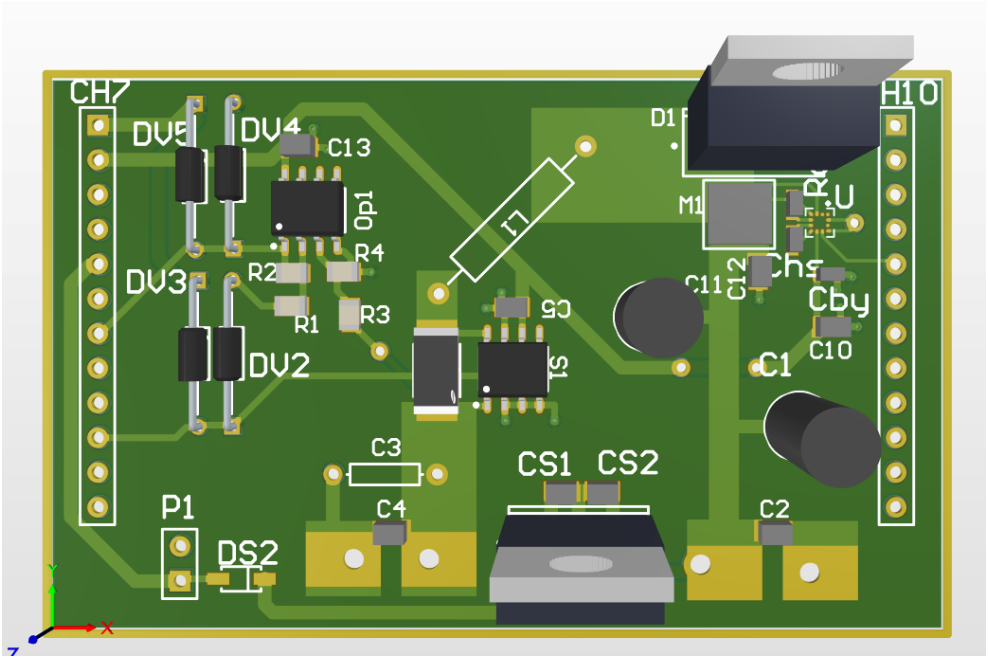

Figure C.3: Smart Plug buck converter board 3D representation.

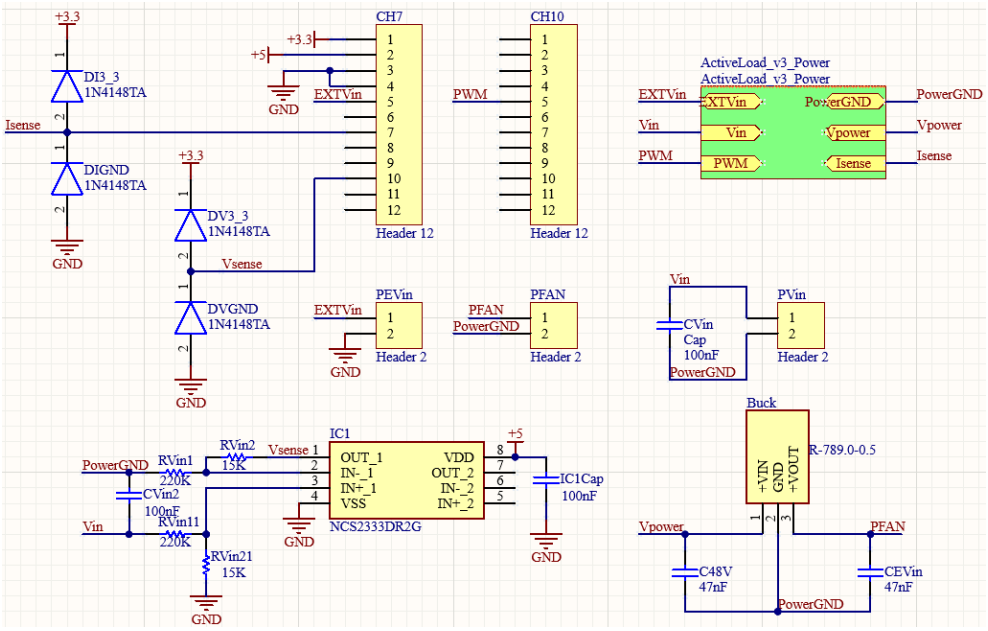

Figure C.4: Active Load connectors and power circuit sheet entry schematic.

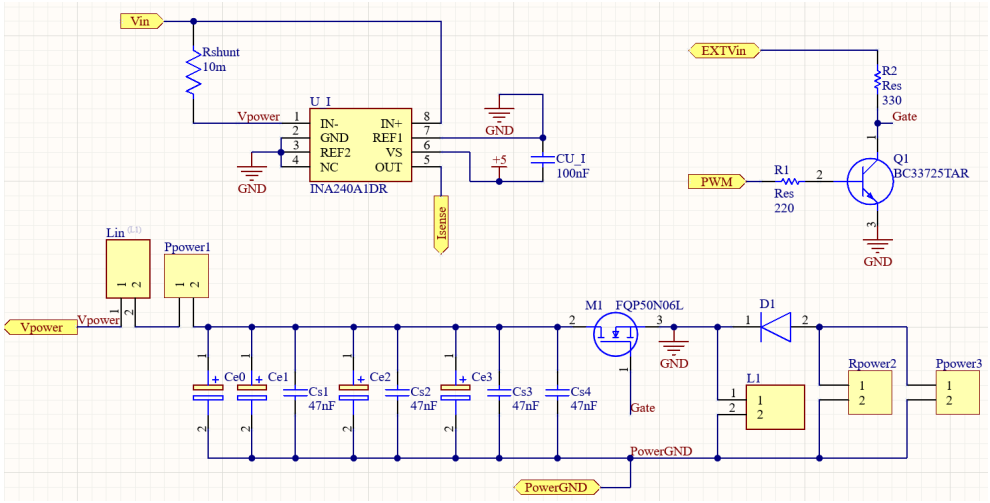

Figure C.5: Active Load power circuit schematic.

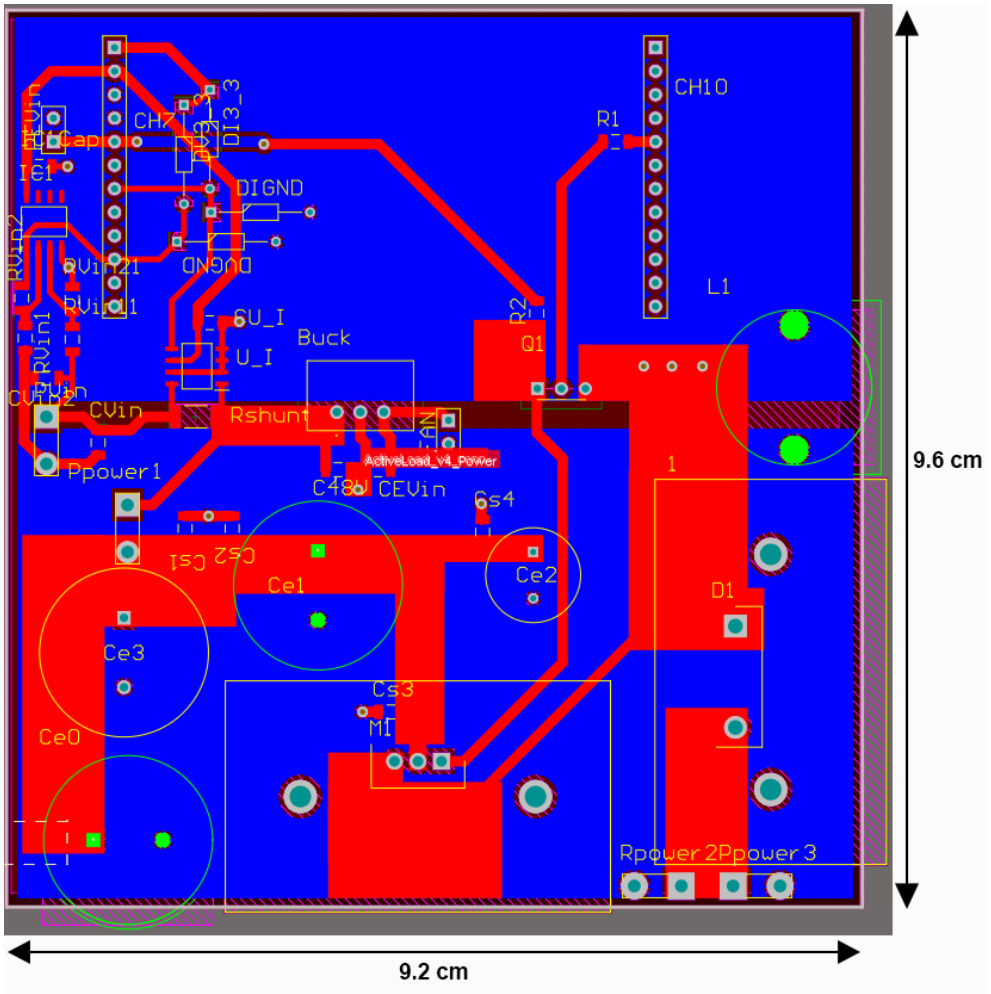

Figure C.6: Active Load board layout.

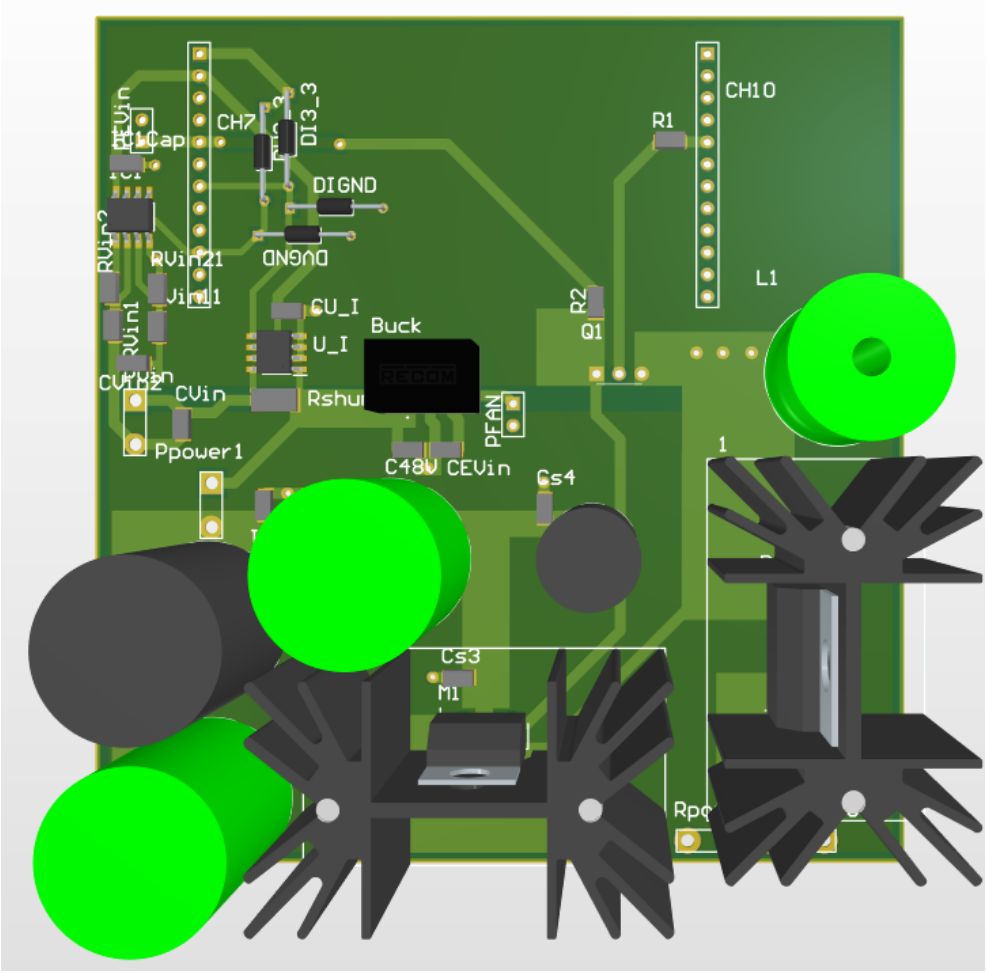

Figure C.7: Active Load board 3D representation.

Appendix D

Soiling Sensor: Circuit Schematics and PCB Layouts

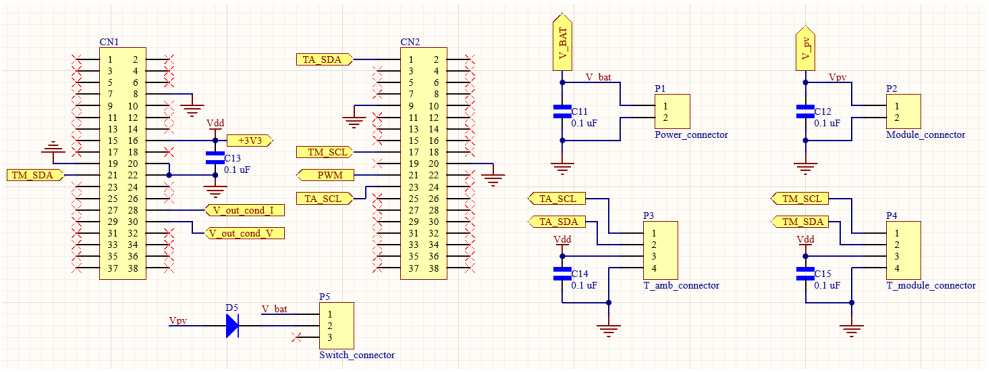

Figure D.1: Soiling sensor connectors schematic.

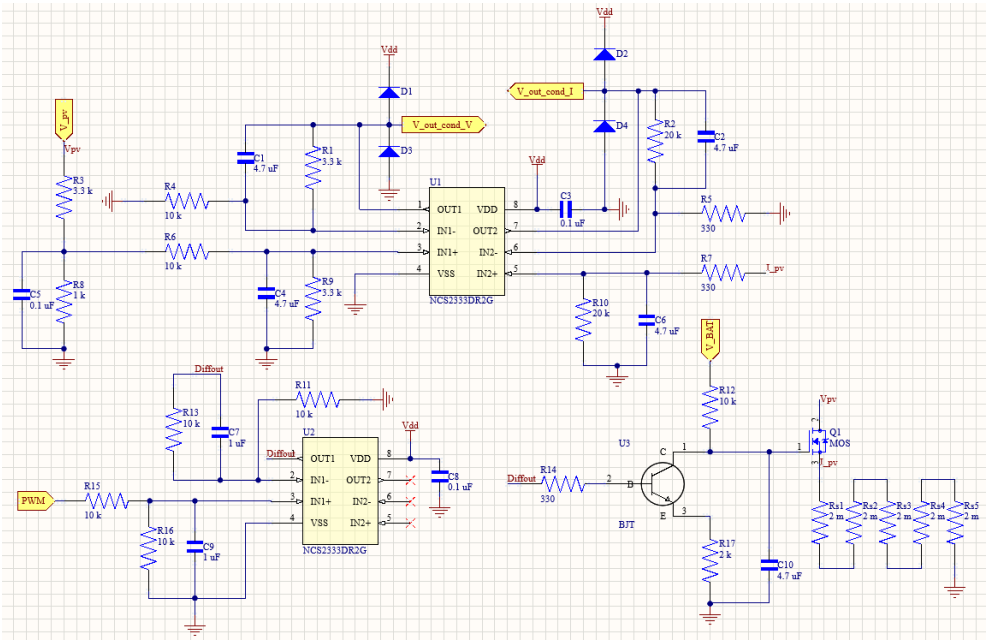

Figure D.2: Soiling sensor voltage and current conditioning schematic.

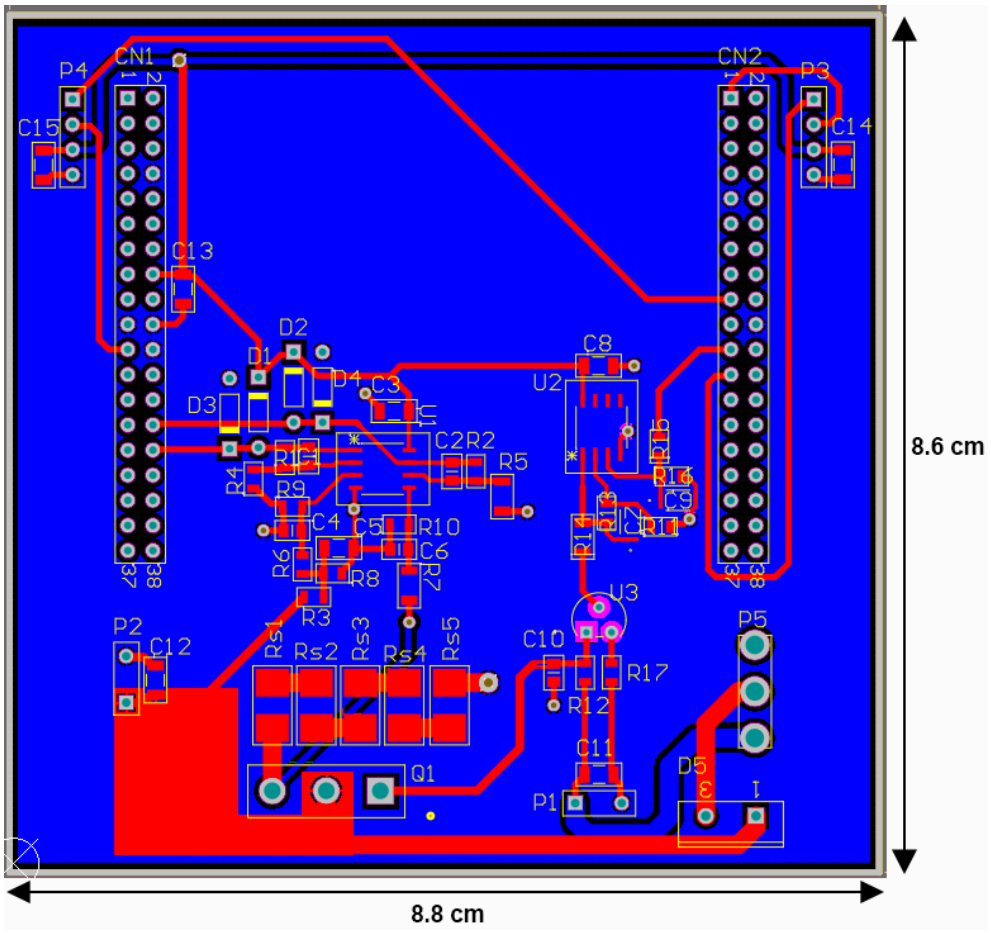

Figure D.3: Soiling sensor board layout.

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