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XXX Ciclo

ACTIVE GATE DRIVERS AND WIDE BAND-GAP DEVICES: ARCHITECTURES, APPLICATIONS AND LIMITS

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Alla mia famiglia
di oggi e di domani.

Sommario

L'elettrificazione si sta diffondendo costantemente, persino in ambiti finora dominati da altre forme di energia. Uno dei mercati più importanti è quello dei trasporti, dove si può osservare una tendenza verso aerei, navi e veicoli elettrificati. L'elettronica di potenza gioca un ruolo chiave nel supportare questa evoluzione. Le applicazioni richiedono convetitori ad alta efficienza e affidabilità, controllati da algoritmi ad alte prestazioni.

In questo lavoro si è studiato l'uso efficace dei dispositivi wide band-gap, specialmente MOSFET SiC, rivolgendo l'attenzione ai nuovi requisiti che questi pongono per il loro pilotaggio. Dopo un'immersione nello stato dell'arte dei gate driver attivi (AGD), sia per dispositivi al silicio che in altri materiali, nuove architetture sono state sviluppate e valutate.

La possibilità di controllare finemente le forme d'onda ha suggerito di utilizzare gli AGD per migliorare l'affidabilità e il tempo di vita dei convertitori di potenza. La seconda parte del lavoro si occupa quindi di controllo termico attivo (ATC): il gate driver può essere sfruttato per determinare la potenza dissipata dal dispositivo e, incrementandola in condizioni di basso carico, la temperatura del dispositivo stesso può essere controllata. Poichè i cicli termici sono noti per essere una delle principali minacce per l'affidabilità, ATC dovrebbe migliorare il tempo di vita sia del dispositivo che dei convertitori.

Per supportare e implementare ATC, diversi modelli di perdite sono stati progettati e analizzati, considerando, oltre alle prestazioni numeriche, anche il tempo necessario per lo sviluppo e la messa a punto degli stessi. Nell'ultima parte del lavoro, differenti tecniche ATC sono state implementate, provate e confrontate, sfruttando figure di merito sviluppate allo scopo.

I vantaggi e gli svantaggi delle differenti tecniche sono stati esplorati e la tecnica di ATC per shoot-through si è rivelata altamente promettente, in quanto può forzare perdite praticamente costanti sul dispositivo, indipendentemente dalle condizioni di carico, persino in caso di conduzione per ricircolo.

Il lavoro è lontano dall'essere completo: occorre studiare diversi dispositivi, l'affidabilità del gate driver stesso deve essere determinata, gli effetti sulla temperatura di giunzione studiati in profondità, il miglioramento di affidabilità deve essere quantificato e il compromesso fra efficienza e affidabilità deve essere studiato.

Abstract

Electrification is spreading constantly, even in areas usually led by other forms of energy. One of the most important markets is transportation, where a trend towards more electric aircraft, ships and vehicles can be seen. To support this evolution, Power Electronics plays a key role. Applications demand high-efficiency and high-reliability power converters, governed by high-performance control algorithms.

In this work the effective use of wide band-gap devices, especially SiC MOSFETs, has been studied, paying special attention to the new requirements that these devices set for their driving. After a deep dive into the state of the art of Active Gate Drivers (AGDs), for both silicon and new-material devices, some new architectures have been developed and benchmarked.

The possibility to finely control the switching waveforms suggested to take advantage of AGDs to improve reliability and power converter lifetime. The second part of the work deals with Active Thermal Control (ATC): the driver can be exploited to determine power loss and, increasing it in low load conditions, the temperature of the device can be controlled. Since thermal cycling is known to be one of the most important threats for realiability, ATC should improve device and system lifetime.

To fully support and implement ATC, different loss models were devised and analyzed, taking into account not only their numerical performance, but also the effort needed to tune them. In the last part of the work, different ATC techniques were implemented, tested and compared, taking advantage of figures of merit developed on purpose.

Limitations and benefits of the different techniques were found and the shoot-through ATC technique turned out to be highly promising, since it can determine almost constant power loss on the device regardless of its load condition, even in case of free-wheeling conduction.

The work is far from being over: different devices should be studied, the gate driver reliability should be assessed, the effects on junction temperature shuld be studied in depth, the reliability improvement should be quantified and the reliability-efficiency trade-off determined.

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Introduction

Electrification, interpreted as the process of shifting to electrical energy to fulfill the needs of society, is widely recognized as one of the greatest achievements of the 20th century [1]. This surely is true, but it is also a fact that electrification is not a feature of the past century alone. In recent years, two important directions are followed: pushing electricity in non-industrialized countries [2] and improving quality and efficiency in those that are already electrified [3, 4].

Looking at the first scenario, the driving force is efficiency improvement at low operating and assembly costs, in order to improve the quality of life in those areas where electricity is not yet available. Here battery-powered systems are often used, sometimes as part of mobile units, so volume and power densities become important constraints, too. This is the area where high-density power converters, especially low-power ones, find their natural habitat: the Google Little Box Challenge raised a lot of interest from research in order to push the limit of power density for domestic, low-power appliances [5, 6, 7, 8, 9].

Already electrified countries, even if urging towards better static power conversion for small and medium size equipment, are also trying to electrify mobility on ground [10, 11], sea [12] and air [13]. There are multiple reasons to do that: reducing the cost of personal and collective mobility, better fuel and energy efficiency, improved comfort for passengers and reduced environmental damage.

This “secondary electrification” relies on already existing converter architectures and device types, but some new technological trends allow to improve the system performance. The first boost comes from the possibility to use new semiconductor

materials to develop the same types of devices of the past, but with increased performance. Wide Band-Gap (WBG) materials, such as Silicon Carbide (SiC) and Gallium Nitride (GaN), breathe new life in the electronic power switches scenario, either in the form of traditional types of devices (MOSFETs, BJTs, JFETs), or for new and uncommon ones (HEMTs, Cascode configurations) [14, 15].

Another technological improvement is related to the availability of better control architectures and more powerful tools: low-cost FPGAs, hardware-in-the-loop (HIL) and automatic code generation all contribute to implement more complex control algorithms and architectures, such as Modular Multilevel Converters (MMCs) and multiport converters (DABs, TABs, QABs) [16].

In this world where new technologies and tools are available and compelling energy problems exist, most of the research interest is devoted to the integration and optimization of different parts, to migrate perspective advantages into real-world ones. This is the reason why well-established parts and components of power converters and systems are experiencing substantial remodeling or even completely new design.

From this point of view, Active Gate Drivers (AGDs) are a relevant enabling technology. Rooted in the first concept of "grid driver" of the Fifties [17, 18], the idea of a dedicated circuit to drive the control terminal of an electronic device used as switch [19] has a long history. Except for some diagnostic features, the basic concept behind base and gate drivers has never changed: amplify the signal coming from the control circuit, to ensure proper switching.

AGDs broaden this idea, adding control to the power of the driving signal: more parameters, such as switching time or waveform time derivatives are considered and possibly managed actively. Of course it leads to more complex driver circuits, but simultaneously it allows exploitation of high-level features of modern WBG devices.

Switching parameters are not the only ones deserving attention: AGDs can also determine losses and have important effects on system performance from the reliability, efficiency and density point of view. This is why many Active Thermal Control (ATC) techniques rely on specialized gate drivers, and often embed also advanced measurement and diagnostic features.

This thesis focuses on some of the aspects related to the interaction of WBG

devices with AGDs. After some introduction about WBG parts and types, existing AGDs are presented and compared to conventional ones. Then, newly developed circuits belonging to this category are described and experimental data is presented. Since most of the PhD program concentrated on the thermal optimization of WBG device switching performance, loss models are presented and discussed, as a prerequisite for the implementation of different device-level ATC algorithms. Advanced notions about optimal ATC design are presented, together with the research topics that this thesis was not able to cover.

Chapter 1

State of the art in power conversion components

Motion or change, and identity or rest,
are the first and second secrets of nature.

– R.W. Emerson, 1844

Nowadays, the trend for electronic converters is in high power density. Higher switching frequencies, smaller magnetic components, reduced losses to shrink the cooling system are the key marks of modern static power conversion. Nonetheless, lack of lifetime is still cause of reluctant embracing of electrification in high-reliability markets. These two factors, together with ubiquitous cost effectiveness, are the drivers for the development of new technologies for power conversion.

High density and high reliability are pursued focusing research on various aspects of power converters. New control algorithms and modulations can relieve stress on the devices, while improved architectures can reduce unevenness in strain for components, also enabling the use of smaller passives. However, technological exploration in device design and manufacturing can still deliver significant improvement on both sides. This chapter focuses on the state of the art of electronic power switches, both in silicon

and WBG materials. Their internal structure is described and their features from the functional perspective highlighted, in order to support the discussion further.

1.1 Modern silicon devices

Silicon technology has been developed for many decades and it is still fueling the power semiconductor market [20], regardless of signals of approaching silicon limits in other areas, such as electronic logic [21].

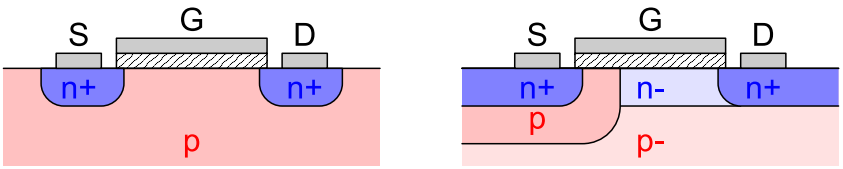
New products are constantly developed in the effort of converging to the theoretical limits of semiconductor materials, and new ones are explored, too [22].

1.1.1 MOSFETs

The origin of the MOSFET device dates back in a remote past, appearing for the first time in 1933, as described in [23]. This invention did not find rapid adoption in the mass market, and major advancements in the MOS technology were carried out mainly in the Sixties. After this initial development, the MOSFET device scenario has seen many improvements, that still continue today. This makes this kind of device still widely used, especially due to its mainly square Safe Operating Area (SOA), high-frequency switching behavior, fairly low on-state resistance, possibility to reverse conduct and to work as a synchronous rectifier.

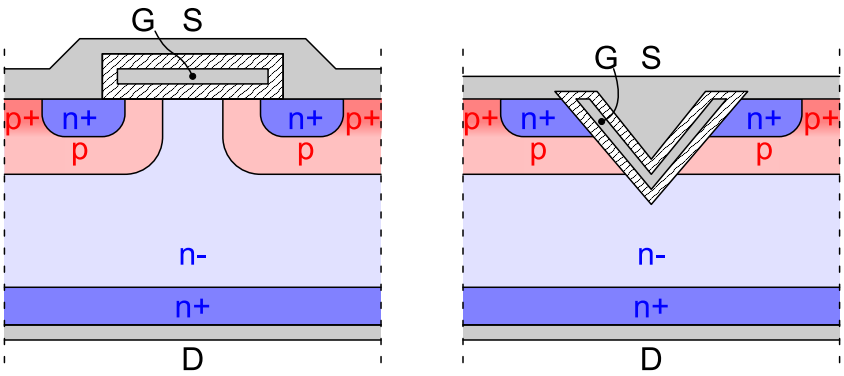
The basic architecture of a planar MOSFET, historically devised first and reported in Figure 1.1a, has evolved into the double diffused MOS (DMOS, see Figure 1.1b), that is capable to withstand higher off-state voltages. The possibility to handle even larger voltages has been made possible by the adoption of the vertical structure, that accommodates larger drift regions; this principle is evident in Figure 1.2a, showing the well-know vertical double-diffused MOS (VDMOS).

This layout was then improved by moving the channel, in order for it to be arranged vertically, thus allowing shorter carrier paths and even better on-resistance behavior. This was adopted firstly in V-groove MOSFETs, and then systematized by the introduction of the Trench MOSFET (depicted in Figure 1.2b and 1.2c, respectively) [24].

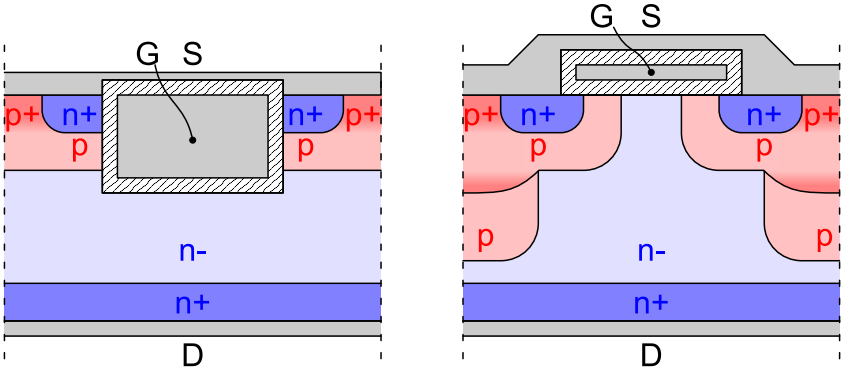


(a) Planar (signal) MOSFET. (b) Double diffused MOSFET.

Figure 1.1: Simplified structures of MOSFETs in planar technology (drawings not to scale).



(a) Vertical diffused MOSFET. (b) V-groove MOSFET.



(c) Trench MOSFET. (d) Superjunction MOSFET.

Figure 1.2: Simplified structures of different power MOSFET device types (drawings not to scale).

However, it is in the late Nineties that the device performance undergoes a major advancement, with the application of the charge-compensation principle and its adoption in the so-called Superjunction MOSFET (SJ) [25, 26, 27]. The introduction of p-type pillars (see Figure 1.2d), giving the electric field in the drift region a squared shape, allowed to break the bond between blocking voltage and on-state resistance, outperforming previous technologies [28].

These arrangements where developed further in the last decades and adopted from different silicon providers under various names: Infineon's CoolMOS and ST's MDmesh are SJ MOSFETs, while Trench MOS layouts are used in Infineon's OptiMOS and StrongIRFET, while Vishay markets its devices under the TrenchMOS brand name. Also other features received specific names: Infineon's HEXFETs are usually Trench MOSFETs with a hexagonal cell structure, in order to use better the available surface of the die.

Despite their almost square SOA, MOSFET short circuit capability is often limited to few microseconds, that is typically lower than the available detection time for short-circuit protection circuitry [29]. In [30] it was found that superjunction MOSFETs can withstand fairly long short circuit times (around $4\mu s$) without any damage, mainly due to their high active volume. However they are far from typical IGBT values, that can be almost one order of magnitude larger [31].

As it can be understood looking at MOSFET layout structures in Figure 1.2, the vertical devices embed an intrinsic diode, resulting from shorting the base junction of the parasitic npn-BJT. This can be an advantage in those applications where free-wheeling path for inductive load currents is needed. What usually happens is that due to the doping profile used for the drift region, the on-state voltage is high and reverse recovery performance bad. Some efforts were adopted in order to improve the performance of this integral diode, to avoid the need for external components, with benefit from the power density point of view [32].

Understanding body diode performance and functionality is really important, because it shares the very same active material of the main MOSFET device. This has two implications, that will be really valuable in the following: diode conduction can result in losses that heat the MOSFET part, and the diode can be used as a junction

temperature sensor, provided that the current flowing through it is known.

1.1.2 IGBTs

MOSFET devices exhibit a structural trade-off between on-state losses, switching speed and blocking voltage, as it is clearly shown by numerous figures of merit in literature [24]. This poses a limit in the adoption of power MOSFETs in some application areas, especially if moderate switching speed is needed together with high power handling capability. This restriction is mainly related to the fact that MOSFETs are majority carrier devices, so the resistance of the drift region is mainly governed by its thickness and doping.

In the Eighties, many efforts were made in order to add voltage control to a bipolar device, or, the other way around, to include conductivity modulation to voltage-controlled devices. This was first patented by Becke and Wheatley [33], and then developed further by Baliga and others [34, 35]. The Insulated Gate Bipolar Transistor (IGBT) is the most widely used name today to address this kind of devices.

The device structure has many similarities with that of the vertical MOSFET, and different geometries for IGBT can be obtained by substitution of the n-doped buffer layer of the MOSFET with a p-doped layer (see Figure 1.3). This supplementary junction has many consequences on the device behavior. First and foremost, it injects minority carriers when it is forward biased, thus realizing conductivity modulation. Then, since it has to be forward biased in order for the device to conduct, a threshold voltage appears in the forward characteristic of the IGBT, whereas it is absent in the MOSFET. Thirdly, it makes the device unidirectional, at least theoretically, as it will be discussed later. Lastly, it transforms the parasitic BJT of the MOS in a parasitic SCR, that has to be forced in the off-state in order to avoid latch-up and device uncontrolled operation.

As stated before, the junction on the collector side of the IGBT makes the device unidirectional. This is not practically true: since the drift region is left floating, it is generally biased by parasitic effects acting at the limits of the active area of the die. This behavior is undesired, since it frustrates the effective reverse blocking capability of the device. In order to retain this, a special making is needed for the end sections

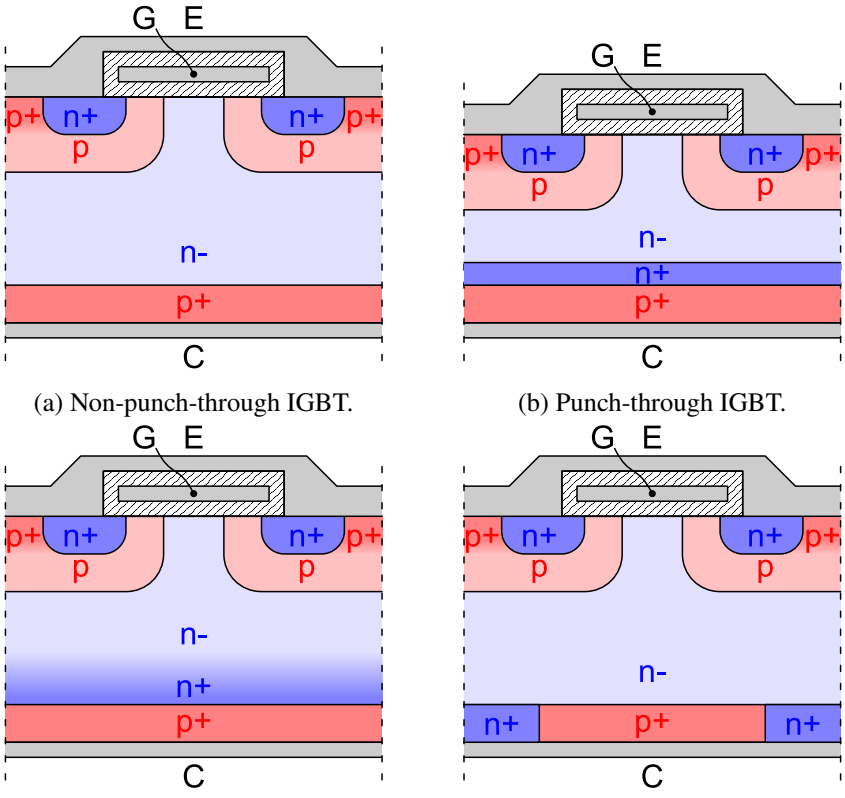
of the die. With this expedient, it is possible to have symmetrical blocking capability; this is the *reverse-blocking IGBT* and it finds application for example in matrix converters, where embedding the diode in the controlled device can result in some loss improvement [36]. On the other hand, since the integral diode of the MOSFET is not available anymore in the IGBT structure, efforts were made to restore the *reverse-conduction* capability. This is accomplished by the substitution of part of the p-doped injection layer with n-type material. The addition of n-type doping below the p base region can help in controlling the carrier lifetime and thus the dynamic performance of the diode. Figure 1.3d gives pictorial representation of this arrangement [28].

Another common categorization of IGBTs is that related to the design of the drift region near to the injection layer; three different possibilities are grouped in Figure 1.3. The *Non-Punch Through IGBT* (NPT-IGBT) has almost constant doping concentration throughout the entire height of the drift region, resulting in a triangular shape of the electric field in the forward-blocking region. Thinner devices can be made if a square-shaped electric field arrangement is forced by the introduction of a n+ buffer layer near to the injection one, obtaining the *Punch Through IGBT* (PT-IGBT); loss behavior is generally improved, but short-circuit and reverse blocking capabilities are usually hindered for PT devices [37]. To mitigate these negative aspects and to amplify the positive ones, the *Fieldstop IGBT* (sometimes marketed as "Trenchstop IGBT") was devised, exhibiting a non-uniform doping, increasing towards the injection layer (see Figure 1.3c).

One point of interest for the following is that differently from what usually happens with MOSFETs, IGBTs are often co-packed with a discrete diode. The resulting part behaves as a reverse conducting IGBT, no external diode is needed, but of course two devices are involved, rather than one. This will have significant impact in the loss distribution and device performance; this issue will be addressed in the following.

1.2 Wide band-gap devices

Silicon is a well-known material, which technologies are established and qualified. In the modern electronic era, silicon has been the material of choice for logic, analog and



(a) Non-punch-through IGBT.

(b) Punch-through IGBT.

(c) Fieldstop IGBT.

(d) Reverse-conducting IGBT.

Figure 1.3: Simplified structures of different IGBT device types (drawings not to scale).

Table 1.1: Physical parameters for some semiconductor materials [39].

	Bandgap eV	Electron mobility $cm^2/(Vs)$	Critical field kV/mm	Thermal conductivity W/(Km)
Si	1.12	1400	30	130
Ge	0.661	3900	10	58
GaAs	1.424	8500	40	55
GaN	3.44	900	300	110
3C-SiC	2.36	300-900	130	700
6H-SiC	2.86	330-400	240	700
4H-SiC	3.25	700	318	700
Diamond	5.5	2200	570	600-2000

power devices, fueling the advance of human activities. During the years, this pushed the research to approach the theoretical limits of the material, posing an upper limit to device performances. Already in the Eighties, many scientist were aware of this issue, and they tried to find new materials that could help in overcoming silicon limitations [38]. The outcomes of these studies foresaw potential solutions in the so-called *wide band-gap* (WBG) devices and materials. These parts owe their name to the magnitude of the energy gap between valence and conduction bands, that is comparably high with respect to that of silicon and, incidentally, also to the germanium one.

Table 1.1 shows the comparison of some semiconductor materials that are known to be suitable for the manufacturing of electronic devices. As it can be seen, energy gap is not the only parameter of interest. From the power electronics side, also critical field and electron mobility are very important, while thermal conductivity becomes interesting with respect to device packaging and assembly.

The possibility of these materials to handle higher electric fields allows to manufacture devices that can withstand breakdown voltages similar to those in silicon, but with significantly reduced dimensions, paving the way to higher power densities. Benefits can arise also in other areas, as different figures of merit can show. Figure 1.4

and 1.5 show the on-resistance vs. breakdown voltage and gate charge vs. on-resistance figures of merit (FoM) for different materials and research and industry results: it is clear how WBG devices can outperform traditional, silicon, ones.

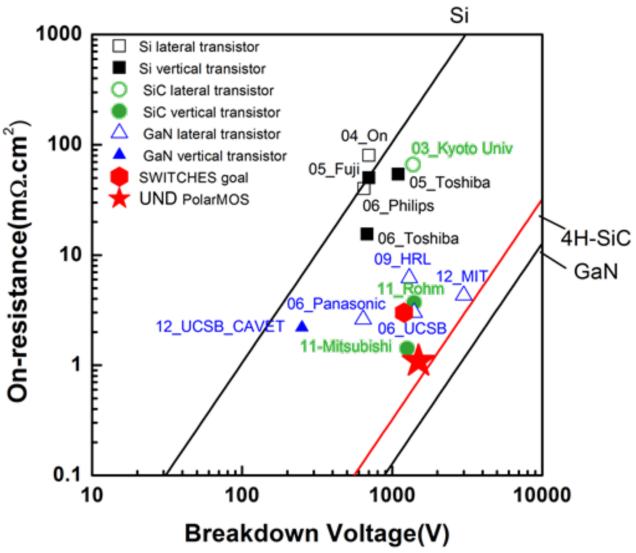
As it always happens when new technologies appear on the scene, good points are easier to be appreciated than the negative ones, that should be accounted anyway. For widespread adoption of WBG devices in large-scale production, cost is nowadays the main obstacle. The new materials, requiring ad-hoc technologies, make costs skyrocket with respect to silicon. The device increased cost can be made affordable if savings are possible elsewhere; two important points are the viable reduction of passive components costs, related to the possible increase in switching frequencies, and overall system performance improvement, provided that capabilities of WBG can be fully exploited.

Moreover, many WBG materials are not as easy as silicon to be supplied. It is also true that some technical issues for these components still exist, mainly related to the accuracy needed for the manufacturing process, device instability and the related reliability limitations. Surely, today many WBG parts are commercially available and other ones are in development status, and this encourages power electronics research to account for them and their peculiar characteristics.

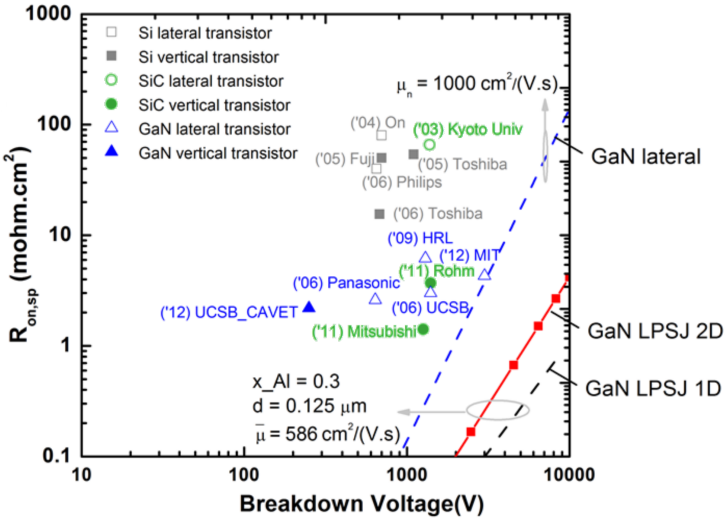
The desire to take advantage of these materials also encourages new approaches to power conversion, to address the material cost issue with remarkable performance improvements. The Active Thermal Control discussion presented in this work is one of the efforts in this direction: WBG are strong drivers, so the work starts from them, but positive consequences are expected also for older yet well-established technologies.

1.2.1 Silicon carbide MOSFETs

One very common device in Silicon Carbide (SiC) material is the MOSFET. Basically, it shares the same layout of the vertical silicon MOSFET, even if new stacking structures are being developed. The qualitative behavior of SiC-MOSFETs is very similar to that of Si counterparts, but some differences are noticeable. Firstly, given a breakdown voltage, SiC parts have lower on-state resistances, thus allowing higher current capabilities; often they also exhibit improved transconductance. An important



(a) Silicon, SiC and GaN compared.



(b) GaN detail.

Figure 1.4: Specific on-resistance as a function of breakdown voltage [40].

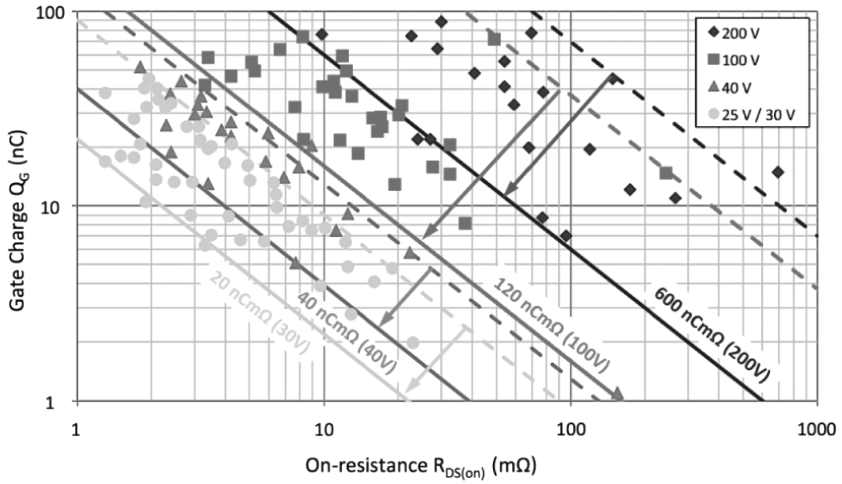


Figure 1.5: Total gate charge vs. Specific on-resistance [24].

characteristic is the temperature behavior of the on-state resistance with respect to the gate voltage: for SiC-MOSFETs it is common to have a zero-temperature-coefficient (ZTC) gate voltage below which the $R_{ds,on}$ has negative temperature coefficient (NTC) and positive behavior (PTC) above. This is important when paralleling multiple devices: only PTC behavior guarantees proper negative feedback and current sharing [41].

Despite originating from the same doping profiles and zones, the fact of using different material makes the body diode behavior radically different between Si and SiC. Performance is generally better for silicon-carbide devices: the body diode threshold behavior can be effectively avoided if the gate voltage is held above the cut-off value, allowing good synchronous rectification and symmetric loss behavior, with respect to the switched current. Moreover, the SiC body diode is usually softer that the silicon one, reducing reverse recovery losses in half-bridge configurations.

The considerations above substantially draw many similarities between standard silicon devices and modern SiC counterparts, differences laying mainly in the quantitative side. The recommended gate voltages follow the same trend. Because of the non-monotonic temperature coefficient of the on-state resistance at low gate voltages

and to get the most linear behavior for the body diode, SiC MOSFET manufacturers usually suggest voltages that are slightly higher than those of silicon, often in the range from 18 V to 20 V. Turn-off voltages are usually negative, to account for the relatively low gate threshold, its temperature change and to accommodate enough margin against the Miller effect, due to the high voltage derivatives that these devices are capable to determine. Lower voltages, typical for Si-IGBTs (such as −15 V), are usually avoided not to damage the gate oxide in the long term [41].

1.2.2 Gallium nitride HEMTs

Gallium nitride is a WBG material that is gaining large interest, mainly due to its high theoretical possibilities that, thanks to the technological advancements, make them also affordable, up to a point where GaN commercial power devices are available on the market. First GaN devices were normally-on, i.e. without gate bias they were able to conduct current. This behavior is greatly undesired in power converters for safety reasons.

The most interesting GaN devices available today are High Electron Mobility Transistors (HEMTs), based on a AlGaN/GaN heterostructure. These devices are lateral, but they allow to achieve MOSFET-like characteristics without the need for device doping, particularly difficult in GaN, where p-doping is not easily obtained. The interesting performance of this lateral structure is determined by the appearance, at the heterojunction, of the so called two-dimensional electron gas (2DEG), that ensures very high electron mobility, without demanding dopant concentrations.

The resulting device is radically different from MOSFETs, despite exhibiting similar overall characteristics. Since the gate is separated from the channel by AlGaN, that is not a proper insulator, high current leakage is noticed, appearing as a static gate current in the order of some milliamperes.

On the other side, parasitic capacitances are very low compared to other kinds of devices, resulting in very fast switching performance. For what concerns the body diode, it is absent due to the lateral structure of the device. However, the device has bidirectional current capability, similarly to traditional MOSFETs: if the gate voltage is above the threshold, symmetrical behavior to that achieved in the forward

direction is seen; if the gate bias is negative, the reverse conduction is possible and the *drain* voltage goes below the source potential. This can be seen in the current-voltage characteristic as a body-diode-like behavior, with slightly higher voltage drop but no reverse recovery, due the lack of injection mechanisms.

GaN devices exhibit very fast switching performance, so they need special packages, not to see their excellent behavior canceled by package parasitic inductances. This is why traditional TO-series chip carriers, widely used in silicon and silicon carbide as well, were dropped for GaN, in favor of new, custom, surface mount, bond-less packages.

1.2.3 Other types of WBG devices

The extensive interest of research in WBG materials and devices has led to the development of many other parts, that have not obtained such a large interest as SiC MOSFETs and GaN HEMTs, but that are interesting and worth nothing anyway, especially recalling that all these technologies are young and still liable of major improvements.

Silicon carbide bipolar junction transistors (SiC BJTs) derive from the traditional BJT, but employ the new material. This allows to overcome or attenuate some of the problems of silicon power parts: mainly high-current gain drop and secondary breakdown. In fact, SiC BJTs perform usually better from this point of view, and many manufacturers are pushing these products. The main limitation is in the static power requirement for the base driver, that can at least get some benefits from the higher β made possible by SiC.

The very first silicon carbide component to be developed was the JFET. This allowed to tune the technology, and these devices are still marketed today, despite their many drawbacks. Since it is a normally-on device, in order to operate it safely in power circuits, it is usually employed in cascode configuration together with a high-speed silicon MOSFET (see Figure 1.6). Since the high voltage during the off state is sustained by the JFET, the MOSFET can be chosen with a low voltage rating, ensuring not to degrade the WBG performance. Of course the switching speed is limited by the MOS behavior, but many believe that still net advantage is possible

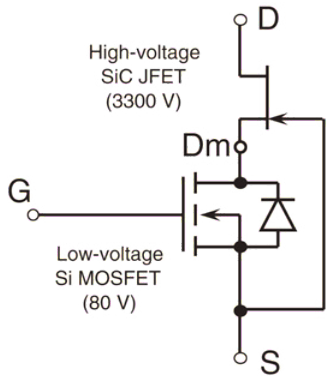


Figure 1.6: Cascode architecture to achieve normally-off behavior with SiC JFETs [46].

with respect to full-silicon components.

The invention of the IGBT in the silicon world, as already stated in Section 1.1.2, allowed to overcome some of the limitation of MOSFETs, namely on-state losses and voltage handling capability. The same relationship can be expected in silicon carbide, except happening at higher voltages and currents, as clearly pointed out in [42]. Since the voltage where SiC MOSFETs and IGBTs can compete lays in the 15 kV zone, the latter is expected to find market and use mainly in medium- and high-voltage applications.

GaN power devices other than enhancement-mode HEMTs exist; the most common and already marketed one is the depletion-mode HEMT. As it happens for SiC JFETs, these devices are used in cascode configuration with a silicon MOSFET, in order to present normally-off behavior. In literature efforts to develop bipolar devices [43], as well as a true MOSFETs [44, 45] exist, but none of them has attracted enough interest to achieve widespread adoption. There are still many difficulties in the doping process of GaN, and in the side effects arising from naive solutions used for the purpose.

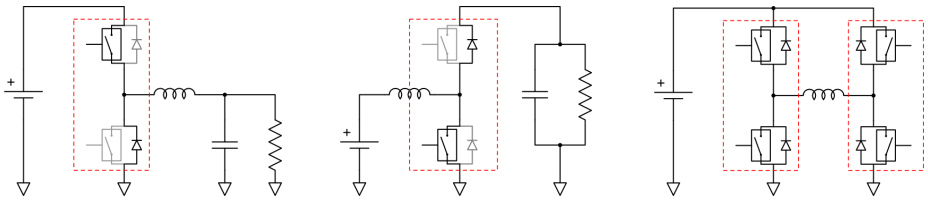
1.3 Gate drivers

In this section, some assumptions and conventions adopted in the following will be described. At the end of the chapter the state of the art for gate drivers will be examined.

Achieving optimal performance from modern power semiconductor devices can be accomplished by using an accurate management of the control terminal (be it a base or a gate). Modern gate driving circuits are targeted at providing facilities not only to switch the power device on and off, but to control and protect it under different situations.

The desired features range from propagation of the command from control unit to the power device, with minimum delay and jitter; the control unit should not be excessively loaded, but enough power to drive the main switch is needed, also under different load and fault conditions. The gate driver should also provide electrical insulation among neighboring devices and other circuit components, limiting damage in case of failure of power lines or hardware parts. Limiting $\mathrm{d}v/\mathrm{d}t$ and $\mathrm{d}i/\mathrm{d}t$, in order to control the harmonic content of the generated waveform is desired, as well as EMI control. Moreover, in most advanced designs, some other features can be added, such as: adjust delay and commutation times in order to control switching energy and device temperature, adjust the device equivalent on-state resistance to determine conduction losses, automatically adjust the dead-time, to provide a low distortion output waveform, but preventing *shoot-through* of the DC source in bridge topologies. Looking at protection features, the gate driver should detect failures as fast as possible and bring the device in a safe state, reporting what kind of error triggered the protection.

These features are of major importance not only for new converter architectures, but for ordinary topologies as well, because they let the designer address different issues that should be otherwise dealt with more expensive circuits. A clear example is given by the problem of switching trajectory control in high power converters. In this scenario it is a common practice to use snubber circuits, but they involve passive components, implying system added cost, possible weight increase and reliability



(a) Buck converter. (b) Boost converter. (c) H-bridge converter.

Figure 1.7: Switching converters seen as composed by half-bridges.

issues. An "intelligent" gate driver could accomplish similar results but with better performance and improved reliability. The focus on reliability is of paramount importance, because this is one of the obstacles to the large scale use of Switched Mode Power Supplies (SMPS) in some context, like in aircraft or other safety-critical areas.

1.3.1 General model for converter topologies

Since a gate driver is a very general purpose circuit, that can be employed in different types of converters, the number of assumptions used to develop it must be kept to a minimum. On the other side, some simplifications have to be done, in order not to develop a circuit that is too complex. It has been noted that stacked devices, like those that are used in half-bridge topologies, can be a good model for a large variety of SMPS. This fact is easily understood for H-bridge and three phases bridge topologies, but it is true for single switch converters, too.

When only one controlled switching device is used, an uncontrolled switch is usually employed somewhere else, to provide the alternative path for current in presence of an inductive load. As it is shown in Figure 1.7, this situation can be seen as a special case of a half-bridge topology, where one of the active devices is held in the off state. This assumption is valid in many cases, because almost all active power devices include a freewheeling diode, be it intrinsic or installed on purpose [47].

In the following the analyzed circuit is always a half-bridge, with an active load, i.e. a load that can drive current independently from the voltage output of the bridge. A schematic representation of this model is given in Figure 1.8.

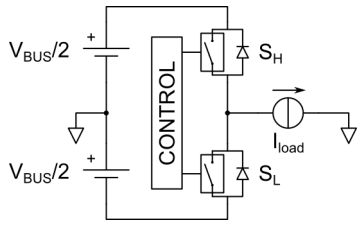


Figure 1.8: Ideal half-bridge circuit with active load, for switch states description.

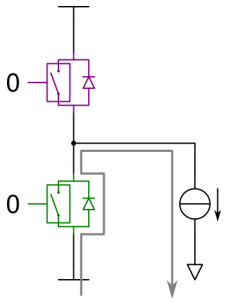
The active load is referenced to ground and the power supply is split in two parts, so that both positive and negative output voltages can be generated. Current is assumed to be positive when leaving the central node of the bridge, i.e. when it is sourcing current.

In order for the gate driver to control the power switch in all circumstances, all the possible configurations and transitions of the bridge should be examined. The two switches cannot be on simultaneously, otherwise a bus short-circuit would occur; commands can have three possible states: both switches off, high switch on and low off, low switch on with high switch off.

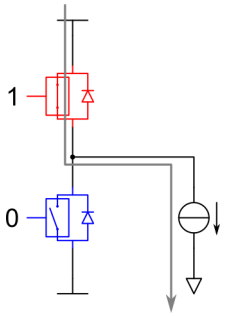
The active load can be in three different states, too. From the bridge point of view, it can force a current that is positive, negative or null. The case of null (or very low) current can rarely be sustained for a long time: it usually happens at startup (when inductances are uncharged), in presence of a high impedance resistive load or in case of unconnected output. The total number of states is nine, because each current condition can happen with each switch condition, under the hypothesis of active load. These configurations are reported in Figure 1.9, where the effective current path is highlighted in gray.

For what has been said before, it is assumed that when the output current is null, driving one switch forces current to flow based on the bridge output voltage sign; this behavior is described by the resistor that replaces the load in Figures from 1.9g to 1.9i.

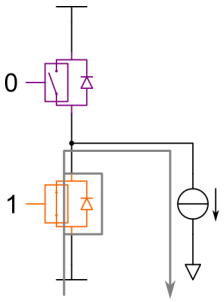
Gate driver design shall be independent of the power circuit topology; half-bridge has been chosen only as a convenience model. The gate driver design will be based on



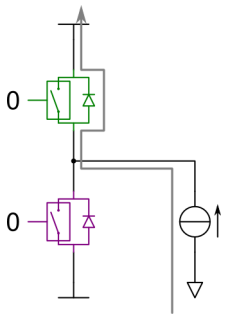
(a) Positive current, both switches off.



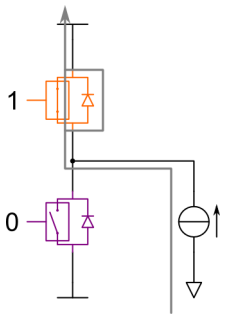
(b) Positive current, high switch on.



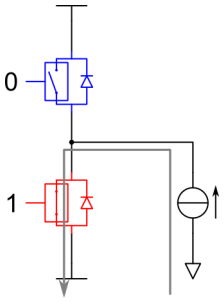
(c) Positive current, low switch on.



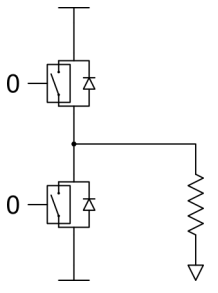
(d) Negative current, both switches off.



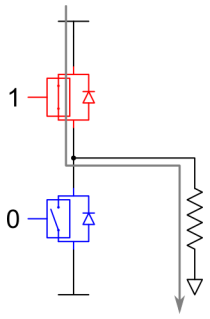
(e) Negative current, high switch on.



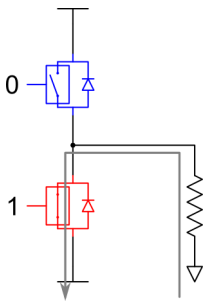
(f) Negative current, low switch on.



(g) Null current, both switches off.



(h) Null current, only high switch on.



(i) Null current, only low switch on.

Figure 1.9: Half-bridge states under different load and command conditions.

Table 1.2: Equivalent switch states, with reference to fig. 1.9. C_M is the command of the switch ('1' for on, '0' for off).

Switches	Description	Conditions
1.9b(H), 1.9f(L), 1.9h(H), 1.9i(L)	active conducting	$C_M = 1, I_d > 0$
1.9a(H), 1.9c(H), 1.9d(L), 1.9e(L)	active off	$C_M = 0, I_d = 0$
1.9c(L), 1.9e(H)	passive reverse conducting	$C_M = 1, I_d < 0$
1.9a(L), 1.9d(H)	passive diode conducting	$C_M = 0, I_d < 0$
1.9b(L), 1.9f(H), 1.9h(L), 1.9i(H)	passive off	$C_M = 0, I_d = 0$
1.9g(H), 1.9g(L)	undefined	$C_M = 0, I_d = 0$

switch states rather than on bridge states. Looking at states depicted in Figure 1.9, it can be noted that, even if there are nine of them, the possible switch states are only six (as suggested by colors). Table 1.2 shows equivalence among different switch states, providing also a "high level" description of the condition.

To understand this classification, the key concept is whether a state is active or passive. A power switch is said to be in the *active* state when a change in its control signal entails a change in the state of the surrounding circuit. Otherwise, the switch is in a *passive* state. When a device is in an active state, a transition of the control terminal causes a "hard switching" commutation of the power terminals, thus with power losses on the switch. If the device is in a passive state, "soft switching" occurs, and very low energy is wasted by the power device.

Another important concept is the *conduction* state of a switch. A power switch is said to be in the *conducting* state if its active part (i.e. the part that is controlled by gate/base terminal) is carrying current; otherwise it is in the *off* state. Even if this description seems to be trivial, it has some important implications, depending on the type of power switch used. Many power devices are unidirectional, but some of them are bidirectional. Power MOSFETs, for example, are unidirectional devices, but they can safely carry negative current (i.e. from source to drain) if they are switched on after the embedded diode is on. This principle is applied in synchronous rectification

applications, to avoid reverse recovery of power devices built-in diodes, as described in [48] and [49].

This feature is not just a possibility, but it is strongly recommended to reduce on-state losses: when a MOSFET is in the passive state, the embedded diode turns on, but switching on the MOSFET part allows lower V_{ds}, as shown in devices datasheets, like [50]. This behavior is not possible with junction based devices, like BJTs and IGBTs: datasheets do not report any reverse operating parameter [51], [52]. To be as general as possible, this state will be accounted for in the remaining part of the description. Switch states are described in Table 1.3. The undefined state is meaningful only at system startup, since it is left at the occurrence of the first transition of gate signal or load current. It can also be the reset state after a fault has been detected by the dedicated unit (see Section 1.3.2.5).

1.3.2 State of the Art in AGDs

Precise definition of the switch states can support in the creation of a FSM that can track the device behavior in real time during its operation. Different control schemes which take advantage of FSM information are possible, each of which exhibits some advantages and disadvantages. In the following, some of this control systems will be presented; they can be grouped in two broad categories: closed-loop topologies (where there is an explicit measurement of the controlled quantities) and open-loop topologies (where this measurement is not present). These considerations are somehow implicit for each Active Gate Driver, but few results are present in literature. This is the reason why the author tried to fill this gap [53].

1.3.2.1 Control FSM and fault detection

The general purpose nature of gate driving circuits calls for high level description and interfaces. From the control point of view, just two signals are needed. The duty cycle of the switch is described by a *modulation input* (C_M), that drives the switch on under some algorithm control, provided that all interlock conditions are satisfied. Another input (E) is useful to *enable* gate driving, guaranteeing safe off condition when no

Table 1.3: Description of the possible states of a switch in a half-bridge circuit.

State	Description
Active conducting	The switch is fully on and carries current in the opposite direction of the diode. Since current is flowing in the active part, the command terminal has complete control over the switching waveform. Device current corresponds to load current.
Active off	The external current has opposite direction to diode, but the active part of the switch is off. No current flows in the device, but the gate terminal can control transition to the on state.
Passive reverse conducting	Current has the same direction of diode, the device is bidirectional and the active part is driven to be on; device current flows mainly on the switch and it has opposite direction of the load current. Control terminal can only switch off the active part, but it cannot considerably move device operating point.
Passive diode conducting	Current on the device is negative, but active part is off. The control terminal can only reduce losses, switching on the active part of the device, if this last is bidirectional.
Passive off	Gate signal is off and no current is flowing in device nor in its anti-parallel diode.
Undefined	No current is flowing and both devices in the bridge are off, it is not possible to determine if a switch is active or not.

modulation is desired.

Other inputs do not come from the high-level control, but from measurement circuitry, in order for the FSM to track in which phase the switch is currently operating. To keep this circuit implementation as simple as possible, a "digital" interface has been devised. In the following, the power device used is assumed to be a MOSFET. This does not introduce any loss of generality: most of the considerations will still hold also for other kinds of devices.

In Figure 1.10, ideal switching waveforms for a half-bridge with constant current are reported. The limiting points of the operating regions are clearly defined (points *A* to *G* in the figure); to spot these points from the waveforms the following inputs to the control FSM are needed:

- Low voltage threshold flag (V_L): high when drain-to-source voltage is greater than a minimum threshold ($V_{ds} > V_{th,low}$). A positive edge on this signal means that voltage rise phase has just started.
- High voltage threshold flag (V_H), active when $V_{ds} > V_{th,high}$; A positive edge on this signal means that voltage rise phase has ended.
- Positive current flag (I_P), active when a positive current is flowing in the MOSFET, i.e. $I_d > I_{th,pos}$.
- Negative current flag (I_N), active when a negative current is flowing in the switch ($I_d < I_{th,neg}$).

Current direction is of great importance in determining if a switch is active or passive, thus identifying which device in the bridge is controlling the output switching waveforms. This is why two independent signals are used for positive and negative current: a "null current" region is created, allowing the gate driver to know when little current is flowing, and a change in sign can occur. Thresholds defined above are shown quantitatively in Figure 1.11, together with the resulting values for the described flags.

The drain-source voltage can be sensed with a resistive divider and current by a shunt resistor on device source terminal. The measured signal is then compared to

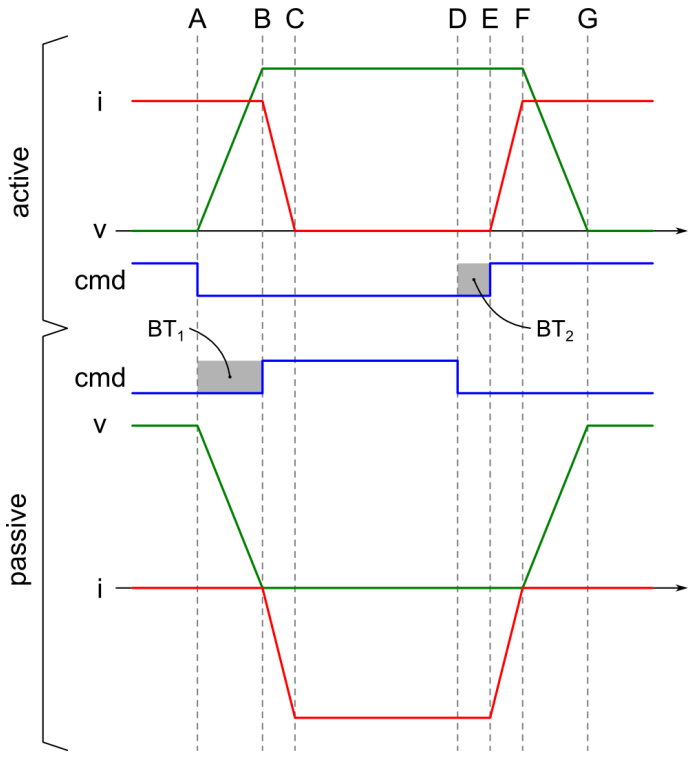


Figure 1.10: Ideal half-bridge switching waveforms with blanking time: voltage (green), current (red), command (blue). Neither delay time, nor stray inductance, nor diode reverse recovery are considered.

a threshold by a high speed comparator and the resulting flags are the inputs to the control logic implementing the FSM.

The most important signal that is output from the control FSM is the gate driving level. Controlling the switching device in different phases requires a special circuit to convert the level signal to a correct gate or base signal. The conversion circuit, presented in Section 1.3.2.2, has to be parametric, in order to provide adaptability to different devices. Table 1.4 shows the level convention adopted in the following description.

To transform these levels to real-world values, a parametric map can be used.

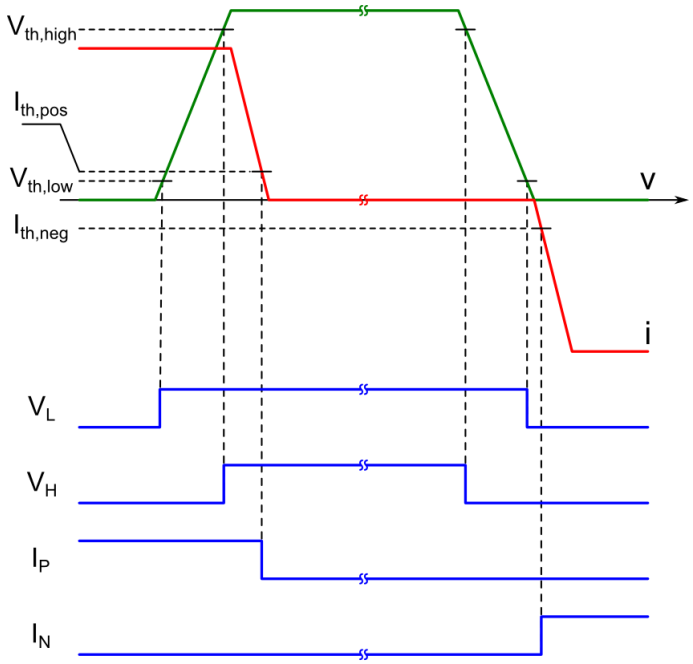


Figure 1.11: Thresholds used to convert sensed voltage and current to digital flags.

Table 1.4: Gate level description for different switch conditions.

Gate-level	Switch condition
-4	stable off state
-3	current fall
-2	voltage rise
-1	delay to off condition
0	delay to on condition
1	current rise
2	voltage fall
3	stable on state

The level values used are arbitrary. Other output values are those associated with the synchronization of high and low-side. As already anticipated, a gate driver is an independent unit, but when it is used in a half-bridge configuration, it needs some information from the other driver in order to operate properly, i.e. to insert the correct dead time and to give up controlling time derivatives when in passive states.

This information is extremely expensive to share, because very high voltage difference or even insulation can be present between the two sides; hence the number of signals should be kept to a minimum. In the proposed solution, two signals are used to synchronize high and low side. The first signal (A) is asserted whenever the power device is in the active state; the other signal (C) is active when the device is conducting, i.e. when its active part is on. This means that the conducting signal is on if the device is actively on, or it is on but with negative drain current. If the device is on but current is negative because of built-in diode, the signal will be off. It must be noted that these signals are connected to dedicated inputs to the control FSM, via an interface that can provide galvanic insulation.

The controlling finite state machine is depicted in Figure 1.12. Tables 1.5 and 1.6 are legend of states and signals, respectively. When multiple conditions are specified for an edge, the associated transition is taken if all of them are verified (logical conjunction). Some states are stable: they can be sustained for an undefined amount of time. Other states are transition phases for the switch, and they are limited in time, because of the device behavior. Every state has specific output values associated: a natural model for this FSM is a Moore machine. The convention to indicate with a superscript the output coming from the other gate driver (in the bridge configuration) is adopted.

Transitions among states can sometimes be expressed in different ways, each of which is correct, but some of them have some advantages. For example, transition from passive off to passive diode can happen because of current going negative for the passive device, or because the other (active) device, stopping to conduct, forces the passive switch diode on. The difference is that C' signal, being insulated, is usually a delayed copy of the other switch C signal, so I_N transition, being measured locally, usually precedes C' one. But I_N is noisy, so, in this case, transition on C' has been

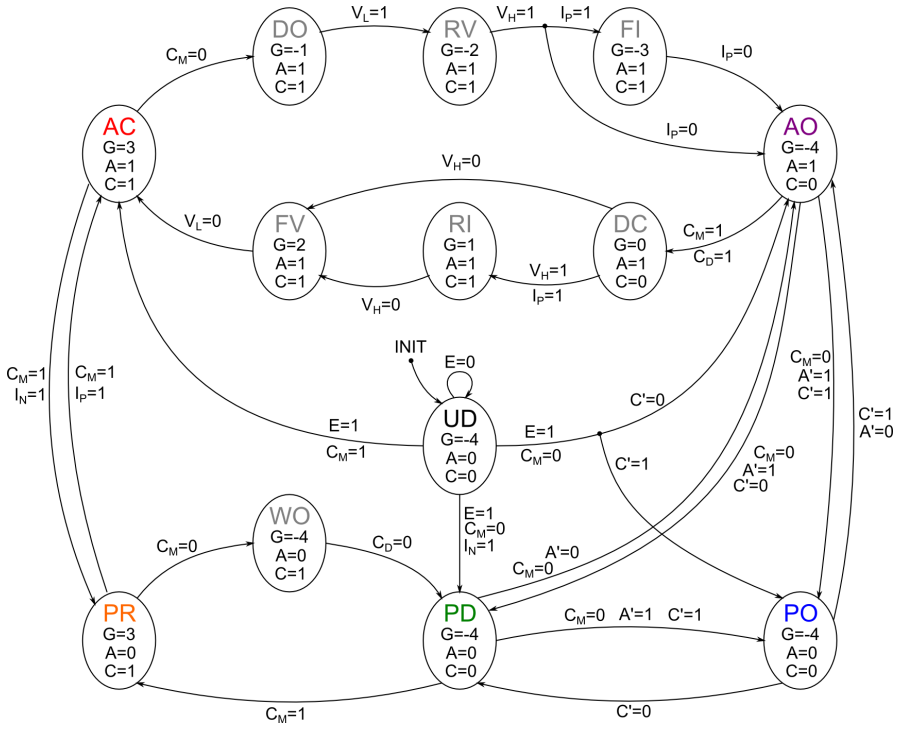


Figure 1.12: Finite state machine to control gate driver.

Table 1.5: Legend of FSM states.

Acronym	Index	State name
UD	0	Undefined
AC	1	Active conducting
DO	2	Delay to off
RV	3	Voltage rise
FI	4	Current fall
AO	5	Active off
DC	6	Delay to conducting
RI	7	Current rise
FV	8	Voltage fall
PR	9	Passive reverse conducting
WO	10	Wait switch-off
PD	11	Passive diode conducting
PO	12	Passive off

Table 1.6: Legend of input and output signals.

Acronym	Type	Description
E	input	enable
C_M	input	command
C_D	input	delayed command
V_L	input	low voltage
V_H	input	high voltage
I_P	input	positive current
I_N	input	negative current
A'	input	other switch active flag
C'	input	other switch conducting flag
C'_M	input	other switch command
G	output	gate level
A	output	active flag
C	output	conducting flag

chosen. Another important transition is that from active conducting to passive reverse conducting: only one flag could be sufficient (e.g. that of negative current, I_N), but taking advantage of the zero current zone it is possible to provide the circuit with some hysteresis, avoiding useless transitions in presence of noise or near-zero modulation.

It is possible to see that current transition states (FI and RI) can be bypassed under certain conditions. Since no restriction are established on the load behavior, the possibility to have very low load current must be accounted for. As already explained, current threshold values are different than zero, to limit noise related problems. If no current is seen from control FSM, neither transition can be seen, this is why these states can be bypassed.

The described control FSM can be easily implemented in a programmable logic device, like an FPGA or a less expensive CPLD. Using high-speed logic available inside these devices, low delays are introduced and reliable switch condition detection and control are expected.

1.3.2.2 Gate-level to current translation

The effective behavior of power switch controlled from gate driver depends heavily on the way gate level obtained from the control FSM is translated to electric quantities. This translation can happen in many ways: voltage or current set-points, linear or non-linear relationship, different circuit implementations [54, 55].

The solution proposed here, valid for insulated gate devices (like MOSFETs and IGBTs), is to convert gate levels to different current values, with two exceptions. In stable state (i.e. completely on or completely off device), no current control is desired, but a gate voltage that ensures low power losses is needed. This behavior can be achieved using a saturable current generator: until the current set-point is inside a predefined window, this current is generated, otherwise a voltage is impressed. A circuit that behaves as described is presented in Figure 1.13.

Voltage generator V_1 is the high gate drive voltage and its value is tuned to provide the desired on-resistance for power switch S. In applications where active thermal control is desired, this voltage can be lowered, in order to increase on-state losses. V_2 voltage is supposed to be as low as necessary to ensure proper switch off of the

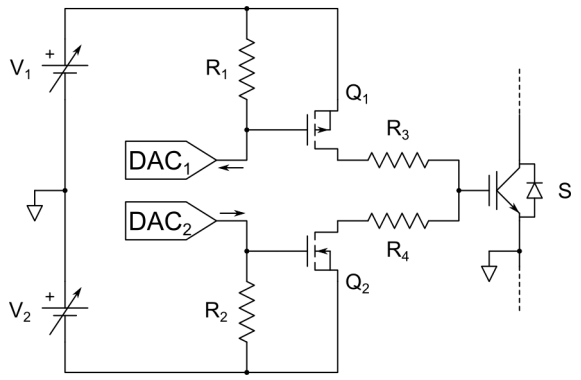


Figure 1.13: Circuit to convert gate level to drive signal for power device (S).

power device. This voltage can be null, if no negative output voltage is needed. Two digital-to-analog converters, controlled by a map from gate level to the desired output current, provide the link with the switch finite state machine. DAC_1 sinks current, while DAC_2 sources current. Current DACs were chosen because of their ability to change their output at very high speed (like in video applications), as it is needed to control fast switching devices.

R_1 and R_2 provide current-to-voltage conversion, and their value contributes to the time constant of the current transition, together with the input capacitance of the driving MOSFETs Q_1 and Q_2: to achieve high speeds, C_{gs} of MOSFETs and R_1, R_2 values have to be as low as possible, while DACs current should determine the effective voltage at gate nodes. Resistors R_3 and R_4 provide current limitation when transistors Q_1 and Q_2 are forced in triode region, i.e. when they drive the output by voltage and not by current.

MOSFETs Q_1 and Q_2 should have enough current capability to drive the power device gate in transient conditions, yet retaining a low input capacitance. An example of suitable component for Q_1-Q_2 is Fairchild FDC6333C, a complementary pair that can drive up to 2 A in both sink and source direction, but with worst-case C_{gs} of less than 300 pF [56].

It is clear that the most important part behind the conversion from gate level to current are the values used as input to DA converters. For example, with reference

to Table 1.4, if negative gate levels are mapped to a strong current output for DAC_2 and a zero current for DAC_1, and positive levels are mapped dually, the gate driver behaves like an ordinary one, with a voltage output and some current limitation as by resistor R_3 and R_4.

To gain control over switching transients, a more complex mapping should be used. During *delay* phases (states *DO* and *DC*), a high current should be generated, in order to move the operating point from a stable state to the first transition. This implies charging gate capacitance up to threshold voltage at turn-on (*DC* state), and discharging gate capacitance down to the V_{gs} value that corresponds to load current in saturation region, at device turn-off (*DO* state).

In current and voltage transition states (RV, FI, RI, FV), output current from the circuit has to be strictly controlled, to respect time derivative values and voltage overshoots. It is worth noting that the relationship between DAC current and gate voltages of Q_1 and Q_2 is linear, while the relationship between gate voltage and drain current is non-linear. This must be accounted for when determining values for the map effectively used to translate gate levels.

To implement a voltage or current control loop, actuation is usually obtained with a buffer, as shown in [57]. This buffer allows to use precise voltage and current generators as reference, yet guaranteeing high power for high-speed switching of the power device. Different buffer topologies are available, with source follower and complementary MOSFET inverting amplifier being the most widespread used. Some of these drivers are also co-packed with opto-isolated control circuitry, in order to provide a monolithic solution. Especially in case of current generation, some form of feedback is involved in circuit implementation, so care must be taken to ensure overall stability of the system.

1.3.2.3 Open-loop topologies

Open-loop control strategies lack the direct measurement of the controlled quantity, hence some means of parameters correction must be provided. What can be done is using some values that have been determined during system development, or dynamically changing parameters with small, subsequent, variations, looking at some

performance parameters. *Perturb and observe* algorithms can be a good example of this kind of strategies.

What is usually done to control voltage and current waveforms during switching transient is changing the gate resistance. This is obviously a very simple yet effective technique, since no special components are needed. Some schemes provide different values for power device switch-on and switch-off, using diodes. This concept can be expanded, providing an array of resistors that are actively commutated; through parallel and series connection, even more resistance values can be obtained [58, 54]. Taking advantage of the FSM, provided that active resistor switching is available, the resistance value used can be associated with the gate level described in Section 1.3.2.1.

Another way to convert gate level to electrical quantities is to associate each level with a specific current, that is forced in the device gate terminal (if this last is insulated). This control technique removes the gate current from the set of controlled quantities, being it inherently limited by the driving circuit. During stable states, current can be set to its maximum value, and current generator should be left free to saturate, in order to impress a voltage (the one of the rail which the generator is connected to). The main drawback of this control is its limited linearity: when an insulated gate device is driven by a constant current on its gate, it hardly happens that voltage and current transition have a linear shape in time. This implies that some undesired harmonic content can show up, even when time constraints of voltage or current transmission are satisfied.

1.3.2.4 Closed-loop topologies

Closed-loop topologies directly measure the actual value of controlled quantities, thus they can achieve high linearity. The purpose of the gate driver can be summarized in controlling four quantities: voltage derivative (EMI and load aging), current derivative (EMI and overvoltage), gate voltage (on-state losses) or gate current (minimum delay time, switch life).

To control all of them, four distinct loops are required, in general. These control loops can be arranged on different levels, in order to achieve better performance and simplify circuit development. Also the output physical quantity of the regulator can

change, thus determining different system responses. In closed-loop topologies, gate levels are linked to loop set-points and enable signals, when these loops are switched.

The most intuitive implementation of a closed loop control for a power switch is probably using as many switched loops as the number of controlled quantities. In every switch state, only one quantity is controlled (e.g. gate current during delay time, gate voltage during on-state, . . .), so it is possible to dynamically choose which loop is active. In order to have a stable control over all switch states, each regulator shall hold its memory when not active, and its error input must be canceled in the meantime.

It must be noted that this control is suboptimal by design: since the output of the regulator is the voltage that is impressed on the control terminal, it is not possible to directly limit the gate current when controlling voltage. This limitation can be added later in the voltage actuating circuit. Figure 1.14 reports a possible block scheme for the implementation of this control. As it can be seen, both inputs and outputs of the controllers are switched by the high-speed control logic, in order to have only one loop active at a time. It must be noted that voltage derivative control requires opposite sign for error signal than other controls: if a high-value positive voltage derivative is demanded, gate voltage must be reduced, since a decreasing relationship exists between these quantities.

This scheme lacks the ability to limit the gate current when the current loop is not active, i.e. when the switch is in a delay state. To overcome this limitation, it is possible to organize control loops in a two-level topology, as shown in figure 1.15. The inner loop controls current and its set-point can be directly a current (the maximum value tolerated by power device gate and actuating circuit), or the output of three time-switched loops, controlling voltage derivative, current derivative and gate voltage. In this case, the inner (gate current) loop is always active, and the FSM logic controls switching of outer loops.

Comparing this solution with the one previously described, this is more convenient. Optimal controller parameters for the first proposed solution can be normalized and the comparison of PI parameters shows that the current control requires different values than the other loops. This suggests that a different relationship between gate

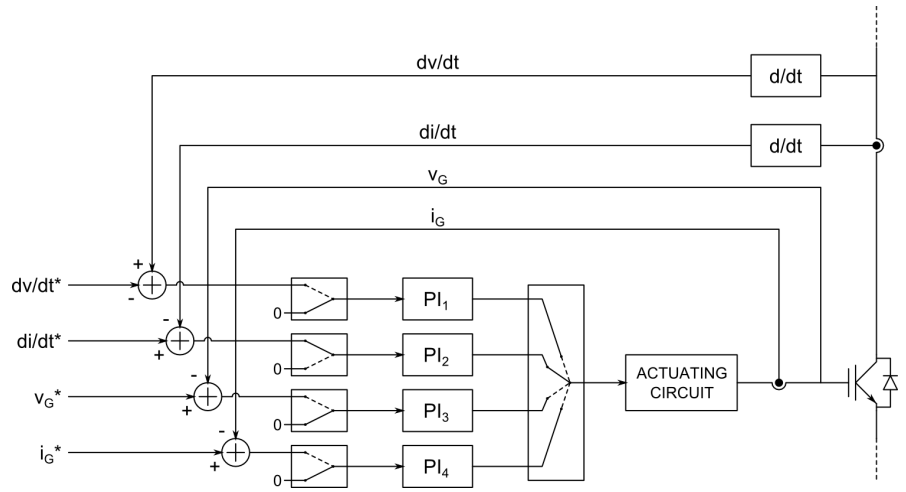


Figure 1.14: Control scheme with four parallel loops, switched in time.

current and other quantities, with respect to gate voltage, exists. Also, some improvement on system cost can be achieved: if parameters of the outer loops are equal, only one controller can be used, with logic controlling error signal input only. The control scheme described here is very similar to the one presented in [57], but with the major difference of the current loop being the innermost.

Starting from the fundamental ideas above, it is possible to keep the loop configuration, while changing the manipulated variable. The actuation system can directly determine the effective series resistance as seen from the gate. This solution overcomes the limitation of current not being limited: if the voltage of the generator is determined by sign (positive to switch-on, negative otherwise), and the magnitude determines the conductance of the generator itself, a saturation of the last can implement a reliable current limitation, regardless of which loop is currently generating the conductance set-point. The described control scheme is the same of figure 1.14.

Many other closed-loop gate drivers exist in literature, such as current-mirror based solutions [55], or with an incomplete number of feedback loops [59]. These are summarized in [60].

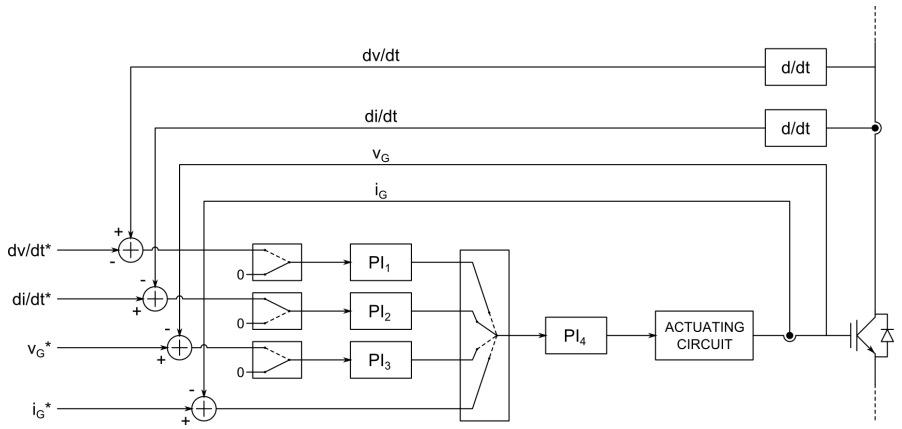


Figure 1.15: Control scheme with three outer loops and one inner loop for gate current.

1.3.2.5 Ancillary features

The augmented knowledge of an active gate driver about the electrical events that occur in a power circuit enable to equip the driver itself with many new features, that can help in improving overall system performance and reliability.

For example, blanking time is essential to avoid power bus shoot-through. In this phase, both bridge switches are commanded off, in order to let the current decay in the previously on device. The effective time needed for a device to switch off depends on many parameters: device characteristics, temperature, load current, control terminal, . . . What is usually done is to set this time to a worst case value, with some margin added. This results in added distortion in the output waveform, and the loss of driving for a relatively long time can trigger also spurious ringing. An active gate driver can provide adaptive blanking time if it has enough information on the state of the switches [61].

First the condition to avoid should be determined; there are three main situations that can lead to a bus shoot-through:

1. Both switches in the bridge are commanded to be on. This is usually caused by an error in the control circuit (i.e. PWM modulator), it can happen at any time and it is not directly connected to a transition or commutation delay of power

devices. Moreover, it can be prevented by proper filtering the gate signals.

2. One switch is actively conducting load current, then it is commanded to be off, and the other switch (that, in presence of inductive load, will be in a *passive* condition) is commanded to be on. If the passive device is switched on before the effective turn-off of the active one, shoot-through can happen.

3. The opposite transition to the last one: when a passive device is commanded to be on but its diode is conducting current, some time is needed for the active part to be off. If this delay is not accounted for and the active device is switched on, shoot-through can occur.

It is important to note that it is not always necessary to command the switch-on of the active part of a power device when its diode is conducting. This can be useful, for example, in the case of power MOSFETs, because they can conduct in both directions (even if reverse blocking capability is guaranteed in only one way), and overall device exhibits lower on-resistance with respect to diode conduction only. Bipolar devices, like BJTs and IGBTs, being unidirectional, hardly give the same benefit, but device turn-on is commanded anyway, since load current direction is generally unknown, and voltage is needed to be forced to one out of two rails.

To avoid shoot-through in all described situations, it is sufficient to switch the second device on only if the first one is completely off. For the studied topology, this information can be inferred from the voltage at device power terminals, it is possible also to monitor the effective gate voltage, as done in [61].

For the active device, effective turn-off can be seen from device voltage: when it reaches bus potential, turn-off transient is complete. This moment (B in Figure 1.10) is recognizable from the passive device, too: when its voltage in near zero, the diode turns on and also the active part can be commanded on. Thus, blanking time related to active device switch-off (BT_1) can be directly sensed from both devices.

On the other side, passive device switch-off (with diode on, from D to E in Figure 1.10) has no evident transitions in voltage nor current waveforms. To overcome this problem, it could be possible to sense effective gate voltage or to measure the small voltage difference that arises between device power terminals when the active part

is on, besides conducting diode. These solutions were discarded because of difficult implementation in a highly noisy environment, like those where high power rating devices are employed.

The adopted solution is to measure the time needed to switch off the active device (i.e. BT_1 duration), and to replicate the same delay also for passive switching (making BT_2 equal to BT_1). This is a sub-optimal solution, but it is fairly inexpensive and provides adaptability with respect to device model, current and temperature (provided that both high and low switches operate in similar conditions). If a strong imbalance in bridge devices operating conditions exists, the last time active switch-off duration of the same device could be used.

It is thus possible to use the same command signal for both high and low devices, using a simple negation for one of them. It is important to note that the information about duration of switch-off must be shared between devices; this can be troublesome since control circuit must often fulfill galvanic insulation requirements.

As described above, the gate driver has to measure switch-off time for power device in hard switching condition, in order to provide a comparable delay for soft (i.e. *passive*) switching. Since it is desirable to have always an updated value of switch-off time, means of evaluating its value are given for both active and passive switch conditions. When a switch is in an active state, the time to measure is that needed to go from C_M signal fall to *active off* state, going through states DO, RV and FI (this last only when applicable). When in a passive state, the other switch time can be measured if signals C' and C'_M (i.e. C and C_M signals coming from the other device) are available. In fact, the time occurring between C'_M fall and C' fall is exactly the duration of the switch-off transition of the other switch.

In this case, if both signals are galvanically insulated, any delay in the insulation circuit will not alter the measured value, supposed it is equal for both signal sources. The ability to measure switch-off time in different switch situations allows a great degree of flexibility. Depending on device characteristics, only one value could be used, or some form of mathematic elaboration can be carried out, if, for example, it is evident that soft-switching switch off time is much different than the hard-switching one.

To improve safety, a programmable minimum value for switch-off timer could be implemented, as a fall-back solution in presence of faults. The timer described here could be implemented in the CPLD device too, along with the programmable delay unit, used to generate C_D signal from C_M.

Following the power switch during its commutation can also give precious diagnostic information, that can be used to embed a robust fault detection system in the gate driver. Basic fault conditions that should be detected are over-current and over-temperature, while over-voltage should be prevented, because, when happening, it is destructive for the power device; these faults are independent of state-of-switch knowledge.

Other diagnostic information can be obtained from checking redundant signals. The presented control scheme has different form of redundancy. Both current and voltage of the power device are examined by means of couples of signals, (I_P, I_N) and (V_L, V_H). Only three configurations out of the possible four are valid: detecting $(I_P, I_N) = (1, 1)$ or $(V_L, V_H) = (0, 1)$ is an error condition and shows some form of malfunction in the sensing circuit. Also command signal C_M is redundant in some way: it is correlated with the other switch command C'_M: if they are equal for a period of time longer than the insulation delay, it means that a short-circuit was requested from control logic, indicating an error in the modulator.

Some consistency check can be performed between input logic and stable states. Transition diagram of Figure 1.12 shows that it is not possible to have positive current in the undefined state, if no transition in command or enable signal is requested. Having $V_L = 1$ or $V_H = 1$ in active conducting state means that desaturation is occurring, i.e. that some fault in gate command circuit or short circuit on power terminals is happening.

Another error condition is a presence of positive current ($I_P = 1$) in states active off, passive off or passive diode conducting. Passive reverse conducting state is not in the list, because positive current is admitted and forces a commutation to the active conducting state. Passive diode and passive reverse conducting can be used to detect failures in built-in diode, if a loss of clamp is noticed, as pointed out by $V_L = 1$ or $V_H = 1$ in these conditions, meaning that power device voltage is growing even if

Table 1.7: List of possible faults and supposed causes.

Condition	State	Possible fault origin
$I_P = 1$	UD, AO, PO, PD	device, measuring circuit
$V_L = 1$ or $V_H = 1$	AC, PR, PD	device, control FSM
$V_L = 0$ and $V_H = 1$	all	measuring circuit
$I_P = 1$ and $I_N = 1$	all	measuring circuit
$C_M = 1$ and $C'_M = 1$	all	modulation
watchdog timeout	transition	device, control FSM
too high/low switch-off time	all	device

diode is expected to be on.

It is also possible to measure the time passed in each state: if the switch stays in a transition state for too long a time, a fault has occurred and appropriate actions shall be carried out. This diagnosis is similar to a watchdog, used in CPUs to detect a deadlock in the code execution. Measuring switch-off duration is the basis to another form of time-based diagnosis. If this time is too long or too short, some kind of problem is occurring, maybe related to over-current, bad gate drive circuit or some form of aging or fault of the power device. Table 1.7 summarizes the error conditions and the possible causes.

1.3.3 Performance evaluation

1.3.3.1 Comparison of control architectures

Figures 1.16 and 1.17 show simulation results for the open loop gate driver architecture described in Section 1.3.2.3, with actuating circuit as in Section 1.3.2.2. Figure 1.16 shows characteristic waveforms for the active switch. Gate driver correctly inserts dead time and generates voltages used to set power switch current. It is evident that during delay time gate current is limited keeping Q_1 and Q_2 transistors of Figures 1.13 in saturation region, while a voltage is set when the voltage transient has finished.

Controlling V_{ds} during its transient forces V_{gs} to exhibit a longer Miller plateau

with respect to the use of a traditional gate driver. Since very small difference in gate voltage during Miller phase is accompanied by a huge excursion of drain voltage, the sensitivity of $\mathrm{d}V_{ds}/\mathrm{d}t$ to gate current is important: this can lead to difficulty in controlling device during this phase, as will be highlighted later.

The output voltage waveforms highlight some problems. Voltage thresholds are evident, and until V_{ds} is lower than $V_{th,low}$, output time derivative is not controlled. Nonetheless $V_{th,high}$ is placed at a value lower than the bus voltage, to account for ripple or tolerance in its value. This causes an additional delay between voltage rise and current fall.

Figure 1.16 shows effects of stray inductance on power device terminals. It manifests overshoot in voltage during device turn-off and undershoot during device turn on. This last can trigger voltage fall detection before current rise, causing some problems. Figure 1.17 shows waveforms for the passive switch. In this case, the gate is always driven by voltage and never current limited. This is not an issue, since the passive switch has no power in controlling waveforms, and it is switched on only to reduce on-state losses.

Looking at the voltage rise transient, a small current on gate terminal can be seen. This is the current flowing through the Miller capacitance (C_{gd}) during voltage transient. If not treated properly, this current can make the gate voltage rise, possibly causing a transient device turn on. The simulation shows that the proposed circuit (as in Figure 1.13) acts as an active Miller clamp circuit too, providing very low resistance path between gate and drain, when the switch is supposed to be off [62].

The output waveforms are fully determined by the active switch, holding these equations:

$$V_{ds,high} + V_{ds,low} = V_{bus}$$
$$I_{d,high} - I_{d,low} = I_{load}$$

The simulation output of the three different closed-loop control schemes described in Section 1.3.2.4 are reported in figures from 1.18 to 1.20. They all show an overall better performance of the direct feedback control over the feed-forward one, but their response is different under many aspects.

As suggested by Figure 1.18, the use of four distinct time-switched control loops allows near-to-ideal results. All set-points are correctly followed, as shown in Figure 1.24. Non-ideal behavior is seen in proximity of device state changes, and can be ascribed in part to delay of transmission chain from control logic to actuated signal, and in part to transition of control from one loop to another. Even when the responses of the loops are over-damped, switching among loops can cause overshoots and ringing: managing transitions from different controllers is the main disadvantage of the switched-loop architectures.

Figure 1.19 reports results when controlling switch with three outer switched loops (voltage derivative, current derivative, gate voltage) and inner gate current control. Waveforms are very similar to the previous case, but the implementation is radically different. Furthermore, some ringing can be seen at the beginning of voltage rise.

Results of conductance control are presented in Figure 1.20; the overall response is under-damped compared to other schemes, and gate voltage phase is much faster, as shown by the high value reached by the gate current. These results suggest that some finer tuning could be necessary in order to implement the control in the real world.

Figures 1.21a and 1.21b report operating points in transient conditions, in the V_{ds}-I_d plane, for both active and passive devices, with open-loop control. These graphics show that the switching trajectory is almost ideal, with very low overshoot in both current and voltage. In fact, even in presence of stray inductance, if the current is controlled, voltage alteration is minimal. Current overshoot is also low because the model did not include diode reverse recovery; this is a correct approximation if the devices are modern silicon-carbide Schottky barrier diodes (SiC SBD).

Figures from 1.21c to 1.22d compare active and passive switching loci for the three closed-loop topologies. They are very similar, but the non-ideal behavior, especially that linked with the low current and high voltage phase, is magnified. As already seen from Figure 1.20, the conductance control is under-damped compared to the others, as it is pointed out by its spiral-shaped trajectory.

Figure 1.23 shows the control FSM states for both high and low devices, the first being the active one (having chosen a positive bridge current in simulation). Diagram reports state acronyms from Table 1.5, and a time comparison with other graphs

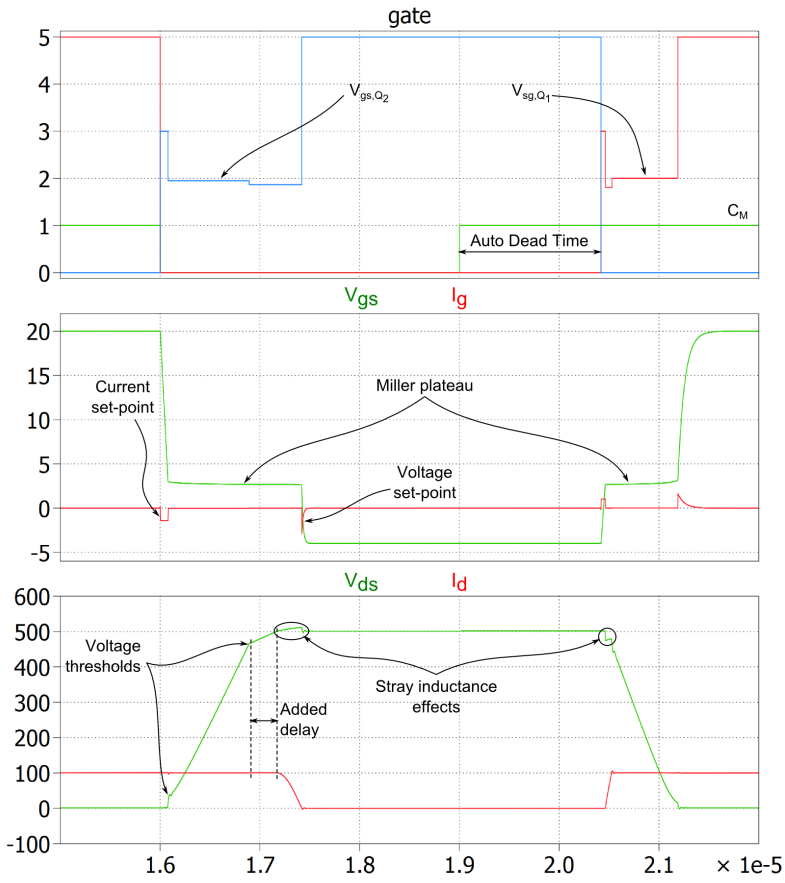


Figure 1.16: Simulation results for active switch, showing gate drive signals, gate voltage and current, drain voltage and current.

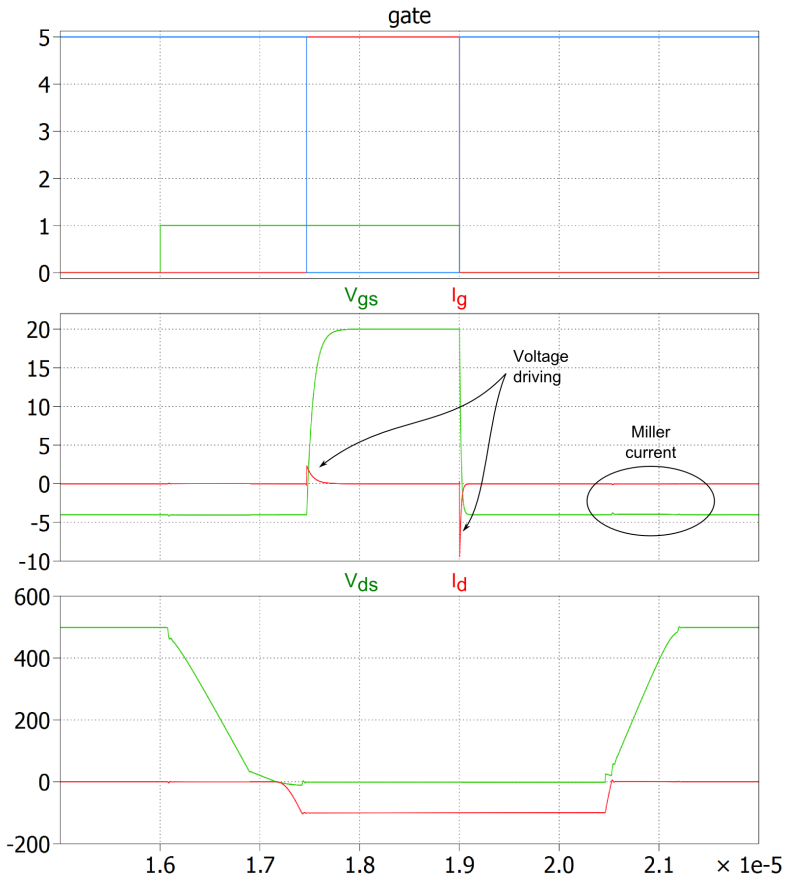


Figure 1.17: Simulation results for passive switch, showing gate drive signals, gate voltage and current, drain voltage and current.

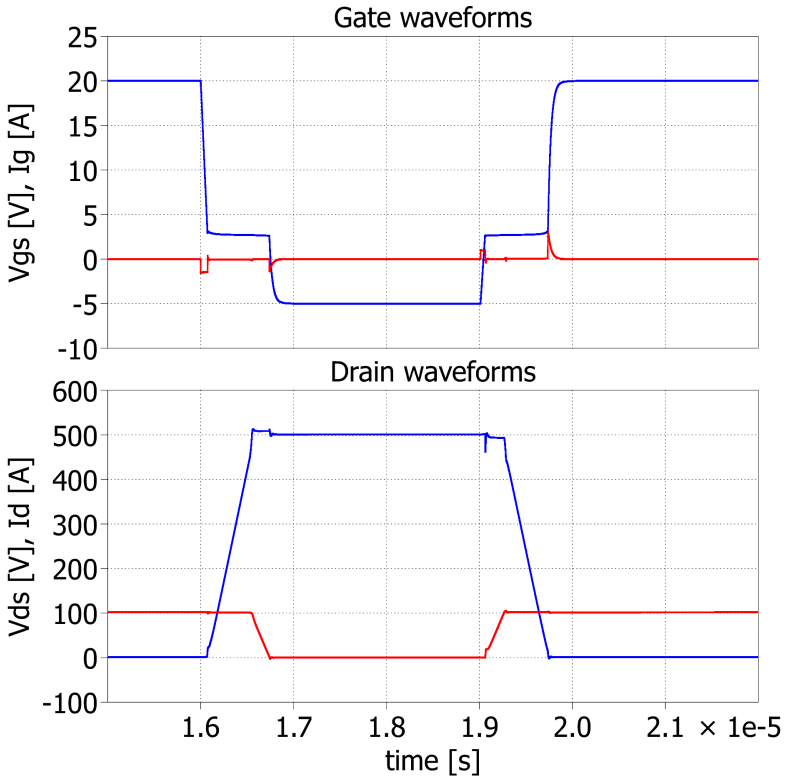


Figure 1.18: Gate and drain voltage and current waveforms, with four switched loops control, voltage output.

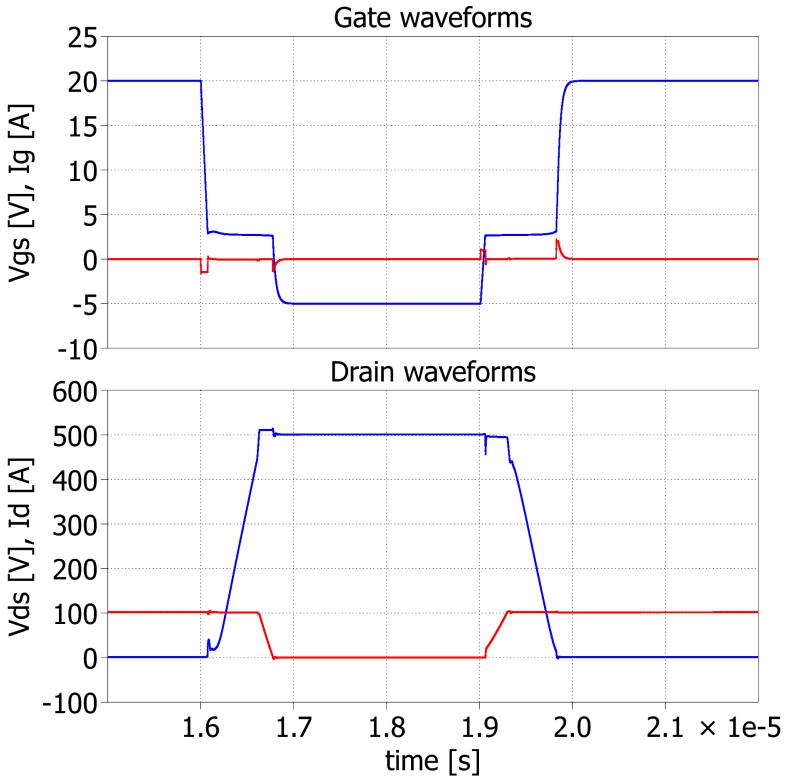


Figure 1.19: Gate and drain voltage and current waveforms, with three switched outer loops and inner gate current loop control, voltage output.

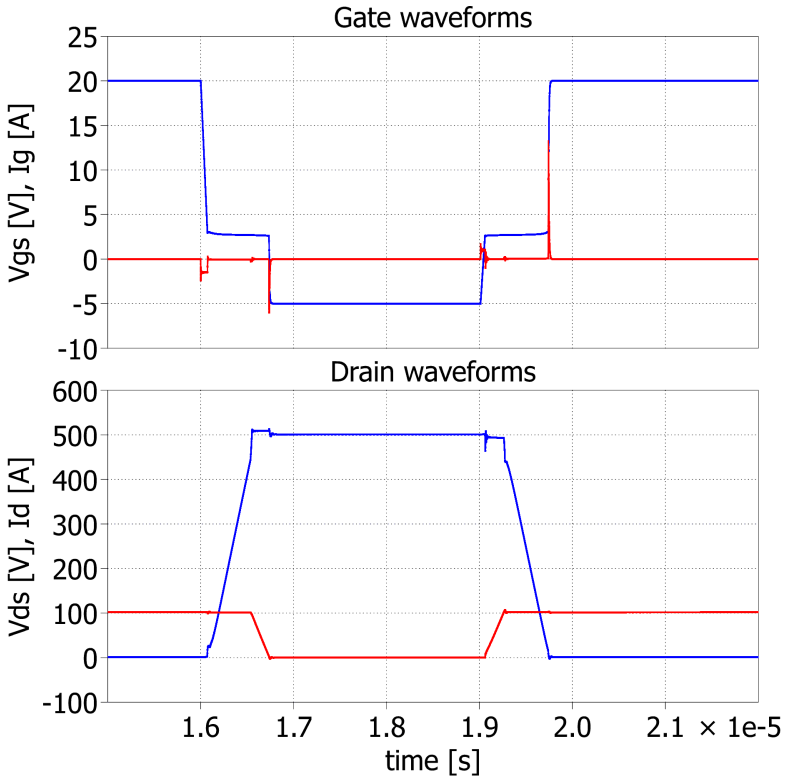
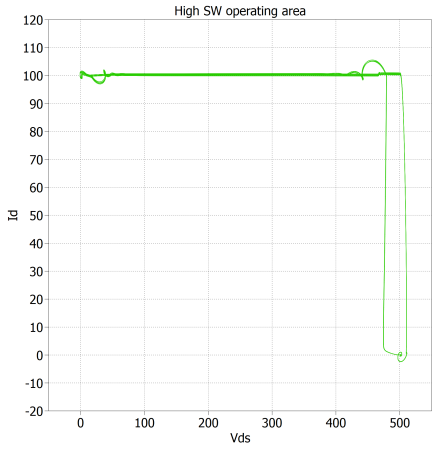
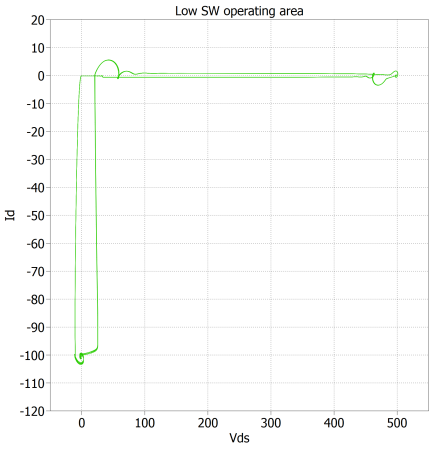


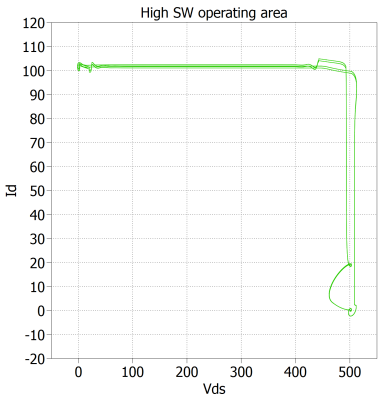
Figure 1.20: Gate and drain voltage and current waveforms, with four switched loops control, conductance output.



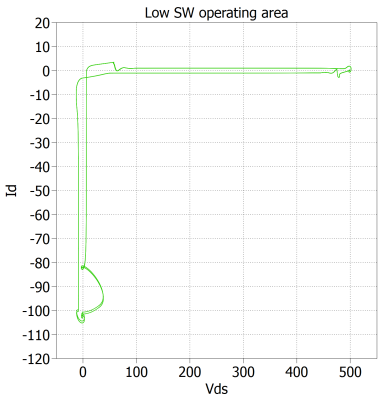
(a) Active switch operating area with open loop current control.



(b) Passive switch operating area with open loop current control.

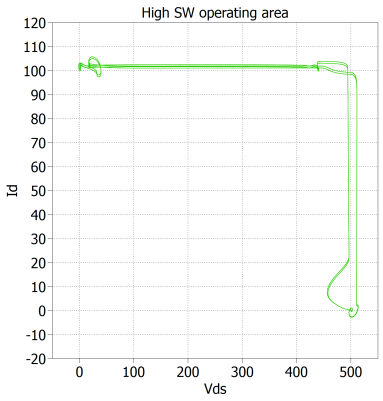


(c) Active switch operating area, four switched loops.

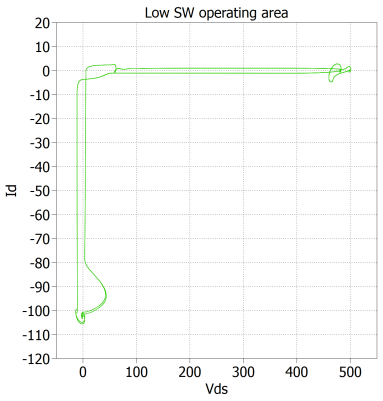


(d) Passive switch operating area, four switched loops.

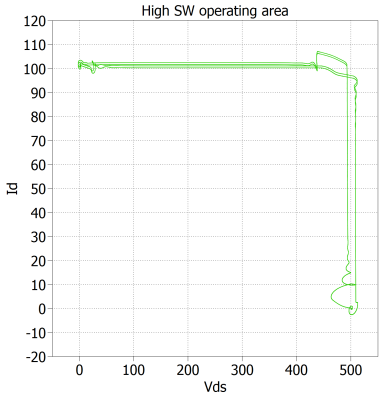
Figure 1.21: Device operating points in switching transitions.



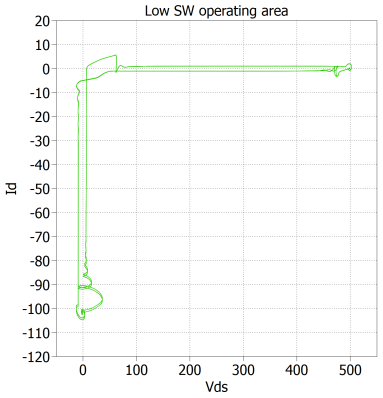
(a) Active switch operating area, three outer loops, inner gate current loop.



(b) Passive switch operating area, with inner gate current loop.



(c) Active switch operating area, four switched loops, conductance output.



(d) Passive switch operating area, four switched loops, conductance output.

Figure 1.22: Device operating points in switching transitions, closed loop controls.

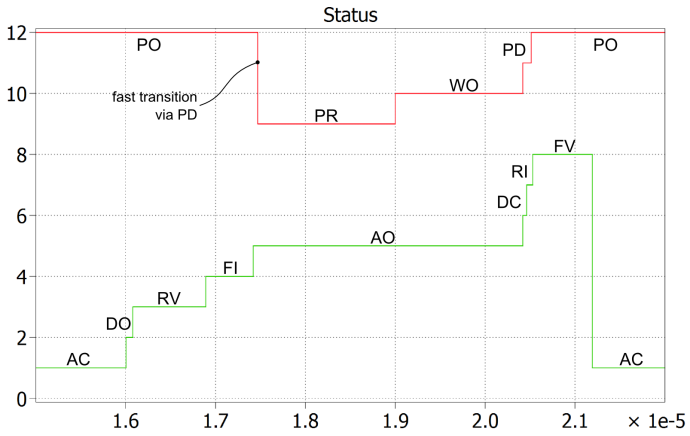


Figure 1.23: Simulation results for switch states: active switch in green, passive in red.

shows that the switch condition is correctly determined. The only anomaly is seen in transition from PO to PR, where PD state is traversed very fast, due to the fact that its exit condition ($C_M = 1$) is already satisfied when entering the state itself.

This figure was obtained with the open loop control, but very similar results can be achieved also when a feedback scheme is employed. This can be verified by examining Figure 1.24, since each set-point is determined by the FSM, together with enable signals for the switches that commutates among the loops.

1.3.3.2 Figure of merit

The plots of Figures 1.21 and 1.22 show at a glance the power device oversizing (i.e. the power handling capability) needed for each control scheme, given its nominal working conditions. Nonetheless, contrasting the bounding box of the actual switching locus with the ideal one and computing the ratio of those areas is a quantitative measure of the control performance. This figure of merit, called Switching Locus Area Ratio (SLAR) is proposed for the first time in [60].

When a traditional gate driver is used and some parasitic inductance exists in the current path, SLAR values can be higher than 1.5. The switching locus of the open-

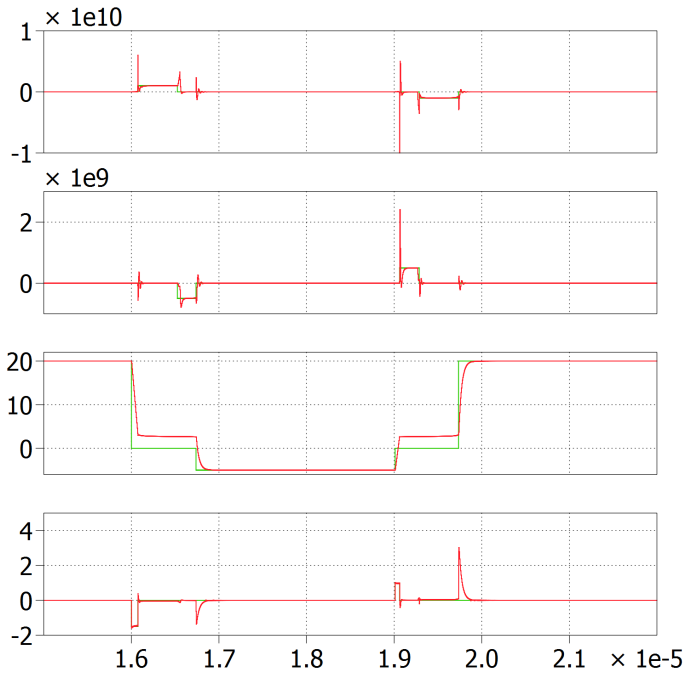


Figure 1.24: Feedback control with four parallel loops following set-points, where they are different from zero. From top to bottom: voltage derivative, current derivative, gate voltage, gate current.

loop current control features SLAR = 1.17, while closed loop topologies exhibit values from 1.09 to 1.12.

Chapter 2

Active Gate Drivers

A journey of a thousand miles
must begin with a single step.

– J.F. Kennedy, 1963

In Chapter 1 the analysis of the state of the art in power conversion components showed that many new, fast and high-performance devices are available today, revolutionizing the possibilities among which power electronics engineers can choose. In order to get the most out of these devices, also ancillary circuits need improvement. To control the effect of parasitic inductance of a SiC MOSFET on the output voltage waveform, a specialized gate driver can be designed. EMI filters should account for different (and possibly wider) spectra due to the use of GaN HEMTs, and so on. Specialized circuits are believed to represent a way to effectively use WBG devices, and to fully exploit their potential.

In this work, special attention is paid to Active Gate Drivers. AGDs are already present in literature and they are often applied to silicon devices. Some efforts were devoted to adapt these circuits to WBG devices, but results are far from completeness. Moreover, the new devices pose some tight constraints in terms of bandwidth, latency and accuracy of gate (or base) terminal control, mainly due to their augmented speed with respect to silicon parts. This calls for improvement also for circuits like those

presented in [63].

In this chapter, the own work of the author in AGDs is presented, showing three developed circuits. The first one can vary its equivalent resistance as from a voltage command; the major shift with respect to the state of the art is in the possibility to handle high instantaneous currents, thus being suitable to switch capacitive nodes at high frequency. The other two circuits, despite being topologically very similar, implement two radically different modes of controlling the gate terminal. In the first one, voltage and output resistance of the driver can be changed simultaneously, differently from the separate action that is commonly seen in literature; in the second circuit a completely new approach is presented, building a driver that can force the power device into a controlled shoot-through condition; this was never explored before and opens up many new possibilities, that will be partially investigated in the rest of this work.

2.1 Voltage Controlled Power Resistor

2.1.1 Adding power to JFETs

As described in Section 1.3.2.4, the main power switch behavior can be controlled by varying the conductance of the gate charge and discharge path. To do so, a special circuit is required, to provide variable conductance under control of an electric signal. Historically, the JFET has been used to implement voltage controlled resistors: when it works in the linear region, the gate voltage can control the equivalent resistance that is seen between drain and source. This is used when automatic gain controls are needed, e.g. in radio receivers, or to change the frequency of oscillators under voltage control (VCOs).

From the strict theoretical point of view, MOSFETs could be used as well, if operated in the linear region: they exhibit a voltage-controlled resistor behavior similar to that of JFETs. The main difference is quantitative: given the higher transconductance, the sensitivity of the equivalent resistance with respect to the gate voltage is much lower, since the equivalent resistance is related to the reciprocal of the transconductance itself. This is clearly highlighted in Figure 2.1, where the current vs. voltage

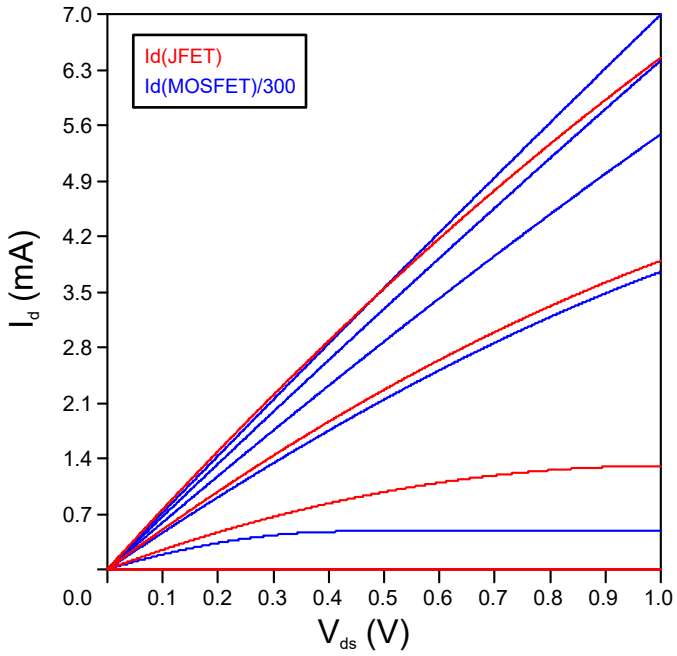


Figure 2.1: Comparison of JFET (red) and MOSFET (blue, scaled) output characteristics, under different gate-source voltages. Drain-source voltage is on the horizontal axis, while the drain current (scaled 300 times for the MOSFET) is on the vertical one.

characteristic of a MOSFET are compared with one of a JFET of similar package and dimension.

For this reasons, the JFET should be preferred if a large resistance value is desired. The main limitation of this component is its (usually) limited current carrying capability. Since gates exhibit a capacitive impedance, and are charged and discharged at high frequency, the required current is usually significant and not manageable by signal devices. Other virtual resistor schemes in literature were explored, as those based on Operational Transconductance Amplifier (OTA), but the limitation was again on the current, and hence power, requirement. The solution was found in using the JFET as a “signal” resistor, and to close a control loop on another component,

using the JFET current as reference.

To arrange this control loop, the voltage of the virtual resistor is applied to both the JFET and the controlled part that is effectively implementing the power resistor. Currents are compared and the output device is operated in order to sink or source a current that is multiple of that measured on the JFET. Since the current depends on the voltage of the node where it appears, an effective resistor is thus made. The proposed circuit is shown in Figure 2.2: it is a bilateral voltage generator with variable output resistance, which value is determined by a voltage control signal. The circuit is complementary, and each section has its own reference, around the power rail that is needed (pull-up or pull-down action).

The basic working principle of the circuit is the closed-loop operation of the operational amplifier. The voltage on the shunt resistor is compared with the voltage on the drain of the small-power MOSFET. Since a voltage divider is used to read the drain voltage, the equivalent resistance seen from drain terminal inward will be roughly the shunt resistance value times the reciprocal of divider ratio.

In order to be able to vary the output resistance, the divider needs to change under voltage control. This can be effectively achieved with a junction FET, acting as voltage controlled resistor (VCR). JFETs cannot directly be employed in the output section, since they are available only for signal processing and not for power. Nonetheless, the VCR behavior is linear for low drain-source voltage. With power signals this cannot be guaranteed, while the closed loop operation of the proposed circuit keeps this voltage small.

An accurate selection of voltage divider parameters allows to both have low error on output resistance, high linearity with control voltage and low voltage on operational amplifier input terminals. This last point is very important if high dynamic control of the output is needed: high speed amplifiers require low voltages, that are usually incompatible with the high swings needed to drive the power gate. Both JFETs share the same gate signal, coming from the control unit. MOSFETs are added to mutually force one amplifier in open-loop configuration, setting its output resistance to a very high value. This prevents a short circuit of the power rails to happen. The main disadvantage of this circuit is the complex bias architecture needed, together with the

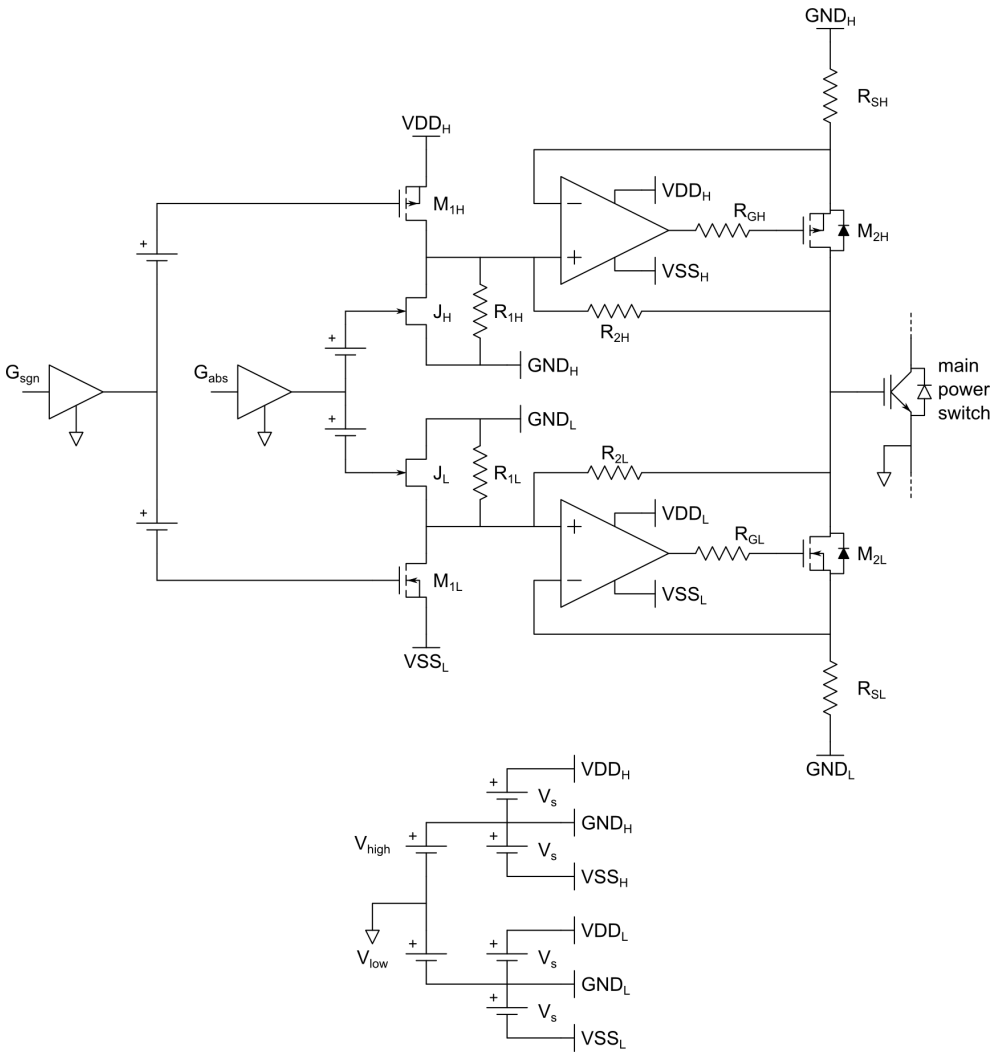


Figure 2.2: Ideal electric scheme of a bilateral voltage generator, with output impedance controlled by voltage.

complicated power supply.

2.1.2 Large-signal behavior

The detailed operation of this circuit can be understood considering only one of the sides; in the following, the low side will be described. Supposing M_{1L} initially off permits to understand the behavior of the circuit when forcing power switch gate to GND_L. The instantaneous drain current of M_{2L} is sensed by R_{SL}, which is a shunt, so its value is low. Setting R'_{1L} to the parallel of R_{1L} and J_L equivalent resistance, and considering V_G as the gate voltage of the power device with respect to GND_L, the voltage on the non-inverting input of operational amplifier is:

$$V_{INP} = V_G \frac{R'_{1L}}{R'_{1L} + R_{2L}} \tag{2.1}$$

If the operational amplifier is working in its linear region, virtual short circuit holds, thus:

$$V_{INP} = V_{INN} = R_{SL} I_D \tag{2.2}$$

Putting together (2.1) and (2.2), I_D can be obtained:

$$I_D = \frac{R'_{1L}}{R_{SL}} \frac{V_G}{R'_{1L} + R_{2L}} \tag{2.3}$$

To determine the resistance seen from gate terminal to GND_L, the current on R_{2L} must be added:

$$I = I_D + \frac{V_G}{R'_{1L} + R_{2L}} = \frac{V_G}{R_{SL}} \frac{R'_{1L} + R_{SL}}{R'_{1L} + R_{2L}} \tag{2.4}$$

Thus, the equivalent conductance seen from power gate terminal to GND_L is:

$$\begin{aligned} G_{eq} = \frac{1}{R_{eq}} = \frac{I}{V_G} &= \frac{R'_{1L} + R_{SL}}{R_{SL}(R'_{1L} + R_{2L})} \\ &\xrightarrow{R_{SL} \ll R'_{1L}} \frac{R'_{1L}}{R_{SL}(R'_{1L} + R_{2L})} \\ &\xrightarrow{R'_{1L} \ll R_{2L}} \frac{R'_{1L}}{R_{SL} R_{2L}} \end{aligned} \tag{2.5}$$

If the suggested approximations hold, the relationship between G_{eq} and R'_{1L} is fairly linear, and the equivalent conductance of the generator can be determined by the gate voltage of J_L. The overall relationship is not linear, since the equivalent resistance of the JFET appears inside a parallel of resistances.

Turning on M_{1L} forces V_{INP} to the lowest possible value for the op-amp, which goes into the negative saturation region, setting M_{2L} off. This avoids short circuit of the power rails. Analogous considerations hold for the pull-up section of the circuit in Figure 2.2.

2.1.3 Small-signal behavior[1]

In order to carry out a more detailed symbolic analysis of the circuit and to handle feedback loops properly, a graphical method [64, 65] based on Signal-Flow Graphs (SFG) and Driving-Point Impedances (DPI) was applied. Unlike the matrix based approaches, best suited to computer processing, this technique makes it possible to manually find the transfer functions of the dynamic system. SFG/DPI provides designers with insights into the circuit behavior and useful information during circuit sizing and performance optimization activity. In addition, using this technique, even the most hidden loops in the circuit are highlighted, thus preventing errors and omissions.

Looking at Figure 2.4, which shows the SFG of the small signal circuit in Figure 2.3, many feedback loops can be identified, therefore an in-depth stability analysis is mandatory. The feedback loops are reported in the denominator terms section of Table 2.1.

The most important transfer function in a circuit of this type is the voltage controlled equivalent resistance $R_{eq} = v_{out}/i_{in}$. The small-signal parameters of J_1 change with its DC gate voltage, as is well known, so R_{eq} is a function of JFET V_g though this parameter is not explicitly present in the analysis proposed.

R_{eq} is obtained by means of the Mason's rule applied to the SFG in Figure 2.4. The analytic expression returned by the SFG/DPI method are quite complex (6^{th}-order), therefore symbolic computation and simplification has to be performed with

[1]This section describes work done together with Giorgio Pietrini, PhD student at University of Parma, as part of his work about WBG devices in avionics applications.

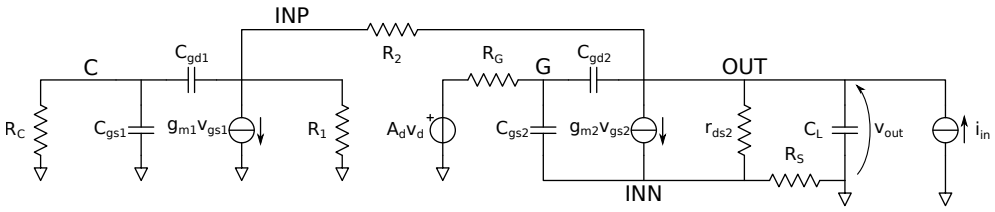


Figure 2.3: Small signal model of the analyzed circuit.

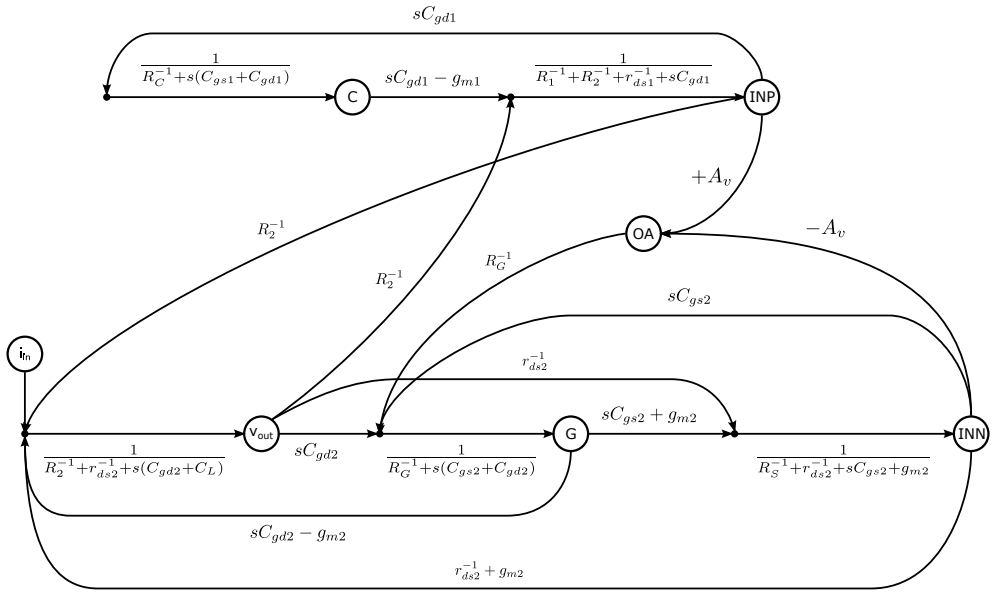


Figure 2.4: Signal Flow Graph of the equivalent circuit.

a mathematical environment like MATLAB in order to make feasible the pole-zero stability analysis. It is worth noticing that single-pole approximation is used to take into account the op-amp's dynamic behavior, so $A_v(s)$ is a transfer function in the complex frequency domain. Moreover, R_g incorporates not only a gate resistor in the circuit but also the output resistance of the op-amp.

$$
\begin{aligned}
R_{eq} = \frac{N}{D}, \qquad & \text{with} \\
& N = T_{1n} \cdot (1 + T_{1d} + T_{6d} + T_{7d} + T_{1d}T_{6d} + T_{1d}T_{7d}) \\
& D = 1 + \sum_{i=1}^{11} T_{id} + T_{8d} \cdot (T_{6d} + T_{7d}) \\
& \quad + T_{1d} \cdot (T_{2d} + T_{3d} + T_{4d} + T_{6d} + T_{7d} + T_{9d} + T_{10d} + T_{11d})
\end{aligned}
\tag{2.6}
$$

2.1.4 Stability analysis[1]

In order to assess the stability of the overall system, pole-zero diagrams were plotted (Figure 2.5) sweeping the small-signal resistance r_{ds1} and transconductance g_{m1} of the JFET in a way similar to varying its gate voltage. Figure 2.5 shows that all poles have a negative real part as required for stability (some poles and zeroes at high frequencies were omitted from the diagram for convenience). The range of r_{ds1} values (from 2.3 Ω to 23 kΩ) applied to the transfer function (2.6) of the analytical model is suitable for producing the typical dv/dt slopes of modern power devices. Of course, the g_{m1} was varied in accordance with r_{ds1}. Although the circuit involves many feedback loops, it exhibits stable behaviour over a wide range of values for the parameters, and the experimental tests confirmed this conclusion.

Electric (SPICE) simulations, pertaining the full symmetric circuit, presented in [66], were used to verify the model described in the previous section. With respect to the circuit of Figure 2.2, the prototype used for experimental testing uses a different high-side circuit, constituted by a simple pMOS. Moreover, the JFET J_L is replaced

[1]This section describes work done together with Giorgio Pietrini, PhD student at University of Parma, as part of his work about WBG devices in avionics applications.

Table 2.1: Sub-expressions of the transfer function.

Base terms
$d_1 = R_c^{-1} + s\left(C_{gs1} + C_{gd1}\right)$
$d_2 = R_1^{-1} + R_2^{-1} + r_{ds1}^{-1} + s\,C_{gd1}$
$d_3 = R_2^{-1} + s\left(C_l + C_{gd2}\right) + r_{ds2}^{-1}$
$d_4 = R_g^{-1} + s\left(C_{gs2} + C_{gd2}\right)$
$d_5 = R_s^{-1} + r_{ds2}^{-1} + s\,C_{gs2} + g_{m2}$
Denominator terms
$T_{1d} = -\frac{s\,C_{gd1}\cdot\left(s\,C_{gd1}-g_{m1}\right)}{d_1 d_2}$
$T_{2d} = -\frac{s\,C_{gd2}\cdot\left(s\,C_{gd2}-g_{m2}\right)}{d_3 d_4}$
$T_{3d} = -\frac{s\,C_{gd2}\cdot\left(s\,C_{gs2}+g_{m2}\right)\left(r_{ds2}^{-1}+g_{m2}\right)}{d_3 d_4 d_5}$
$T_{4d} = -\frac{r_{ds2}^{-1}\left(r_{ds2}^{-1}+g_{m2}\right)}{d_3 d_5}$
$T_{5d} = -\frac{R_2^{-1}\cdot A_v\cdot R_g^{-1}\cdot\left(s\,C_{gs2}-g_{m2}\right)\left(r_{ds2}^{-1}+g_{m2}\right)}{d_2 d_3 d_4 d_5}$
$T_{6d} = -\frac{R_g^{-1}\cdot A_v\cdot\left(s\,C_{gs2}+g_{m2}\right)}{d_4 d_5}$
$T_{7d} = -\frac{s\,C_{gs2}\cdot\left(s\,C_{gs2}+g_{m2}\right)}{d_4 d_5}$
$T_{8d} = -\frac{R_2^{-2}}{d_2 d_3}$
$T_{9d} = -\frac{R_2^{-1}\cdot A_v\cdot R_g^{-1}\cdot\left(s\,C_{gd2}-g_{m2}\right)}{d_2 d_3 d_4}$
$T_{10d} = \frac{r_{ds2}^{-1}\cdot A_v\cdot R_g^{-1}\cdot\left(s\,C_{gd2}-g_{m2}\right)}{d_3 d_4 d_5}$
$T_{11d} = -\frac{r_{ds2}^{-1}\cdot s\,C_{gs2}\cdot\left(s\,C_{gd2}-g_{m2}\right)}{d_3 d_4 d_5}$
Numerator terms
$T_{1n} = \frac{1}{d_3}$

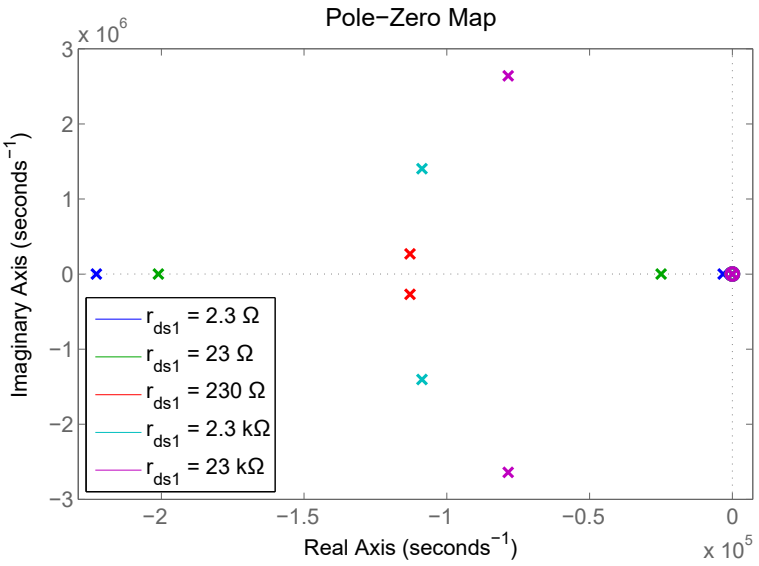


Figure 2.5: Pole-zero diagram of transfer function.

by the series of an n-channel MOSFET and a resistor, in order to generate abrupt steps. Resistor R_{1L} is replaced with a trimmer, to manually control the actuated resistance. The components used are: *OPA4350* operational amplifier, *IRFRC20* nMOS (both for M_2 and M_{step}), *VP2410L* pMOS as active pull-up. Passive components are $R_1 = 50\,\text{k}\Omega$ trimmer, $R_2 = 47\,\text{k}\Omega$, $R_G = 100\,\Omega$, $R_S = 1\,\Omega$, $R_{step} = 1\,\Omega$, $C_L = 1\,\text{nF}$ (to mimic the input capacitance of the main power switch). OPA4350, despite having 35 MHz bandwidth and $22\,\text{V}/\mu\text{s}$ slew-rate, imposed some limitations on the voltage range, being single supply and withstanding only 7 V. Using such component, no negative output voltage, with respect to the main power switch source terminal, could be supplied. Switch commands and stimulus signals were delivered to the circuit using a *TTi TG101A* function generator, data retrieved with a *LeCroy HDO6034* oscilloscope and analysis in the frequency domain was carried out off-line.

The first test to be performed was the generation of large signal commanded steps; associated results are shown in Figure 2.6, where generation of steps with four different fall times is presented. Despite some minor ringing immediately before and after the voltage transition, the shape of the transient response is merely a pure exponential one: being the load capacitive, it means that the circuit is behaving like a commanded resistor.

It is important to observe that during the non-driving phase (generating high rail voltage, for the pull-down circuit analyzed) the operational amplifier should not be driven open loop, in order to maintain a fast response. What is being done is to force the generation of a high, yet finite, resistance. In this way, the amplifier operates always with low differential voltage and fast switching response. The best falling time recorded is 180 ns, which is nearly ten times slower than the speed needed for the effective use of the circuit with wide band-gap devices. It is believed that this performance can be hugely improved by an accurate selection of amplifier and MOSFET: the op-amp output saturates in this extreme condition, limiting the waveform steepness. Higher MOSFET conductivity can obviously be obtained with larger overdrive: greater MOS gain, lower threshold voltage and wider op-amp supply are several means by which the reduction of fall time can be achieved.

Other experiments involved small signal response and bandwidth evaluation.

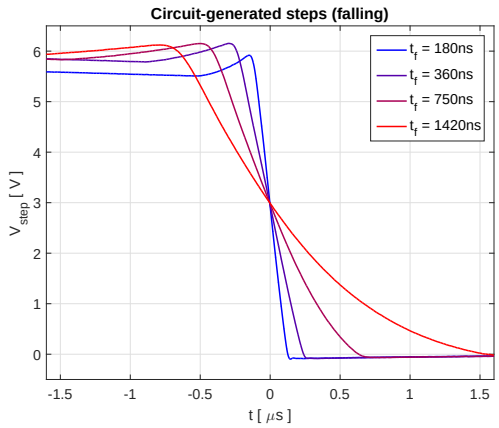
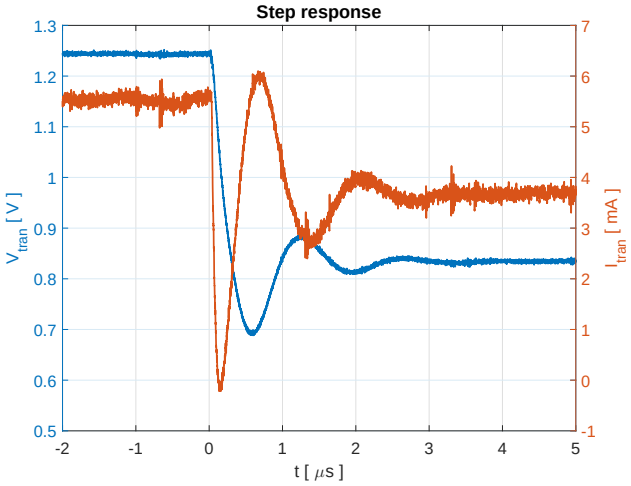


Figure 2.6: Experimental measurement of the circuit generated steps, with command resistance as parameter, generating different falling times.

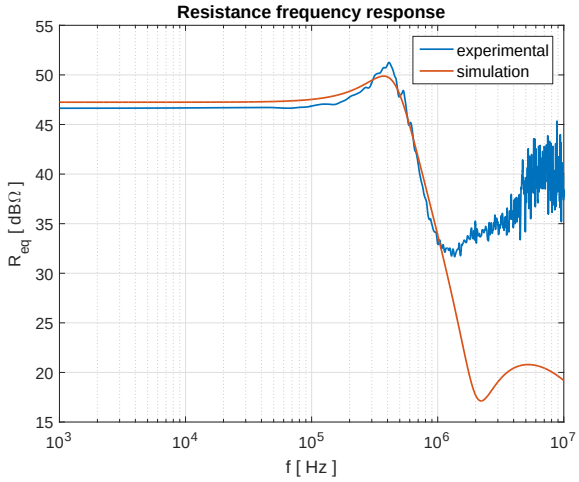
These measurements were done setting the feedback trimmer to a particular value, and forcing a small amplitude (500 mV-wide) falling step. Results over time are plotted in Figure 2.7a, where an equivalent resistance of around $R_{eq} = 220\,\Omega$ is being actuated. This value holds only during the steady-state phase: close to the triggering event, the limited bandwidth results in a different value of effective resistance.

Figure 2.7b depicts the experimental frequency response of the VCPR (in blue) and Bode diagram obtained from the SPICE simulation (in red). These results are obtained as follows: voltage and current values from Figure 2.7a are directly transformed using FFT algorithm, gathering the Discrete Fourier Transform of the impulse response divided by frequency. The ratio of these transforms is then computed, making the divide-by-frequency term, common to both, disappear. The frequency response obtained in this way is equivalent to directly dividing the transform of voltage by that of current *impulse* responses. The value of 47 dBΩ at low frequency is indeed correspondent to $R_{eq} = 220\,\Omega$ in DC.

The Bode diagram (in red) is directly obtained from the small signal AC analysis in SPICE simulator. Figure 2.7b shows a very good agreement between real world and simulation. A significant difference is noticeable at high frequencies ($f > 1$ MHz);



(a) Experimental circuit step response, representing output voltage and current.



(b) Comparison of simulation and experimental results of the circuit frequency response.

Figure 2.7: Experimental responses of the Voltage Controlled Power Resistor circuit.

Table 2.2: Experimental measurement of the circuit-generated resistance bandwidth.

Equivalent DC resistance R_{eq} [Ω]	10	30	100	300
Bandwidth BW[kHz]	37	95	200	176

this is believed to be ascribable to inaccurate modeling of high frequency capacitive and inductive parasitic components in SPICE.

The bandwidth, in this case, is defined as the difference from the DC value, regardless of the Bode diagram drifting upwards or downwards; the usual 3 dB threshold is adopted. This definition allows to spot errors in equivalent resistance even in presence of resonant-like behavior. Table 2.2 shows bandwidth measurements for different actuated R_{eq} values. A strong dependence of the bandwidth on the equivalent DC resistance is noticeable, with slower response in correspondence with lower resistance values, hence when device is supposed to switch faster. A non-monotonic trend is also visible, and it could be referable to the appearance of resonant behavior in some cases. These results are described in more detail in [67].

2.2 Voltage-Resistance stepped gate driver

The voltage controlled power resistor circuit allows to control the switching waveforms, but it lacks the possibility to manage the on state losses of the power switch. These do not depend on the gate driver impedance, but on its output voltage during the commanded on-state. Addressing the loss component connected to conduction adds a degree of freedom to implement various types of controls. It also enables to act on losses without changing the output waveform spectrum and EMI, making the AGD more versatile.

A flexible gate driver should thus include both capabilities, i.e. it should be able to change both conduction and switching losses. To do so, an AGD was developed on purpose, and its output was quantized: the system engineer can choose among different discrete output resistance values and voltages.

In WBG devices, it is important to achieve fast actuation of the commanded

quantities; the use of discrete values for voltages and resistances helps in this way, since it is sufficient to switch among different circuit parts, as it will be shown later. Moreover, the possibility to control the gate driver output voltage, even if born with the desire to control conduction losses, can improve the resolution in switching phases, since this voltage, together with the output resistance, determines the current that can be sunk or drained to the gate capacitance.

This gate driver was developed mainly as a part of a test bench for electrical drives to be used in aircraft, the FP7 project ALEA, devised from the Clean Sky consortium [68, 69, 70]. The target of this project was to assess the reliability of the whole drive assembly (motor, cables, converter, ...) by stimulating the device under test with different types of stress: mechanical, thermal, electric. This last point was achieved by using a WBG converter equipped with the aforementioned AGD, to change the output voltage time derivative dynamically, thus exploring different fault mechanisms, as those connected with reflections on the power cables.

2.2.1 Quantized driver architecture

The simplified schematic of the gate driver is reported in Figure 2.8, while the full schematic can be found in appendix A. This relates to driving of a single device, and should be repeated for each power switch of the converter. The primary voltage supply can be shared among the different devices, since insulation is provided on board, as it often happens in these cases.

The high-state voltage value is set by dynamically changing the feedback network of the first DC/DC converter, that transforms the primary supply voltage before the insulation layer, provided by a commercial DC/DC converter with transformer. Since the feedback network is made by resistors, it can easily be changed in discrete values by switching different resistors in parallel or series connection. Due to the easier hardware implementation, multiple parallel configurations were chosen. Each resistor can thus be included or excluded by a simple open-drain pin, coming from a microcontroller or an IO expander. There are two possible limitations related to this implementation: firstly, changing the feedback network can determine stability issues, so values should be chosen carefully. Then, the change in voltage is supposed to be slow, mainly

due to the fact that after changing the command, some time is needed to charge or discharge the output and intermediate capacitances to the desired value. This problem is addressed in Section 2.2.3.

To be able to switch among discrete output resistance values, many traditional gate driver integrated circuits were paralleled. To do this effectively, the point of common contact is the gate terminal itself and all the gate driver ICs share the same PWM signal. Each gate driver can be driven in a high-impedance state by an enable command: the pattern fed to the enable binary vector determines the number of operating gate driver units and hence which resistors participate in the parallel making the gate resistor. More states can be added if a diode is included for each resistor, allowing to decouple the charging value from the discharge one.

The resulting output waveforms generated by this gate driver are documented in Figure 2.9, where all the states are captured by means of oscilloscope persistence, looking at the voltage on a capacitive load. The gate driver is effectively capable of changing both time derivative and steady-state value of the voltage. A thermal study was also performed on the driver itself, in order to find the existence of critical point from the thermal point of view. The results are depicted in Figure 2.10, where the thermal images of bottom and top sides of the gate driver are represented. As it can be seen, higher temperature occurs on one of the output switching resistances: to achieve a wide range in regulation, the base resistance values are asymmetric (see next section). In this test the switching frequency was set to 400 kHz with a capacitive load of 7 nF.

2.2.2 Discretization values and optimization

Since the presented gate driver can actuate only a limited number of values and states, care must be taken to choose each value appropriately, keeping in mind the parameters of the driven power device and the application. The first consideration should be towards the possible desaturation of the power switch. A switch is said to “desaturate” (adopting also for gated devices the nomenclature used for bipolar junction transistors) when it goes out of the region with low output voltage (i.e. linear region for MOSFETs); this results in a large amount of conduction losses. Since

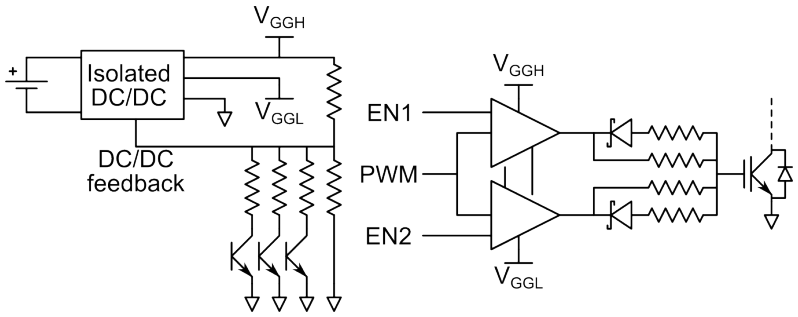


Figure 2.8: Simplified schematic of the gate driver actuating discrete values of voltage and resistance.

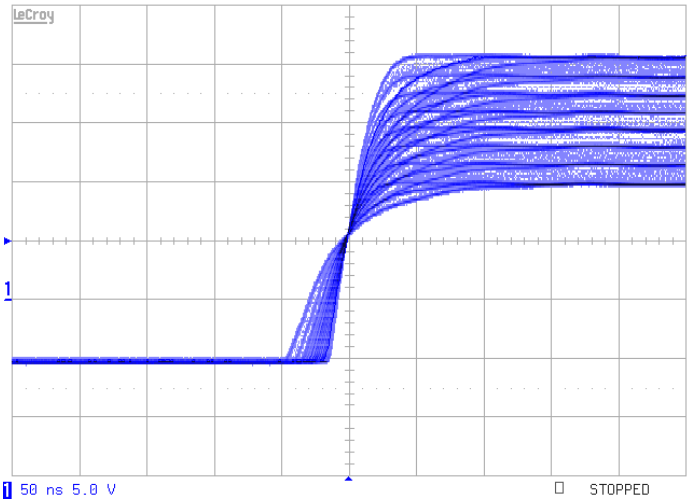


Figure 2.9: Output gate-source voltage waveforms of the implemented quantized gate driver with a capacitive load. The different values of output voltage and resistance are plot, with oscilloscope set in persistence mode. Time axis 50 ns/div, vertical axis 5 V/div.

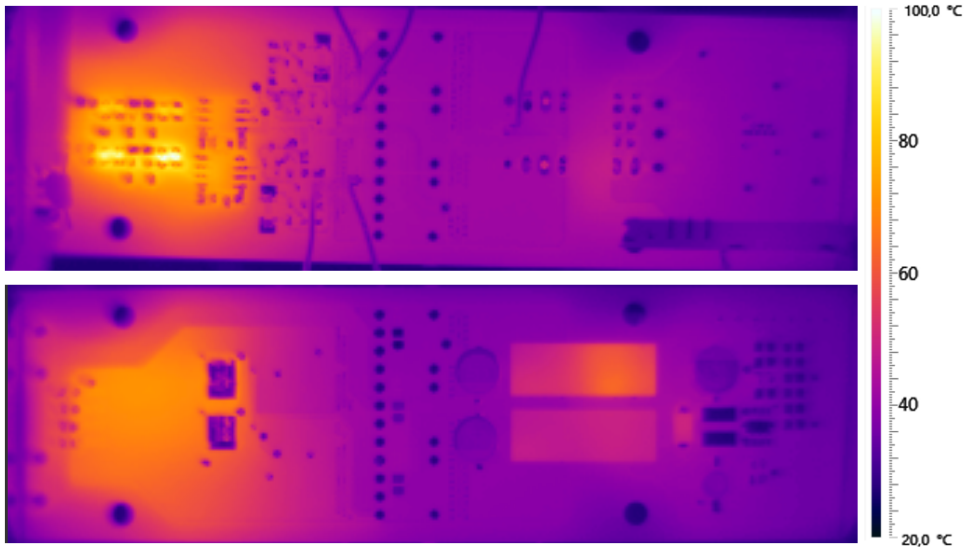


Figure 2.10: Thermal image of top and bottom sides of the quatized gate driver. In the top side (top figure) the hot-spot is located on the output amplifiers and resistors. In the bottom side, part of the heat of the top side is noticeable on the left, while the hot-spot is on the negative supply isolated DC/DC converter.

the desaturation marks the boundary of the voltage controlled current source region (VCCS-region), the load current determines the minimum value of the gate voltage below which desaturation will occur. This implies that the lowest among the voltage values should be above the desaturation voltage. Some exceptions to this point can be made in other applications, as Section 2.3 will discuss.

Moreover, it is useless to have values above the maximum suggested one for the gate of the power device. For SiC MOSFETs, the typical values are usually included in the [10 V; 20 V] range. This range can be narrowed, especially on the lower bound, if more margin is desired with respect to desaturation. Beyond that, the spacing of the values can be set according to a linear relationship; it is also worth nothing that, since conduction losses do not have a linear relationship with the gate voltage, uneven spacing of voltages could result in even spacing of conduction losses. This point is now neglected and linear spacing is sought.

Referring to Figure 2.8, the output voltage can be determined by knowledge of the input-output characteristic of the first, non-insulated, DC/DC converter and its dependence from the feedback resistor, and on the gain of the secondary, fixed, insulating DC/DC converter. If the number of control open-drain lines is n_l, then the number of values is $n_v = 2^{n_l}$. This results in $n_l + 1$ resistance values R_{xj} to determine ($j = 0, \ldots, n_l$, where R_{x0} is the one that cannot be excluded), since the feedback network has always to preserve a connection to the reference node. Supposing an even spacing of values from V_{min} to V_{max}, the spacing is thus:

$$\Delta V = \frac{V_{max} - V_{min}}{n_v - 1} \tag{2.7}$$

so that each value V_i, with a zero-based indexing, given by binary weighting the command bit vector, is:

$$V_i = V_{min} + i \cdot \Delta V \tag{2.8}$$

The output voltage that is used for the gate drivers is determined if the internal reference voltage of the feedback regulator V_{ref} is known, together with the gain k_{iso} of the insulating DC/DC. If R_h is the high-side resistor of the feedback network, and

Table 2.3: Possible resistance configurations needed to realize eight different voltage values with the discrete gate driver.

i	Binary	Resistance	Conductance
0	000	$R_{l0} = R_{x0}$	$G_{l0} = G_{x0}$
1	001	$R_{l1} = R_{x0} \| R_{x1}$	$G_{l1} = G_{x0} + G_{x1}$
2	010	$R_{l2} = R_{x0} \| R_{x2}$	$G_{l2} = G_{x0} + G_{x2}$
3	011	$R_{l3} = R_{x0} \| R_{x1} \| R_{x2}$	$G_{l3} = G_{x0} + G_{x1} + G_{x2}$
4	100	$R_{l4} = R_{x0} \| R_{x3}$	$G_{l4} = G_{x0} + G_{x3}$
5	101	$R_{l5} = R_{x0} \| R_{x1} \| R_{x3}$	$G_{l5} = G_{x0} + G_{x1} + G_{x3}$
6	110	$R_{l6} = R_{x0} \| R_{x2} \| R_{x3}$	$G_{l6} = G_{x0} + G_{x2} + G_{x3}$
7	111	$R_{l7} = R_{x0} \| R_{x1} \| R_{x2} \| R_{x3}$	$G_{l7} = G_{x0} + G_{x1} + G_{x2} + G_{x3}$

R_{li} the low-side one, related to the i-th voltage, the output is given by:

$$V_i = k_{iso} V_{ref} \left(1 + \frac{R_h}{R_{li}}\right) \tag{2.9}$$

Equating (2.8) with (2.9) for $i = 0, \ldots, (n_v - 1)$ results in a system of n_v equations. This is well-determined mathematically, but usually over-determined practically, since the resulting R_{li} are electrically related, coming from the parallel of the active R_{xj}. The easiest way to determine the $n_l + 1$ resistors R_{xj} is to solve the previously described system for those values of R_{li} that come from a configuration made up of the least number of resistors. Table 2.3 shows the possible configurations in the case of $n_l = 3$, matched with each index and binary command vector for the open-drain switches. It is clear that the first value to be determined is R_{x0} directly from $V_0 = V_{min}$, then R_{x1} from V_1, then R_{x2} from V_2 and eventually R_{x3} from V_4. It can be demonstrated that if even spacing is used, also all other voltage constraints are satisfied, too. Some minor change in the actuated values can also result from the limited commercial availability of some values.

A much simpler approach, that is useful if uneven spacing is sought, is to rewrite

Table 2.4: Example of calculation for dimensioning the discrete gate driver output voltages.

(a) Values of resistance and conductance needed to determine possible output voltages for an example gate driver.

i	Binary	R_{li} (kΩ)	G_{li} (µS)	V_i (V)
0	000	343	2.92	10.0
1	001	257	3.89	11.4
2	010	205	4.87	12.8
3	011	171	5.85	14.2
4	100	147	6.82	15.7
5	101	128	7.80	17.1
6	110	114	8.78	18.5
7	111	103	9.75	20.0

(b) Parameters needed to obtain eight evenly spaced discrete output voltages from the gate driver.

Parameter	Value	Unit
V_{min}	10	V
V_{max}	20	V
V_{ref}	1.195	V
k_{iso}	4.8	–
R_h	255	kΩ
R_{x0}	343	kΩ
R_{x1}	1024	kΩ
R_{x2}	512	kΩ
R_{x3}	256	kΩ

(2.9) using the conductance $G_{li} = 1/R_{li}$:

$$V_i = k_{iso} V_{ref} (1 + R_h G_{li}) \tag{2.10}$$

This greatly simplifies the total conductance, as it is shown in the last column of Table 2.3, transforming the parallel operation into a simple sum. A possible example of resulting values is summarized in Table 2.4.

The results presented show a geometric relationship between R_{xi} or G_{li}, for $i \neq 0$. This condition is sufficient in order to have linear spacing regardless of the number of levels. Starting from (2.10), the voltage step between two adjacent values (that is constant for linear spacing) can be computed as:

$$\Delta V = V_{i+1} - V_i = k_{iso} V_{ref} R_h (G_{l(i+1)} - G_{li}) \tag{2.11}$$

so that

$$\Delta G = G_{l(i+1)} - G_{li} = \frac{\Delta V}{k_{iso} V_{ref} R_h} \tag{2.12}$$

This means that conductances G_{li} should be linearly spaced as well. This can easily be accomplished using a 2 ratio between the G_{xi}, as from fundamentals of the binary numbering system. Only $G_{x0} = G_{l0}$, determining the starting value, is out of this geometric proportion.

A similar approach to that used for voltages can be applied to the choice of gate resistances, too. In this case, since the dependence of switching losses on gate resistance is not so clear, both linear and logarithmic spacing of values can be used and the two results for the sizing are presented as well.

Since the number of gate driver ICs is determined by the base-2 logarithm of the desired number of resistance levels decremented by one, the final circuit can become quite expensive. For this reason, the prototype was devised with only two driving units, leading to three different values. The fourth level corresponds to both drivers disabled and it is retained as a convenient safety feature.

Suppose that $G_1 = G_b$ is the conductance at the output of the least significant gate driver IC (configuration $01_2 = 1_{10}$). The other will have conductance $G_2 = aG_b$, with $a > 1$. Since the third level, corresponding to both the ICs enabled, presents a conductance that equals the summation of both, it results in $G_3 = (a + 1)G_b$. Logarithmic spacing can be obtained by setting:

$$\frac{G_3}{G_2} = \frac{G_2}{G_1} \quad \Rightarrow \quad \frac{a+1}{a} = \frac{a}{1} \quad \Rightarrow \quad a^2 - a - 1 = 0 \tag{2.13}$$

that is the well-known equation describing the *golden ratio*. It can be straightforwardly solved in its only positive solution $a_{log} = \varphi = 1.61803\ldots$ It is worth noting that the result is the same if logarithmic spacing between *resistances* is sought, due to the reciprocal relationship between the two quantities. The linear spacing of the conductances can be obtained by solving:

$$G_3 - G_2 = G_2 - G_1 \quad \Rightarrow \quad (a+1) - a = a - 1 \quad \Rightarrow \quad a_{linG} = 2 \tag{2.14}$$

while the equation for linear resistance spacing is different (where $R_i = 1/G_i$):

$$R_1 - R_2 = R_2 - R_3 \quad \Rightarrow \quad (a-1)(a+1) = (a+1) - a \quad \Rightarrow \quad a_{linR} = \sqrt{2} \tag{2.15}$$

It is clear from (2.13)–(2.15) that the base conductance level G_b, i.e. the value of output conductance for the least significant driver, can be set freely, in accordance

Table 2.5: Dynamic range comparison of different ratios among output conductances and resistances.

Enable bits	G_i	Value	$(G_i/G_b)_{linG}$	$(G_i/G_b)_{linR}$	$(G_i/G_b)_{log}$
00	G_0	0	0	0	0
01	G_1	G_b	1	1	1
10	G_2	aG_b	2	$\sqrt{2} \approx 1.414$	$\varphi \approx 1.618$
11	G_3	$(a+1)G_b$	3	$1+\sqrt{2} \approx 2.414$	$\varphi + 1 \approx 2.618$

with the suggested gate resistance of the power device in use. The dynamic range for the linear spacing is slightly wider than the logarithmic one if conductances are concerned, while it is lower in case of linear resistance spreading. This is affirmed in Table 2.5. It would also be clear in the following, especially from Section 3.2 onward, that the resistance relationship, despite being less comfortable to manipulate, is more interesting from the loss point of view.

The statements above can be generalized easily to develop gate drivers that are capable of realizing a larger number of output resistance levels, remembering that the multiplicity of degrees of freedom is given by the number of gate driver ICs employed.

2.2.3 Bandwidth enhancement

The circuit of Figure 2.8 presents an inherent limitation in the bandwidth of the voltage actuation. This comes from the fact that the output driver IC supply voltage is changed dynamically in accordance with the structure of the feedback network of the DC/DC converter on the primary side. Power integrity demands that filter capacitance is provided on the supply voltage of the driver: this implies that a certain amount of current is needed to change the voltage within a specified amount of time. This entails a non-linear bandwidth limitation with respect to voltage regulation.

Moreover, the picture is worsened by the usual asymmetry in sourcing and sinking capabilities of power converters: the first is commonly higher, even tenfold. This implies an asymmetric bandwidth limit, usually worse when sinking current, that is

when the output voltage is decreased.

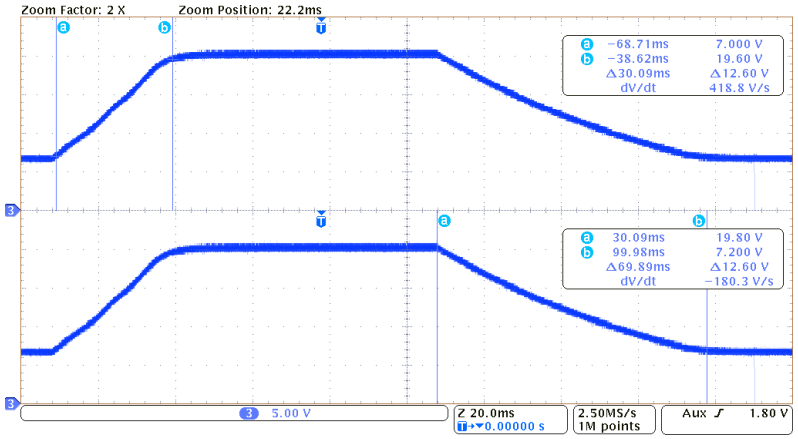
The limitations described above can be lessened by properly designing the DC/DC converter, in order to have a high transient current rating and almost identical sink and source capability. This is effective but difficult to implement if off-the-shelf components are to be used. A simpler, yet inefficient solution, is to increase the static loss on the secondary side. This makes the load heavier to source, but easier to sink, and this can improve overall performance if the sinking current limit is the most compelling one.

Care must be taken when choosing the amount of dissipation that is added on the secondary side, since it degrades the filtering capability of the capacitor. This worsens the ripple value, that is generally increased. This brings also prospective degradation of EMI indexes, due to the generally wide bandwidth of the switching signal. The solution adopted in the gate driver under test is a mixed one: the output capacitance was slightly lowered, while introducing a limited static resistance in parallel with the output rail. The general improvement in the behavior is summarized in Figure 2.11.

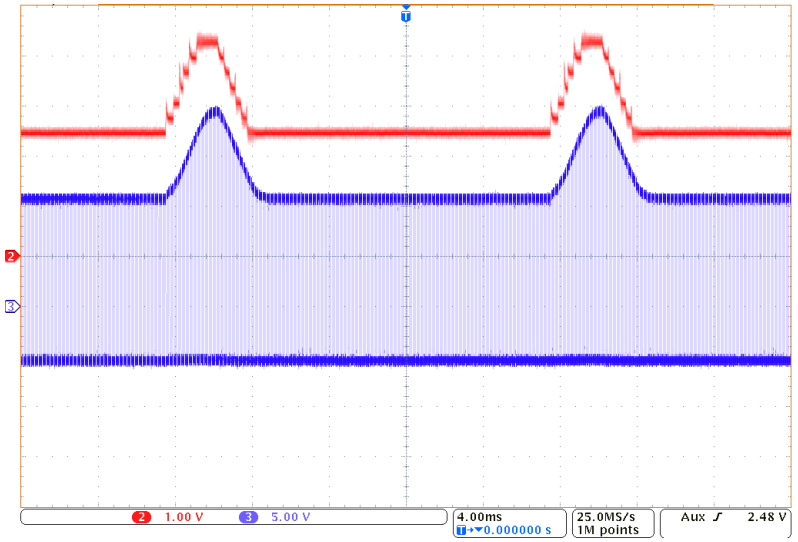
2.3 Shoot-through-ready gate driver

A novel gate driver circuit that was conceived in this PhD program is the so-called *shoot-through-ready* gate driver. Its purpose is to activate a new loss mechanism in the power device, with the objective to control the temperature of the part. It is named after its ability to activate losses due to shoot-through of the DC supply, when used with another identical unit in a half-bridge power converter. The most innovative point of this circuit is that the shoot-through is controlled, both in time and current. This allows to perform the operation without damaging the device and also to easily control the power loss used to heat the device because of its linear relationship with the duration of the shoot-through pulse.

This driver is especially designed not to alter the output voltage nor current, even during the shoot-through condition. This is seen as a plus, since the loss control can be achieved in a transparent way with respect to device functional quantities. The modulation pattern chosen, presented in the next section, makes this gate driver



(a) Before optimization; no PWM switching.



(b) After optimization of supply capacitance and static loading (with PWM switching); primary side voltage (red), secondary side voltage (blue).

Figure 2.11: Gate driver bandwidth limitation in changing voltage.

unable to act on the output waveform: no modification in transients can be obtained. This restriction does not exist anymore if a different pattern is used, that can place the intermediate voltage pulse inside the device switching phase.

2.3.1 Modulation patterns

For shoot-through to occur, a DC supply with a half-bridge should be identified. As already shown in Section 1.3.1, many complex converter architectures can be broken up into units constituted by half-bridges. This is true not only for the legs of traditional three-phase inverters, but also for DC/DC converters, where the basic unit can be easily identified in case of synchronous rectification.

The shoot-through condition is usually avoided by never switching on the high- and low-side of the half-bridge simultaneously. This is the reason for the inclusion of dead-time in PWM patterns and for the existence of some interlock features in the monolithic drivers for half-bridges. The shoot-through condition can be dangerous if not limited in time, or too high a current can build on the leg path, resulting in a DC supply short-circuit and potential destruction of the bridge itself.

A dangerous shoot-through happens if the "on" gate command is identical for devices on both sides. Turning on one device with the nominal gate voltage and the other, complementary, with a reduced one allows to limit the shoot-through current and can be even "invisible" on the output if the new gate voltage level is chosen properly. The key point is to drive the device to be heated in the saturation region (VCCS, using MOSFET nomenclature) instead of the linear one: this allows to limit the current and not to make the drain-source voltage drop, resulting in the shoot-through not being noticeable from the output. The choice of the appropriate third-level voltage will be object of discussion in Section 2.3.2, and will be analyzed further both in Chapters 3 and 4. This new gate voltage level adds to the traditional turn-on and turn-off ones.

This approach is safe for the device provided that the shoot-through pulse is narrow enough; when this holds, the controlled shoot-through is indistinguishable from the current rise and fall phases that occur during switching (see Section 1.3.1), at least from loss and device stress point of view. To fulfill all these requirements, the third-level pulse should appear in the middle of the turn-on pulse of the complementary device,

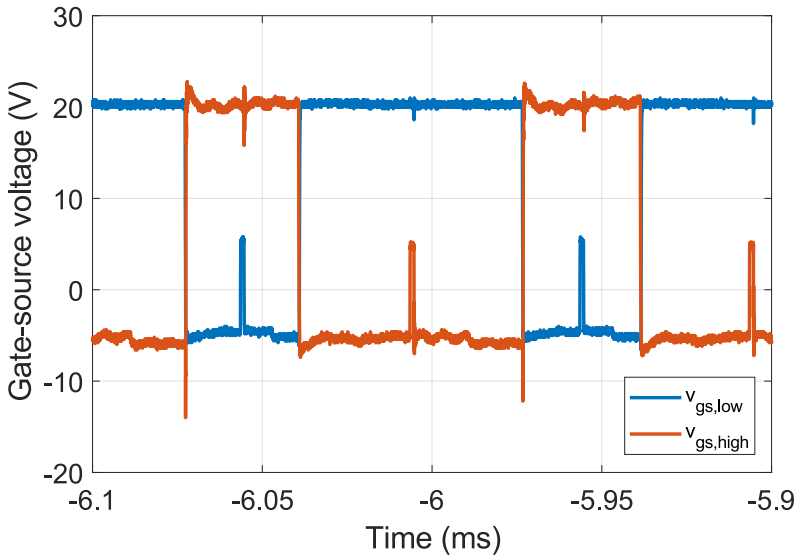


Figure 2.12: Gate pattern for high- and low-side devices, showing the third voltage level needed for the controlled shoot-through of the half-bridge.

in order to be as far as possible from the switching phases, where spurious current conduction could be detrimental for other aspects, such as output spectrum. The resulting pattern is depicted in Figure 2.12, where the 7 V pulse is clearly noticeable against the 20 V on-state voltage and the −5 V used at turn-off.

2.3.2 Three-level architecture

The challenge of implementing the new level lays in the very demanding bandwidth requirement. In fact, since the shoot-through pulse (ST-pulse) should occur while the other device is on, its duration is limited by the time length of the narrowest fully-on pulse, that in turns is connected with the minimum duty-cycle d_{min}. If f_{pwm} is the switching frequency, the shoot-through pulse width t_{st} must be be $t_{st} < d_{min}/f_{pwm}$, where the strict inequality comes from the need to accommodate some room for the switching transients when all the edges come close to each other.

For example, when WBG devices are used, switching frequencies in the range of

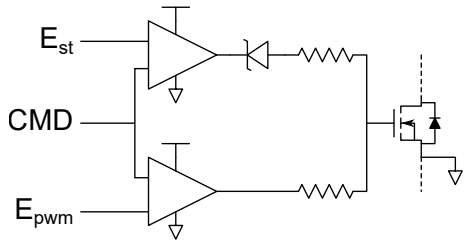


Figure 2.13: Schematic of the shoot-through-ready gate driver.

[50 kHz; 150 kHz] are quite common; in the hypothesis of a bootstrapped gate driver, $d_{min} \approx 2\%$, so that the pulse should be $t_{st} < 133$ ns. Such a fast voltage change cannot be achieved from the discrete gate driver presented in Section 2.2, since the control loop of the DC/DC converter is too slow. The enable signals, used to change the output resistance, can be much faster. In order to make the driver fast enough, its scheme should be rearranged as in Figure 2.13, and the signals reported in Figure 2.14 used. Both the gate amplifiers are fed with the same command pattern, presenting two transitions in each period, one corresponding to the fully-on pulse (PWM-related) and another to the ST one. The driver with Zener diode on output is enabled during the ST phase, while the other is enabled during the normal on state. The resulting signals are thus complementary, and can be generated without any dead-time, since they relate to the same device. Their polarity should change in the middle of the zero-level pulses of the PWM, in order to leave enough room for the extreme pulse widths, minimizing the impact of the time needed for the amplifier to enter or leave the enabled state.

It is clear that the Zener diode plays a key role in determining the magnitude of the third voltage. In fact, when its driver IC is enabled, the diode turns on and its voltage subtracts to that supplying the IC itself. Hence, the shoot-through voltage is determined by the IC supply and the Zener rating. The nominal value of the voltage should be determined following several criteria. First, the device must be driven in saturation region during shoot-through; this means that the third level must be below the Miller voltage for the instantaneous drain current of the power device. Since this value changes with the output current, its lowest limit should be considered. Secondly, the ST voltage needs to be above the threshold of an amount such that the drain current

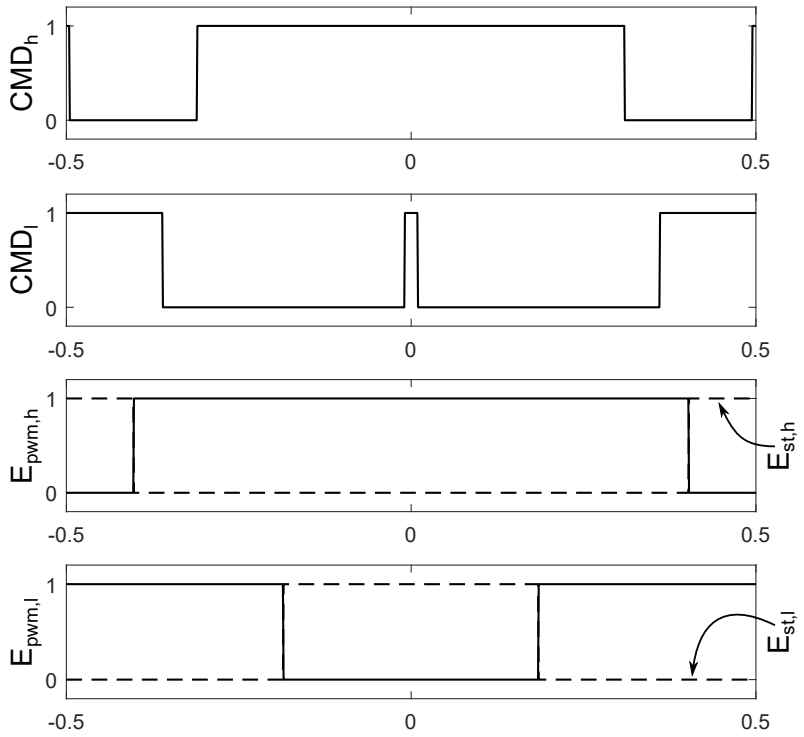


Figure 2.14: Patterns of enable and PWM signals for the shoot-through-ready gate driver.

is limited; this value depends on the transconductance of the particular power switch used.

Moreover, the overall instantaneous power, averaged by the ST pulse length over a switching period, should be high enough to achieve the target temperature in case ATC is implemented; in this case the ST pulse is related also to nominal losses and load profile of the device over time. It is worth noting that a trade-off exists between the maximum ST pulse width ($t_{st,max}$), the minimum duty-cycle d_{min} and this voltage $V_{gs,st}$: higher gate voltages in ST allow to shrink the pulse at constant losses. If no other criteria are examined, this results in a degree of freedom for the system designer; further analysis will show some optimizations in the choice of $V_{gs,st}$.

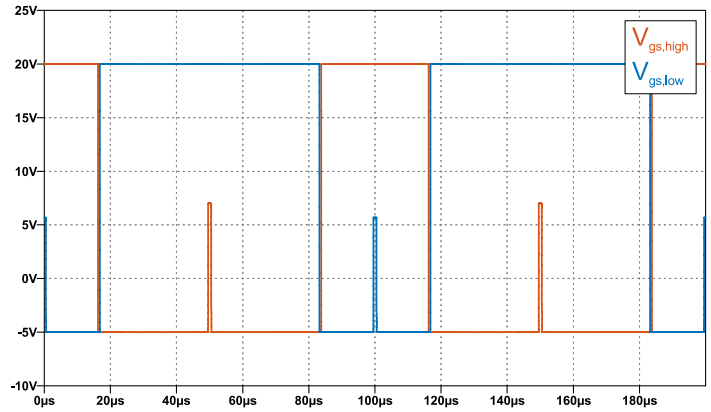
In Figure 2.15 the half-bridge output waveforms with the shoot-through gate driver for both power switches are reported as from SPICE simulation. The gate pattern of Figure 2.15a is the simulation equivalent of that in Figure 2.12; the output waveforms of Figure 2.15b should be compared to the experimental results in Figure 2.17.

Figure 2.16 shows that the output waveforms of both current (i_O) and voltage (v_O) are almost insensitive to the controlled shoot-through events (A and B). The drain current of the low-side MOSFET is depicted in red. The ripple of i_O is large due to the limited load inductance; in any case the short circuit current flows along the leg, and does not effect the output. The A event relates to the "proper" ST event of the low-side device, since the current conduction occurs when the power device is off, while the B event is connected to the ST event of the high-side device. Of course, this current flows also into the low-side device, adding to the load current. It is worth noting that, due to the fact that the drain-source voltage of the low-side switch is equal to almost full DC supply during the A event, important power losses will appear in this case. This corresponds with simulation outcomes and supports the validity of the proposed gate driver when loss control is desired without affecting the output.

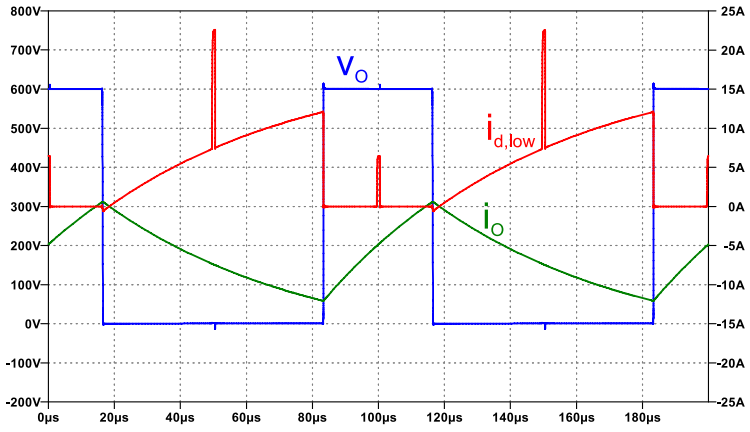
The loss distribution and magnitude is best understood in Figure 2.17, where the low-side device losses are represented. It can be noted that the instantaneous power during ST (at time $t = 0$ and $t = 100\,\mu$s) is very similar to that occurring during the switching phases: this is a clear sign that the new loss mechanism introduced by the gate driver pushes the switch in a safe operating point, provided the pulse duration is

narrower than the short-circuit rating of the device and with an overall energy that is manageable by the components itself.

Quantitative aspects are of course crucial for this type of driving; they will be thoroughly examined in the following chapter, where an in-depth discussion about loss models is dealt with. This is a necessary prerequisite if the proposed AGDs are to be employed for Active Thermal Control.



(a) Gate waveforms for high- (orange) and low-side (blue) devices, of a half-bridge with controlled shoot-through.



(b) Output waveforms; output node voltage (blue), low-side device drain current (red), load current (green).

Figure 2.15: Waveforms for a half-bridge with shoot-through-ready gate driver (simulation).

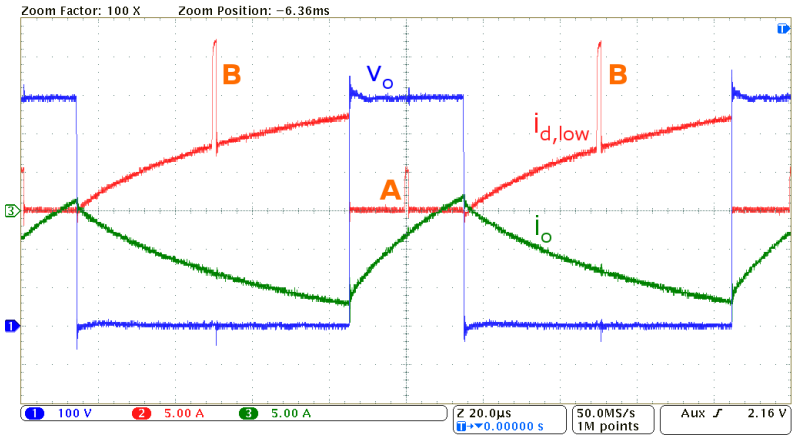


Figure 2.16: Experimental output waveforms for a half-bridge with shoot-through-ready gate driver.

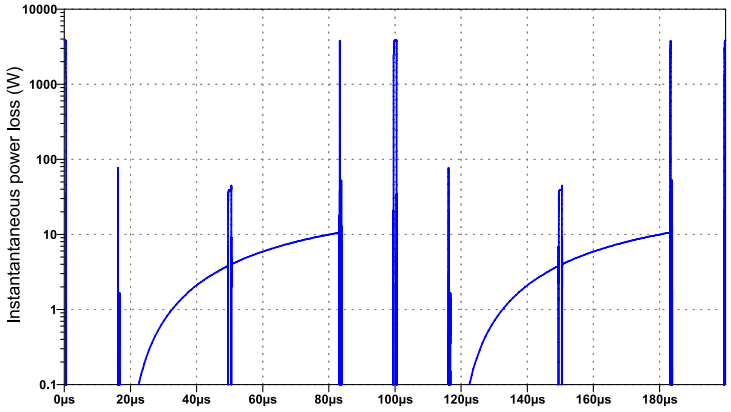


Figure 2.17: Instantaneous power loss of the low-side device: conduction, switching and shoot-through losses are shown.

Chapter 3

Loss modeling for power devices

We have no idea about the 'real' nature of things.
The function of modeling is to arrive at descriptions which are useful.

– R. Bandler and J. Grinder, 1979

The modeling of losses in power converters has a great importance for many different design aspects. It impacts the sizing of the cooling system, it can guide the choice of both converter architecture and device type and model, it can be strictly connected with efficiency and thus be regarded as an optimization parameter.

Accurate loss modeling is something other than a trivial task; it calls for knowledge of many variables, since losses depend on many electric and control parameters (gate voltage, gate resistance, temperature, duty-cycle, . . .). Moreover, many device parameters depend on the device junction temperature, that is often unknown and also difficult to estimate.

These reasons contribute to the birth of many different loss models, each with some benefits and disadvantages; some of them will be described and examined, after a preliminary description of the mechanisms behind the generation of device power losses.

3.1 The origin of losses

When operated in Switched-Mode Power Supplies (SMPS), electronic power devices are desired to behave like ideal switches. This means that they should carry current with almost null voltage drop and block high voltages without any current leakage. This behavior is described by operation in two regions: linear and off, respectively, when using the MOSFET nomenclature. For bipolar devices, it is common to call "saturation" the on-state region, colliding with what is usually accepted for MOSFETs [71].

The off-state region can be regarded as ideal for many commercial devices, being the leakage current very low, provided that the device is correctly driven. The same does not hold for the linear region: in this case the on-state voltage drop is rarely negligible, especially for high-voltage devices. The reason for that can be rooted to parasitic resistances (channel and drift) in majority-carrier devices, and to junction threshold voltages in case of bipolar devices (based on minority carrier injection). These non-idealities are the main cause of conduction losses.

Furthermore, the transition between off- and on-states is not instantaneous, and requires the switch operating point to travel in the MOSFET saturation region ("linear" for bipolar devices). Here the device behaves as a Voltage/Current Controlled Current Source (VCCS/CCCS): voltage and current are simultaneously large, and some losses originate, since they are the product of device voltage and current. These are referred to as "switching losses" and they can be attenuated by ensuring as fast as possible switching time between the two ideal regions.

In Chapter 4 the concept of Active Thermal Control (ATC) will be presented, together with the classification of its different typologies. Device-level ATC is one of these and it is based on the possibility to control power switch temperature by action on device power loss. In order to heat the power device in a controlled way using its losses, their natural level needs to be forecast, depending on the load, and some additive losses shall be induced, if necessary, using some specialized system, such as an AGD.

To precisely control the losses, knowledge of their natural level, as well as the

amount to add, shall be linked to the parameters of the actuating circuit. A device loss model is thus of paramount importance for both aspects, giving foundation to device-level ATC; the quality of the implemented ATC is supposed to depend heavily on the model performance, so special care in its development is demanded.

One first difficulty in developing accurate models resides in the dependence of losses not only on "functional" quantities (such as drain current and drain-source voltage), but also on other parameters, that are usually kept constant, once tuned on the particular system (e.g. gate voltage). Moreover, temperature can influence all the internal and external quantities related to power devices, so it shall be taken into account.

Another key point is that instantaneous power loss is a very discontinuous quantity: some assumptions on the real working cycle of the device can lead to "average" models, that can be readily used in ATC implementations. In this work the basic working cycle considered is the PWM cycle: loss models will output the average power loss on this time span.

Summarizing, each loss model should be based on an appropriate working cycle, account for both load parameters and device control adjustable parameters (depending on the gate driver), and also on temperature.

A by-product of the loss model is the Safe Operating Area (SOA) related to the adjustable gate parameters: since they can vary from the nominal ones, too-wide changes in their values can drive the device out of its safe limits. This is particularly important for example to prevent desaturation of the device if its gate voltage is lowered to increase conduction losses: given a specific value of the drain current, there is a lower bound of the gate voltage. If this limit is not respected, the device goes into the saturation region (current-generator behavior) and serious damage can occur, due to the high power dissipation.

3.1.1 Load types

To deeply understand the origin of losses and thus create an accurate model for them, some hypotheses about the architecture of the circuit the device is in are needed. The type of load is part of this scenario, since every load forces different switching profiles,

Table 3.1: Classification of loads based on impedance phase angle.

φ	Load class
0	resistive
$]0, \pi/2[$	resistive-inductive
$\pi/2$	inductive
$]-\pi/2, 0[$	resistive-capacitive
$-\pi/2$	capacitive
$\pm\pi$	regenerative
$]\pi/2, \pi[$	regenerative-inductive
$]-\pi, -\pi/2[$	regenerative-capacitive

with different impact on overall system losses. In sinusoidal steady state, loads can be divided into three broad categories: resistive, reactive, regenerative. The same classification holds for switched-mode circuits, provided that PWM-average values are considered. The load impacts on conduction angle and phase delay, resulting in different loss distributions.

In sinusoidal terms, each kind of load can be classified based on its angle, i.e. the oriented angle from the current to the voltage phasor. The angle thus defined coincides with the phase of the impedance vector. Loads can therefore be classified based on the φ angle, as stated in Table 3.1 and represented in Figure 3.1. Regenerative loads are those that exhibit a negative real part of the impedance; this in turn translates into a negative active power P.

It is possible to describe and identify loads also from a graphical point of view: using voltage and current as the coordinates in a cartesian system, the load waveform is represented as a parametric curve, which shape can be related to the load type. These curves are known as Lissajous figures and are used in many different situations [72].

Figure 3.2 reports Lissajous figures for the different loads described before. Using this representation, it is easy to understand at a glance, and even in experimental

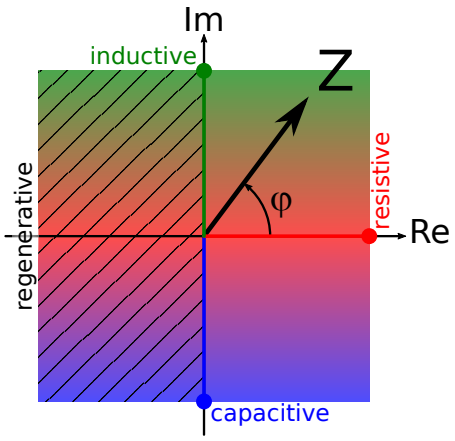


Figure 3.1: Load classification based on impedance phase angles.

conditions, the type of load. In fact, Lissajous figures can be obtained easily with an oscilloscope configured in X-Y mode, with current and voltage probes to feed the channels.

In order to make significant assumptions about the load type from its figure shape, the axes should be normalized: they refer to different quantities (voltage and current), so their value should be divided by the peak value, thus giving a dimensionless quantity in the $[-1, 1]$ interval.

With this convention in mind, the slope of the main axis of the ellipsis can instantly point out if the load is regenerative or not: if it is parallel to I-III quadrant bisector, then the load has a dissipative component and can drain active power from the source; if it is parallel to the other bisector, then the load is regenerative. Analogously, a circumference denotes a purely reactive load, while resistive loads degenerate into segments. Capacitive and inductive loads can be discriminated if the direction of the trace is known: clockwise for inductance and counterclockwise for capacitance.

Lissajous figures are a general tool that can help in identifying the real nature of a load even if it has some non-linearity. In fact, this representation is agnostic from the waveform point of view, with the only exception of the peak value. This means that

it is possible to represent also non-linear loads: Figure 3.3 represents the Lissajous diagram for a rectifier followed by an RL network, as seen from a sinusoidal source.

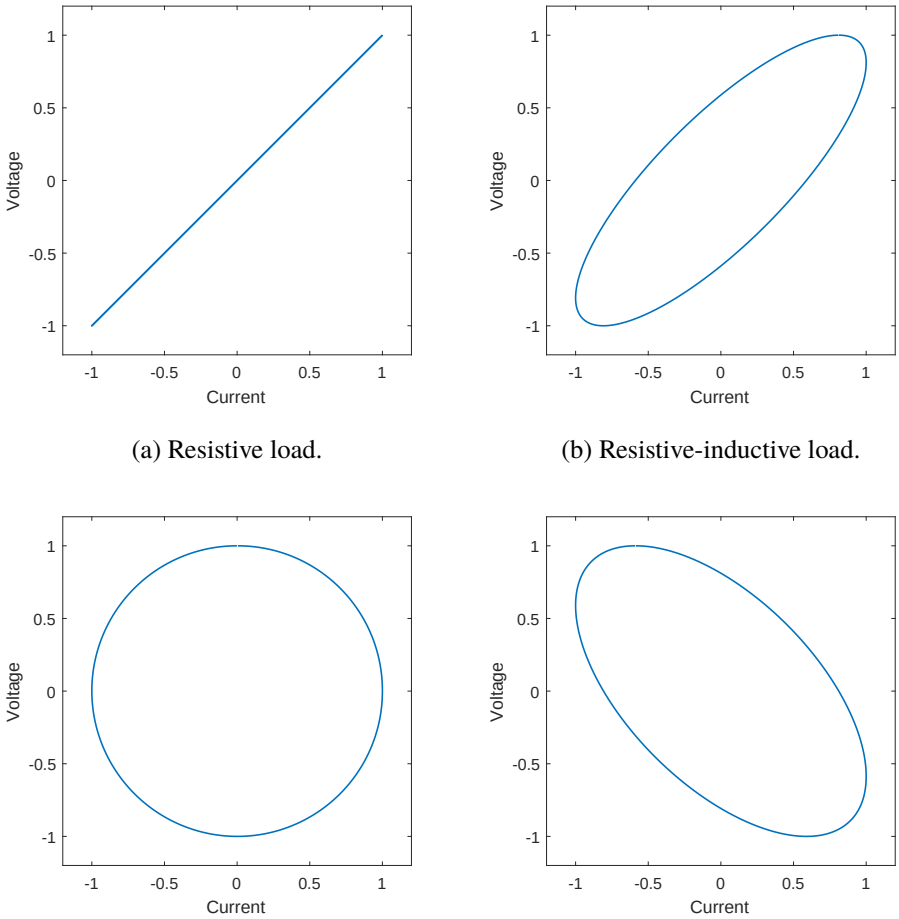
3.1.2 Devices and their working regions

In the following only the completely controlled half-bridge will be analyzed, as it already happened in Chapter 1. This is because many converter topologies can be studied as a collection of half-bridge units, possibly with some non-controlled parts such as diodes.

To clarify the following explanation, some generalization about device operating regions shall be made. Despite output characteristics of different power devices being very similar, nomenclature for their working regions is quite heterogeneous. This originates from the various historical birth of different electronic devices. Despite the possibility to define many working regions, depending on the node in common between input and output sections, from the switching point of view there are only three stationary regions of interest, plus a transient one.

Let us assume that all the devices are n-type, i.e. they rely on electrons as main charge carriers. Also consider that the gate terminal (e.g. in MOSFETs and IGBTs) is analogous to the base lead (in BJTs); likewise the drain terminal corresponds to the collector and the source to the emitter. The stationary regions are *fully-on* (or simply *on*), *fully-off* (also *off* or *blocking*) and *reverse-conducting* (or *free-wheeling*). The transient region here is called *linear* or *current-limiting*.

The on-state region is characterized by the device operating as a closed switch, with limited voltage drop at its ends; the control terminal is usually driven with a positive voltage (or current for BJTs) and the current flows into the collector or drain node. The blocking region is achieved by proper driving of the control terminal, that is biased with a null or negative voltage (or current), preventing it from conducting even if the drain/collector terminal has a positive voltage with respect to the source/emitter. Some devices can also carry *negative* current, i.e. sourcing from the conventional drain/collector terminal. When this happens, the device is in the free-wheeling region. This mode can be controlled by the gate/base terminal or not, depending on the particular device used.



(a) Resistive load.

(b) Resistive-inductive load.

(c) Capacitive load.

(d) Regenerative-inductive load.

Figure 3.2: Lissajous figures for different linear loads; voltage and current are expressed in normalized unit with respect to load peak value.

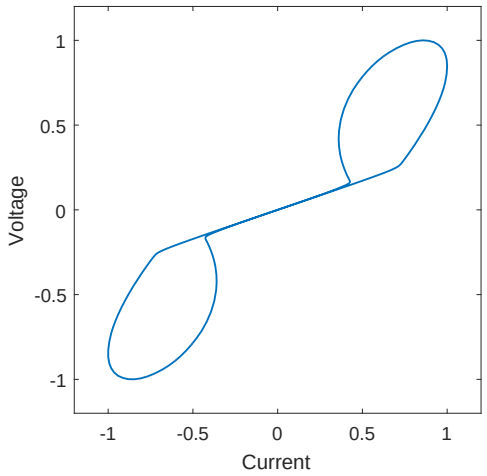


Figure 3.3: Lissajous figure for a non-linear load.

The current-limiting region is considered a transient phase in power devices: here the device carries important current with a large voltage at its ends, thus dissipating a large amount of power. Transit in this region happens when the device is changing from the off-state to the on-state or backwards. Another situation of operation in this region is in case of short-circuit: the device is commanded to turn on fully, but some electric constraint prevents its drain/collector voltage to drop. The name given to this zone recalls the use of the device as an almost-ideal Voltage-Controlled Current Source (VCCS, in gate-controlled devices) or Current-Controlled Current Source (CCCS, in base-controlled devices).

The free-wheeling region is often neglected, since bipolar devices usually cannot conduct negative current, i.e. sourcing from the collector; reverse-conducting IGBT is a notable exception to this rule. FETs instead can carry a negative current if turned-on properly by the gate terminal; however they often have an anti-parallel diode, that can be intrinsic or standalone. In the first case, the diode originates from the particular doping structure used to manufacture the main device, and thus it shares the same die of this one. In the standalone case, the diode is provided externally of the die and

Table 3.2: Analogies between different devices, working regions and terminal names.

Device type →	MOSFET	JFET	IGBT	BJT
Control terminal	gate	gate	gate	base
Reference terminal	source	source	emitter	emitter
Output terminal	drain	drain	collector	collector
Control quantity	voltage	voltage	voltage	current
On-state region	linear[1]	linear[1]	saturation	saturation
Current-limiting region	saturation	saturation	active[2]	active[2]

[1] Also “ohmic” or “triode”.

[2] Also “active forward” or “linear”.

can be inside the same package (as it often happens with IGBTs co-packed with free-wheeling diodes) or even in another device, connected electrically on the main circuit PCB. When a free-wheeling diode is provided, the controlled device can conduct current only if its impedance in the reverse-conducting region is lower than that of the diode. In any case, in a half-bridge circuit, changing the working point of a device from off to reverse-conducting does not provide substantial change of the output node.

Following the descriptions given in [71, 47], the on-state region is called *linear*, *triode* or *ohmic* for FETs and *saturation* for bipolar devices, while the current-limited region is *saturation* for FETs and *linear* or *active* for bipolar parts. Table 3.2 reports the analogies among different power devices, operating regions and terminal names.

3.1.3 A typical working cycle

Deep understanding of losses goes through identification of a typical load and consequent working cycle. In switched mode applications it is common to refer to an inductive load. This load can represent roughly both motor phases and grid impedances; when a more accurate description is sought, it is customary to add generators and resistances, in order to account also for the regenerative part.

Supposing a mainly inductive load that can impose current continuity over an entire PWM cycle, the load can be further simplified in a current source. The steadiness of current over the switching cycle makes obvious that one device will have positive drain current, while the other will see a negative one, if not null. In the following, the first device will be referred to as the *concordant* device of the bridge, while the other will be called the *discordant* one. Concordant and discordant devices will exchange their role upon a change in the sign of the output current of the half-bridge: this can happen, for example, after the zero crossing of a sinusoidal load.

Using the convention of positive currents sourcing from nodes, a positive bridge current will make the high-side device the concordant one, while a negative current will set it as discordant. When speaking about power devices in half-bridge configuration, only the concordant device can determine the change of status of the output node: actions on the gate signal of the discordant device will lead to different results depending on the kind of device used.

For MOSFETs without any external diode, turning off the gate of a discordant device will make the MOS part of the device turn off, forcing the negative current to flow on the inherent (parasitic) diode: the user will see a limited increase in the magnitude of the on-state voltage. When an external free-wheeling diode is used, the behavior is similar, but quantitatively different due to the dissimilar on-state voltage of intrinsic and monolithic diodes. Note that in the second situation the power will flow partly in the diode and partly in the MOSFET, that are not sharing the same die.

For bipolar devices the controlled device will never conduct any current until it becomes concordant. If a free-wheeling diode is provided, as it should always be with inductive loads, it will carry the load current whenever the concordant device is off. If no diode is available, the converter will go in discontinuous mode, producing a deeply distorted output current.

Another important aspect to consider is the behavior of the diode and its effect towards the main power switch. Indeed, every time a pn-junction switches off, there is some charge flowing in the circuit due to the carrier removal from the injected depletion region. The following study is performed relying on the usual modeling of the diode recovery, without any new contribution. Moreover, in circuits that use

SiC-SBD (silicon carbide Schottky-barrier diode), diode recovery is almost null, since no pn-junction is involved, and the recovery phenomenon can be neglected.

3.2 Shichman-Hodges analytical model

One of the first and simplest models used for MOSFETs is the Shichman-Hodges (SH) set of equations [73]. This is usually referred to as "quadratic model", due to the degree of the polynomial describing the drain current. It represents the operation of the MOS transistor in three regions. The meaningful parameters are reported in Table 3.3.

When $V_{gs} < V_T$, then the MOSFET is off and the drain current is null ($I_d = 0$). When $V_{gs} > V_T$, if $V_{ds} < (V_{gs} - V_T)$ the MOSFET is working in linear region and the current is described as:

$$I_d = \frac{k}{2}\left[(V_{gs} - V_T)V_{ds} - V_{ds}^2\right](1 + \lambda V_{ds}) \tag{3.1}$$

Instead, if $V_{ds} > (V_{gs} - V_T)$, the transistor is working in the saturation region (i.e. current-limiting) and the drain current is determined mainly by the gate voltage:

$$I_d = \frac{k}{2}(V_{gs} - V_T)^2(1 + \lambda V_{ds}) \tag{3.2}$$

This model, born before the power MOSFET and hence with signal-level parts in mind, is fairly simple yet accurate if the device satisfies the hypothesis under which it was developed [73]. This can be used also in dynamic conditions if proper capacitances C_{gs}, C_{gd} (gate-source and gate-source, respectively) are considered.

Despite its simplicity, building a loss model around these equations is not trivial: integration of the electrical quantities in closed form to get the total energy is not always possible, but some assumptions and approximations can be done in order to achieve functional results, as it will be shown in the following.

3.2.1 Linear region

A closed form for the on-state voltage of the MOSFET, and hence the conduction loss P_{on}, can be derived from (3.1). The saturation current I_{sat} can be defined as

Table 3.3: Symbols used in the Shichman-Hodges model.

Symbol	Meaning
V_{gs}	gate-source voltage
V_{ds}	drain-source voltage
V_T	threshold voltage
I_d	drain current
k	MOS transconductance
λ	channel-modulation coefficient

the current that marks the boundary between linear and saturation regions, given a specific V_{gs}:

$$I_{sat} = I_{sat}(V_{gs}) = \frac{k}{2}(V_{gs} - V_T)^2 \tag{3.3}$$

Let us drop the channel modulation term $(1 + \lambda V_{ds})$ in (3.1); solving for V_{ds} yields:

$$V_{ds,12} = (V_{gs} - V_T) \pm \sqrt{(V_{gs} - V_T)^2 - 2I_d/k} \tag{3.4}$$

To satisfy the hypothesis of the MOSFET in linear region, the plus sign in (3.4) should be dropped; the resulting drain-source voltage is the on-state voltage $V_{ds,on}$:

$$V_{ds,on} = (V_{gs} - V_T)\left[1 - \sqrt{1 - \frac{2I_d}{k(V_{gs} - V_T)^2}}\right] = (V_{gs} - V_T)\left(1 - \sqrt{1 - \frac{I_d}{I_{sat}}}\right) \tag{3.5}$$

where the drain current coincides with the load one $I_d = I_\ell$.

If the device is turned on and off by a PWM signal with duty cycle d, this will reduce the conduction losses by the same factor, so that they are expressed as:

$$P_{on} = dV_{ds,on}I_\ell = dI_\ell(V_{gs} - V_T)(1 - \sqrt{1 - I_\ell/I_{sat}}) \tag{3.6}$$

This can be rewritten as:

$$\sqrt{1 - \frac{2I_\ell}{k(V_{gs} - V_T)^2}} = 1 - \frac{P_{on}}{dI_\ell(V_{gs} - V_T)} \tag{3.7}$$

Computing the square of both members and reorganizing:

$$\frac{2P_{on}}{dI_\ell} = \frac{kP_{on}^2 + 2d^2I_\ell^3}{kd^2I_\ell^2(V_{gs} - V_T)} \tag{3.8}$$

Ultimately solving for V_{gs} gives:

$$V_{gs} = V_T + \frac{P_{on}}{2dI_\ell} + \frac{dI_\ell^2}{kP_{on}} \tag{3.9}$$

Equation 3.9 is the first important result of SH model applied to loss control: when a certain level of losses is desired with a specific load current, there exists a gate-source voltage that makes the device dissipate this power. Desaturation (i.e. the device goes out of linear region due to a small V_{gs}) limits practically the range of achievable power, since there is a V_{gs} voltage below which the device goes in saturation region. This is called *Miller voltage* (V_M) and it is determined by inversion of (3.2):

$$V_M = V_T + \sqrt{\frac{2I_\ell}{k}} \tag{3.10}$$

The practical limit of on-state losses achievable by action on the gate terminal is thus:

$$P_{on,max} = dI_\ell \cdot V_{ds,on}(V_M) = dI_\ell(V_M - V_T) = dI_\ell\sqrt{2I_\ell/k} \tag{3.11}$$

Equation 3.11 is very important, since it shows that for devices following the SH model, conduction losses are infinitesimal when duty cycle or load current tend to zero.

3.2.2 Switching behavior

Studying the switching transients using the SH model requires integration of the gate voltage equation over time and substitution inside the relevant model law. The gate voltage V_{gs} is moving from the off-state level V_{ggl} to the on-state value V_{ggh}; the gate capacitance C_{gs} is charged through a resistor R_{gh}, and $\tau = R_{gh}C_{gs}$ is the time constant. The general expression of the gate transient starting at $t = t_0$ with voltage

$V_{gs} = V_0$ and ending at $V_{gs} = V_f$ (stationary value) is:

$$\begin{aligned} V_{gs} &= V_0 + (V_f - V_0)\left[1 - \mathrm{e}^{-(t-t_0)/\tau}\right] = \\ &= V_f - \left[(V_f - V_0)\,\mathrm{e}^{t_0/\tau}\right]\mathrm{e}^{-t/\tau} \end{aligned} \tag{3.12}$$

The time t_x needed to go from V_0 to V_x can be computed by inversion of (3.12), giving:

$$t_x = \tau \ln \frac{V_f - V_0}{V_f - V_x} \tag{3.13}$$

The turn-on transient can be divided into three different sections. During the first phase, V_{gs} moves from V_{ggl} to V_T: this happens in the time $t_{d,on}$, the delay-to-on-state. In this phase the output does not change at all, because the gate is below the threshold; the duration is computed by substitution of relevant parameters in (3.13):

$$t_{d,on} = \tau \ln \frac{V_{ggh} - V_{ggl}}{V_{ggh} - V_T} \tag{3.14}$$

After reaching the threshold V_T, V_{gs} keeps rising: the device has a large drain voltage if an inductive load is assumed. This happens because the load forces current continuity, making the complementary device of the bridge conduct; this last clamps the output node voltage and the result is that almost the complete DC voltage (V_{dc}) appears at the terminals of the switching device. This phase terminates when the device enters the linear region; this occurs when V_{gs} hits the Miller voltage V_M. Simultaneously the drain current is increasing, following (3.2); the current rise time t_{cr} is hence:

$$\begin{aligned} t_{cr} &= \tau \ln \frac{V_{ggh} - V_T}{V_{ggh} - V_M} = -\tau \ln \frac{V_{ggh} - V_T - \sqrt{2I_\ell/k}}{V_{ggh} - V_T} = \\ &= -\tau \ln \left[1 - \sqrt{\frac{2I_\ell}{k(V_{ggh} - V_T)^2}}\right] = -\tau \ln \left(1 - \sqrt{I_\ell / I_{sat}}\right) \end{aligned} \tag{3.15}$$

where (3.3) and (3.10) were used. To determine the energy loss for the current rise phase, drain current is computed from the V_{gs} and then multiplied by $V_{ds} \approx V_{dc}$.

Employing (3.2) and shifting the time axis properly in order to simplify equations, SH model determines the current rise energy as:

$$\begin{aligned} E_{cr} &= \int_0^{t_{cr}} \left[V_{dc} \frac{k}{2} (V_{ggh} - V_T)^2 (1 - \mathrm{e}^{-t/\tau})^2 \right] \mathrm{d}t = \\ &= V_{dc} I_{sat} \int_0^{t_{cr}} (1 - \mathrm{e}^{-t/\tau})^2 \, \mathrm{d}t = \\ &= V_{dc} I_{sat} \left[t + 2\tau \, \mathrm{e}^{-t/\tau} - \frac{\tau}{2} \mathrm{e}^{-2t/\tau} \right]_0^{t_{cr}} \end{aligned} \tag{3.16}$$

This equation is not easy to simplify, due to the integration of the squared exponential term. We can compare this result numerically with two linear approximations: one with the Maclaurin formula and the other with linear interpolation between starting and ending points of the transient. For the Maclaurin formula we get the approximation $E_{cr} \approx E_{cr}^m$:

$$\begin{aligned} E_{cr}^m &= \int_0^{t_{cr}} \left[V_{dc} \frac{k}{2} \frac{(V_{ggh} - V_T)^2}{\tau^2} t^2 \right] \mathrm{d}t = \\ &= \frac{V_{dc} I_{sat} t_{cr}^3}{3\tau^2} \end{aligned} \tag{3.17}$$

Using interpolation, the approximation is $E_{cr} \approx E_{cr}^i$, with:

$$\begin{aligned} E_{cr}^i &= \int_0^{t_{cr}} \left[V_{dc} \frac{k}{2} \frac{(V_M - V_T)^2}{t_{cr}^2} t^2 \right] \mathrm{d}t = \\ &= \int_0^{t_{cr}} \left[V_{dc} \frac{k}{2} (V_{ggh} - V_T)^2 \frac{I_\ell}{I_{sat}} \frac{t^2}{t_{cr}^2} \right] \mathrm{d}t = V_{dc} I_{sat} \frac{I_\ell}{I_{sat}} \frac{t_{cr}^3}{3t_{cr}^2} = \\ &= \frac{V_{dc} I_\ell t_{cr}}{3} \end{aligned} \tag{3.18}$$

Plotting E_{cr}^m / E_{cr} and E_{cr}^i / E_{cr}, using $x = I_\ell / I_{sat}$ as parameter, it is possible to understand which formula is more accurate and the amount of error with respect to the particular device used, characterized by its x value. This graphical comparison is depicted in Figure 3.4.

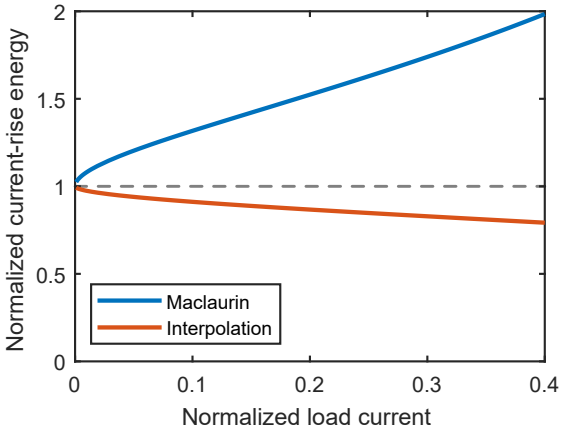


Figure 3.4: Comparison of current rise energy loss relative values using various approximations. Maclaurin approximation is in blue, while the linear interpolation is given in red; the dashed line denotes the non-linear exact relationship described in (3.16).

The linear interpolation approximation seems to be quite accurate, especially for low levels of x, i.e. when the device gain is very high and a large overdrive is used. Substituting with the expression of t_{cr} previously computed, we get:

$$E_{cr} \approx \frac{R_{gh} C_{gs} V_{dc} I_\ell}{3} \ln \frac{V_{ggh} - V_T}{V_{ggh} - V_M} \tag{3.19}$$

Equation 3.19 shows that the gate resistance strongly affects the current rise losses, while the dependence on the gate voltage is weak; in any case, low load currents make this energy loss negligible.

When V_{gs} reaches V_M, the device carries the whole I_ℓ current and this allows the complementary bridge device to turn off; the MOSFET then moves from saturation to linear region, discharging the gate-drain capacitance C_{gd}. During this transient, the gate voltage is almost constant and equal to V_M, so the gate current is assumed to be dependent on C_{gd} only: the contribution of C_{gs} is neglected.

In first approximation, the V_{ds} voltage transient is considered linear, characterized

by the constant current charge of the C_{gd} capacitance:

$$C_{gd}\frac{\Delta V_{gd}}{t_{vf}} = C_{gd}\frac{0-(V_M - V_{dc})}{t_{vf}} \approx C_{gd}\frac{V_{dc}}{t_{vf}} = \frac{V_{ggh} - V_M}{R_{gh}} \tag{3.20}$$

So the voltage fall time t_{vf} can be computed as:

$$t_{vf} = \frac{R_{gh}C_{gd}V_{dc}}{V_{ggh} - V_M} \tag{3.21}$$

By straightforward integration, it is possible to obtain the energy loss during the voltage fall phase:

$$\begin{aligned} E_{vf} &= \int_0^{t_{vf}} I_\ell V_{dc}\left(1 - \frac{t}{t_{vf}}\right)\mathrm{d}t = V_{dc}I_\ell\frac{t_{vf}}{2} \\ &= \frac{R_{gh}C_{gd}V_{dc}^2 I_\ell}{2(V_{ggh} - V_M)} \end{aligned} \tag{3.22}$$

This equation clarifies that beyond a linear relationship with the gate resistance, a dependence of voltage fall energy on gate voltage exists, too. This leads to the important result that, as far the SH model is applicable, switching losses depend also on the gate voltage, and not only on the gate resistance.

The switching phases towards the off-state are qualitatively symmetric to those presented before, but quantitatively different. The gate driver forces the voltage V_{ggl} and discharges the gate capacitance through a resistor of value R_{gl}, possibly different from R_{gh}.

The delay time to turn-off $t_{d,off}$ may be longer than the turn-on one, since the voltage span from V_{ggh} to V_M can be larger than the one from V_{ggl} to V_T. Applying (3.13) we obtain:

$$t_{d,off} = \tau \ln\frac{V_{ggh} - V_{ggl}}{V_M - V_{ggl}} \tag{3.23}$$

where $\tau = R_{gl}C_{gs}$.

During the voltage rise phase, the gate voltage is clamped at V_M and the C_{gd} capacitance is charged at V_{dc}; the time needed to complete this phase is:

$$t_{vr} = \frac{R_{gl}C_{gd}V_{dc}}{V_M - V_{ggl}} \tag{3.24}$$

This results in a voltage-rise energy loss that amounts to:

$$E_{vr} = \frac{V_{dc} I_\ell t_{vr}}{2} = \frac{R_{gl} C_{gd} V_{dc}^2 I_\ell}{2(V_M - V_{ggl})} \tag{3.25}$$

Considerations analogous to those used to obtain (3.19) lead to the SH approximate expression for current fall losses:

$$E_{cf} \approx \frac{R_{gl} C_{gs} V_{dc} I_\ell}{3} \ln \frac{V_M - V_{ggl}}{V_M - V_{ggl}} \tag{3.26}$$

Equations 3.19, 3.22, 3.25 and 3.26 can be summed together to get the total energy loss per switching cycle, and multiplying the results for the PWM frequency (f_c) makes possible to estimate the average switching loss:

$$P_{sw} = f_c(E_{cr} + E_{vf} + E_{vr} + E_{cf}) \tag{3.27}$$

This model, despite being quite simple, allows to make some assumptions on the loss trend with respect to different parameters. The main limitation lays in the lack of an explicit dependence on temperature, which can be accounted for only indirectly, changing the values of the parameters.

3.3 Empirical models

Section 3.2 has demonstrated how difficult it can be to produce a loss model starting from basic device equations, even in their simplest form. Beyond the implicit difficulty in gathering losses from electrical quantities and waveform shapes, some effort is needed to determine relevant parameters and to account for minor deviations of the model from the real device.

One possible solution to completely overcome this problem is in the development of empirical or semi-empirical models. By definition, these rely on the data coming from experience, and thus they do not suppose any specific knowledge about device physics nor electrical models. These models can be developed starting from directly measured data, or from "second-hand" information, retrieved from SPICE models (usually fitted on experimental curves by the manufacturer) or directly from the

datasheet. Different approaches have both pros and cons, and will be discussed in the following.

3.3.1 SPICE-fitted or experimental-fitted model

The availability of a sufficiently detailed SPICE model for the device in use is a necessary prerequisite to develop this model. When the SPICE model fits properly the real behavior of the device, this model can be very accurate, since it can determine losses on almost every vector of input parameters, regardless of their number.

To obtain loss data from SPICE parameters, some simulation benches need to be prepared, to explore the behavior of the device in different regions. One circuit is used to study conduction losses, while another one can give switching energies directly, taking advantage of numerical integration feature of many SPICE systems; example for the LTspice application are reported in Figure A.1 in Appendix A.

Once the circuits are available, many parametric simulations must be carried out to explore the loss behavior in dependence of all relevant parameters. In this case, the SH loss model presented in Section 3.2 gives some precious information on which quantities need to be swept with respect to each investigated loss contribution. Recalling (3.6), on-state losses depend on the commutated DC link voltage, load current, gate voltage and junction temperature:

$$P_{on} = f\left(V_{dc}, I_{\ell}, V_{ggh}, T_j\right) \tag{3.28}$$

The simulations to get this data are of the DC type, and the numerosity of runs is given by the product of the steps of each parameter: for example, five parameter values for each quantity give $5^4 = 625$ total simulations. After gathering the SPICE points, the result can be generalized outside the simulated values by some form of fitting. Given the results of the SH-based loss model, polynomial interpolation can be a proper candidate to achieve the purpose.

Some more hints on the fitting function can be given by the study of other device models, to find a specific model to which correlate the data, when polynomials are not accurate enough.

For switching losses the problem is even more difficult, since more parameters affect the result. In fact the collection of (3.19), (3.22), (3.25), (3.26) and (3.27) shows that the model is:

$$P_{sw} = g\left(V_{dc}, I_{\ell}, V_{ggh}, V_{ggl}, R_{gh}, R_{gl}, f_c, T_j\right) \tag{3.29}$$

Comparing this equation with (3.28), it is clear that there is a higher number of parameters involved; moreover, the energy data is determined by a transient simulation, rather than a DC, making simulations last longer at constant number of runs.

This model for losses, yet requiring many simulation time and post-processing, is believed to be highly accurate if the underlying device model is. Moreover, accuracy can be improved by increasing the number of steps, by choosing a proper fitting function or reducing the number of parameters when a dependence can be clearly stated. For example, in (3.29), the PWM frequency f_c is usually not simulated, since it is known that it acts as a multiplying factor in front of the sum of energies, as stated in (3.27).

Moreover, it is difficult to adapt a model obtained in this way to another, even similar device, as well as applying the same interpolation functions to different devices: too many variables can make one part different from the others, so further generalization cannot be done.

What is done in the SPICE domain can be accomplished also in the real world: simulation runs are substituted by experimental measures, data is collected, then fitted to some mathematical function and a model is obtained. In this case the task can be even longer, since time is needed to collect a sufficient number of measures. The payoff is the greater accuracy of the model, given a number of data points.

Models developed through this procedure, not relying on a particular device model, are suitable for different device types and materials, even when the underlying physics is not completely known or mathematically manageable.

3.3.2 Datasheet-driven models

Developing a SPICE- or experimental-fitted model can be a time-consuming activity, and demanding from the prerequisite point of view: in the first case, an accurate SPICE

model should be provided by the device manufacturer, in the latter, an accurate test bench is needed. The device datasheet embeds many useful and experimental data points about the device, presenting the drawback of poor cross-correlation of different parameters: curves often represent single operating points or dependence between two or three parameters only.

One first possibility is to use simple models, such as the SH set of equations, and to infer the parameters using the datasheet information: when a device is not described correctly by such a model, different sets of parameters for each working region can be computed. For example, referring to the aforementioned SH model, both (3.6) and (3.26) depend on parameters k and V_T.

Another possibility is to project the datasheet parameters outside the conditions under which they are specified, using some heuristic from literature or interpolated data (when provided by the manufacturer) [74].

For example, the on-state resistance R_{DS0}, connected to the on-state voltage, is usually given at a specific load current $I_{D,Rds}$ and gate voltage $V_{GGH,Rds}$. This is just a point, but the information about losses needs to be available under different conditions. Equation (3.6) shows that the power loss depends on the square root of the current. The Taylor approximation of this function allows to determine roughly the desaturation current limit corresponding to the $V_{GGH,Rds}$ voltage:

$$I_{D,max} = \frac{V_{GGH,Rds} - V_T}{\alpha R_{DS0}} \tag{3.30}$$

Analytical study shows that it should be $\alpha = 2$, but some investigation suggests that $\alpha = 1.5$ yields better values. Even if the function should be shaped as a square root, it can be approximated using a second-order polynomial f in drain current. The polynomial coefficients can be determined forcing the curve to hit the points $(0; 0)$, $(I_{D,Rds}; R_{DS0} \cdot I_{D,Rds})$, $(I_{D,max}; V_{GGH,Rds} - V_T)$, where $I_{D,sat} = (V_{GGH} - V_T)/(\alpha R_{DS0})$, in analogy with (3.30). To obtain the conduction power loss, V_{DS} needs to be scaled appropriately: this can be accomplished using an affine transformation applied to the curve obtained from the datasheet parameters; the result is then multiplied by the load current and

reduced by the duty-cycle:

$$P_{on} = dI_{load}\frac{V_{GGH} - V_T}{V_{GGH,Rds} - V_T} \cdot f\left(I_{load}\frac{I_{D,max}}{I_{D,sat}}\right) \tag{3.31}$$

Switching energy losses are supposed to depend linearly on drain voltage, drain current and gate resistance. For example the turn-on energy can be expressed as:

$$E_{on} = E_{on0}\frac{V_{bus}}{V_{DS,Eon}}\frac{I_{load}}{I_{D,Eon}}\left(\frac{R_{GH}}{R_{G,Eon}}\right)^{\beta} \tag{3.32}$$

where E_{on0} is the measure coming from the manufacturer, done at values $V_{DS,Eon}$, $I_{D,Eon}$ and $R_{G,Eon}$. Simulations show that $\beta = 1/3$ makes resulting values fit best with the manufacturer-provided curves. The turn-off energy can be expressed similarly.

This model, even if neglecting the effects of gate voltage on switching losses and without giving any insight on switching times and mechanisms, allows to use readily available data, coming from the device manufacturer information sheets.

3.3.3 Temperature dependence

Temperature can influence deeply the device performance and this is exposed by an explicit dependence of model parameters on temperature itself. Both case and junction temperatures are meaningful, but the latter should be chosen when the electrical behavior is concerned. This dependence can be advantageous when it is known: in this case the observed model quantity becomes a Temperature-Sensitive Electrical Parameter (TSEP) and it can be used to indirectly measure the device junction temperature, that would be otherwise very difficult to obtain.

There are several ways to account for temperature dependence into electrical models. Junction temperature can be explicitly added as an independent variable to the model, or it can be managed as a variable that changes some parameter values. Also the sensitivity of the particular observed quantity to temperature should be explored, since in some cases, or for some operating ranges, this dependence can be neglected. This can be particularly effective in WBG device, that are usually less susceptible to junction temperature change.

Moreover, the focus of this work is on loss models for ATC. After a first attempt to retain the T_j dependence in all models, a simple idea relaxed this requirement. The objective of ATC is to control temperature, so the concern is mainly devoted to the steady state of this quantity. If a model is tuned on the steady-state temperature (if not fixed, at least with limited variance) rather than the actual value, the control should be able to drive the system towards the set-point, even in case of inaccurate models, at least for the temperature dependence. Some experimental results that will be presented in Chapter 4 show that this assumption can work, even for transients from ambient temperature up to device limit. This is the reason why, in the following, no explicit temperature dependence is considered further; nonetheless the author believes that deeper insight into this should be pursued.

3.4 Shoot-through loss modeling

So far the attention has been focused on natural losses, occurring in each switching circuit due to the common, high-efficiency driving circuits that are usually employed in power converters. It was shown that following some model, it is possible to change the loss value acting on some system parameters.

It is very important to observe that at least another remarkable category of power losses exists, when power devices are arranged in half-bridge configuration. These are losses originating from the shoot-through (ST) of the DC source of the bridge: when the high- and the low-side command signals are not driven in correct complementary mode, some overlap of the two conduction phases can happen, leading to a partial short-circuit of the source. This condition is usually undesirable and avoided in converters, since it can lead to EMI, device wear, efficiency drop and possibly overheating of the switches.

From a strictly electrical point of view, devices in this condition transit the areas that are usually followed during the switching phase. Since the gate is possibly at an intermediate value between the rails, the bridge output voltage changes and high current flows through the device while it sustains a high voltage. When ST happens accidentally, it is located near the switching instants; but it can happen or it can be

forced in every moment, supposed that no interlock between high- and low-side is enacted by the gate driver.

A simple model for ST losses can be built if the hypothesis that the bridge voltage is invariant during the phenomenon holds. In this case only the shoot-through current (very similar to a *short-circuit* current) needs to be modeled. The product of the current by the DC voltage, integrated in time, yields the energy associated with the ST event.

If the ST is long enough, but the gate voltage is lower than the nominal one, the current is constant during the event, so a linear relationship between energy loss (or power loss, if thinking about the time average) and ST exists. This relationship is not linear for very short pulses, narrower than the device bandwidth. These aspects are detailed in the following.

3.4.1 Direct model

The development of a ST loss model needs some hypothesis about the driving circuit of the device; in particular, along the "high" gate level V_{ggh} and the "low" value V_{ggl}, a third voltage V_{gst} is supposed to exist. This is the gate voltage that appears on one of the devices of the half-bridge during the ST event, while the other is supposed to be fully driven. Moreover, the V_{gst} level is assumed to be constant for the whole ST event.

The conditions stated above result into the inequality $V_{ggh} > V_{gst} > V_{ggl}$. Assuming for example that the high-side device is fully on, i.e. $V_{gs,H} = V_{ggh}$, then $V_{gs,L} = V_{gst}$. Supposing negligible the mismatch between the devices of the leg, the output node voltage V_o will satisfy the relationship:

$$V_{dc} > V_o > V_{dc}/2 \tag{3.33}$$

This happens because the effective conductance of the two devices is modulated by their gate voltage. If V_{gst} is low enough to hold the device in the current-limiting region, the output voltage will be set by the companion part, that is fully on; in the example above, $V_o \approx V_{dc}$.

Calling I_{st} the shoot-through current, i.e. the current that flows *along* the leg, and t_{st} the duration of the ST event, supposing the switch bandwidth negligible, the ST energies for both switches are:

$$E_{st,H} = (V_{dc} - V_o) I_{st} t_{st} \tag{3.34a}$$

$$E_{st,L} = V_o I_{st} t_{st} \tag{3.34b}$$

These add to the natural losses of the devices: this is the reason why only the I_{st} current is considered and not the whole I_d. Equations 3.34 shows that the energy on each device can be made very different depending on the voltage value of the output node, i.e. controlling in which moment of the PWM period the intermediate gate voltage is applied. Recalling the fact that in the example the ST is initiated by the low-side device, (3.33) holds and this component will sustain most of the ST losses.

3.4.2 Non-linear effects representation

The change in the drain current of the device is not instantaneous with the gate voltage. In particular, we can assume that the transient is described by a first-order exponential equation. This is not theoretically true, since the gate transient has usually exponential profile, and the current in the limiting region depends on the square of the overdrive; anyway, the result can be more accurate than assuming an ideal square current pulse (as it was done in 3.34). Let the shoot-through current have the form:

$$I_{st}(t) = \begin{cases} I_{st0}(1 - \mathrm{e}^{-t/\tau}), & 0 < t < t_{st} \\ 0, & t > t_{st} \end{cases} \tag{3.35}$$

The delay due to the limited bandwidth is considered only during the rise transient, despite being present also at the end of the pulse, falling. This is due to the different magnitude of the area that needs to be ignored, as shown in Figure 3.5. This simple assumption allows to keep the equations readable without affecting the overall quantitative result.

We can now determine the energy using this improved formula. Looking at the low-side device, and supposing $V_o \approx V_{dc}$ since the high-side device is fully on, we

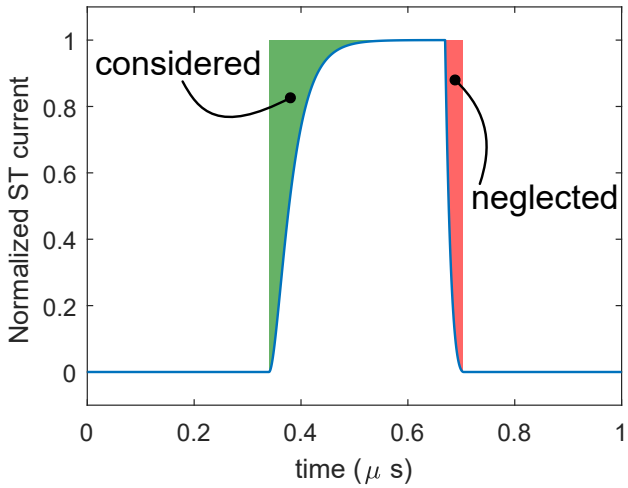


Figure 3.5: Current components considered and neglected for the non-linear modeling of shoot-through energy loss.

have:

$$\begin{aligned} E_{st,L} &= \int_0^{t_{st}} V_{dc} I_{st}(t)\,\mathrm{d}t = V_{dc} I_{st0} \int_0^{t_{st}} (1 - \mathrm{e}^{-t/\tau})\,\mathrm{d}t = \\ &= V_{dc} I_{st0} \left[t + \tau\,\mathrm{e}^{-t/\tau} \right]_0^{t_{st}} = V_{dc} I_{st0} \left(t_{st} + \tau\,\mathrm{e}^{-t_{st}/\tau} - \tau \right) \\ &= V_{dc} I_{st0} t_{st} \left[1 - \frac{\tau}{t_{st}} (1 - \mathrm{e}^{-t_{st}/\tau}) \right] \end{aligned} \tag{3.36}$$

Comparing this result with (3.34b), the term in brackets acts as a correction coefficient, which magnitude depends on the ratio $x = t_{st}/\tau$, i.e. the shoot-through time normalized to the time constant of the drain current in the limiting region. This time constant is defined empirically: it descends from the exponential transient of the gate voltage that, through the device model, determines the current. Since the law relating gate voltage to drain current is not linear, the current transient is not exactly exponential. Nonetheless, it can be approximated by a single time constant exponential: this is where the definition of τ emerges.

It is possible to give another simplification of (3.36) when $t_{st} > 4\tau$. In this case,

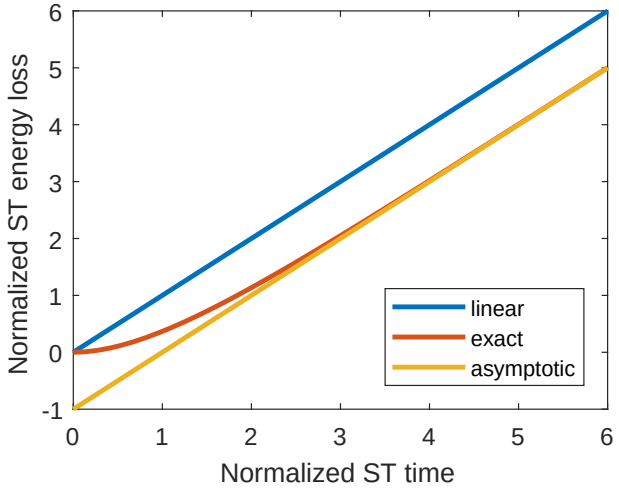


Figure 3.6: Comparison of different approximations for the non-linear computation of shoot-through energy loss.

the exponential term is negligible and we get a simple formula that yet is more accurate than (3.34b), despite being valid only for $t_{st} > \tau$:

$$E_{st,L} = V_{dc} I_{st0} t_{st} \left(1 - \frac{\tau}{t_{st}}\right) \tag{3.37}$$

Figure 3.6 compares the three different expressions for the shoot-through energy, as a function of x defined above. The simplified formula (3.34b) gives a static error that is negligible only for $t_{st} \gg \tau$.

3.4.3 Inverse model

From the previous section, the shoot-through power loss can be computed, supposing the additive loss negligible for the device that is fully on. Looking at the device which is held in current-limiting region, using the same symbols as before:

$$P_{st} = E_{st} f_c = V_{dc} I_{st0} f_c \tau \left(x - 1 + \mathrm{e}^{-x}\right) \tag{3.38}$$

This equation is very important since it directly and accurately correlates electrical (V_{dc}, I_{st0}, f_c, τ) and user-controllable parameters (x) to the shoot-through loss P_{st}. If one wants to choose the proper x to achieve the desired P_{st} (as it will be highlighted in the next chapter), (3.38) should be inverted. The problem is that the closed form is not easy to manipulate, since a transcendental equation arises:

$$x - a - 1 + \mathrm{e}^{-x} = 0 \tag{3.39}$$

with $a = P_{st}/(V_{dc} I_{st0} f_c \tau)$. This can be solved numerically or graphically. In the first case the solution is trivial, while in the latter some notes can be made.

Firstly, the equation can be set into fixed-point notation, i.e. in the $x = f(x)$ form:

$$x = a + 1 - \mathrm{e}^{-x} \tag{3.40}$$

Since $a > 0$, the equation can always be solved and it has exactly one solution. To be sure to converge, the starting point can be chosen below the point x_s, where the curve is parallel to the bisector. The concavity of the function ensures convergence of the iterative computation; this can be proven also using the Banach fixed-point theorem [75]. The iteration step is:

$$x_{i+1} = a + 1 - \mathrm{e}^{-x_i} \tag{3.41}$$

as it is shown by the path traced with arrows in Figure 3.7, reporting an example of graphical-iterative computation of the solution.

It is interesting to note that for this special case, a closed-form solution can be found in terms of the Lambert W function. This family of functions is defined to satisfy the following:

$$W(x\,\mathrm{e}^{x}) = x \tag{3.42}$$

This results in a family of functions since $f(x) = x\,\mathrm{e}^{x}$ is not invertible on its whole

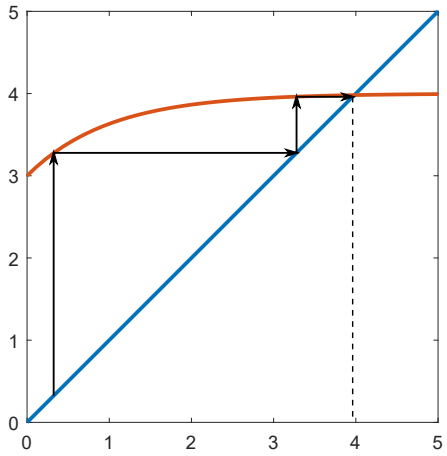


Figure 3.7: Example of graphical solution for the inversion of the shoot-through loss model.

domain. Starting from (3.39), some steps are needed:

$$\begin{aligned}
x - a - 1 &= -\mathrm{e}^{-x} \\
(x - a - 1)\,\mathrm{e}^{a+1} &= -\mathrm{e}^{-x}\,\mathrm{e}^{a+1} \\
(x - a - 1)\,\mathrm{e}^{x-a-1} &= -\mathrm{e}^{-a-1}, \qquad (y = x - a - 1) \\
y\,\mathrm{e}^{y} &= -\mathrm{e}^{-a-1} \\
W(y\,\mathrm{e}^{y}) &= W(-\mathrm{e}^{-a-1}) \\
y &= W(-\mathrm{e}^{-a-1}) \\
x &= a + 1 + W(-\mathrm{e}^{-a-1})
\end{aligned} \tag{3.43}$$

Figure 3.8 compares the resulting normalized shoot-through time $x = t_{st}/\tau$ when using this method, together with the inversion of (3.34b): $x = a$. It is clear that if a is large, no difference between the two is noticeable, while it becomes important for $a < 3$.

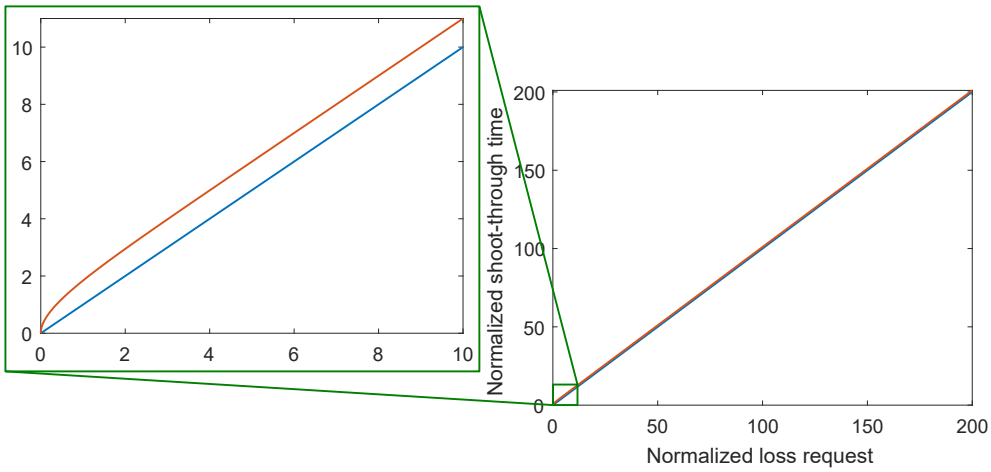


Figure 3.8: Inversion of the exact (red) and approximate (blue) model of shoot-through losses. On the horizontal axis the normalized loss request a is represented, while on the vertical axis the normalized shoot-through time x is reported.

Chapter 4

Active Thermal Control

La vera scelta non è mai tra il fare una cosa e il non farla.
Ma tra il farla o non farla per coraggio oppure per paura.

– M. Gramellini, 2010

In the introduction Active Thermal Control (ATC) was presented as a possible technique capable of improving performance of traditional electronic switches, as well as getting better results from modern wide band-gap devices. ATC is a locution that encompasses different aspects and methodologies that share the common denominator of controlling the temperature of electronics components. In this work, ATC is studied concerning only its applications in power electronics, and only one of its different categories will be analyzed thoroughly.

The main target of ATC is to improve device performance from the reliability point of view. Many degradation mechanisms in power devices are induced by thermal stress, particularly thermal cycling [76]. Being complex structures, power switches are made of different materials, each one with peculiar properties. It is common for these materials to have different Coefficients of Thermal Expansion (CTE); this means that when thermal cycles occur, each part extends differently from the others. Ultimately, this results in mechanical fatigue on the parts, that can lead to failure. Also average temperature can have important effects, since it can accelerate many chemical

degradation processes.

ATC can be implemented using various control schemes: with feedback, in feed-forward or indirect. The first kind requires knowledge about the device temperature, but the case one is hardly meaningful (being influenced heavily by what is outside the device itself), while the junction temperature is difficult to measure, both directly and indirectly. Predictive and feed-forward schemes rely massively on accurate models, that are infrequently available to the system developer, and are often bound to knowledge of many parameters. Indirect controls can vary depending on the particular observed quantity; it will be demonstrated that controlling device power loss is a powerful method to achieve good ATC performance.

In this chapter different ATC schemes are classified as from literature, then the technology developed during the research program is presented, highlighting the choices that brought to the idea. Simulations and experimental results are presented for three different ATC methods, and a discussion about the achievable benefits and the necessary drawbacks is drawn. The results presented here assume the device arranged in the same half-bridge analyzed so far. The power loss diagram over time will be used repeatedly: in this case the quantities of the bridge assumed are those represented in Figure 4.1, i.e. cosinusoidal current and voltage (average). Since the studied device is always the low-side one, the bridge quantities have opposite sign to the device ones. Table 4.1 reports the parameters of the experimental test bench set up.

4.1 ATC classification

In [77] a convenient classification of ATC techniques is proposed. It distinguishes among four different levels, numbered low to high starting as far away from the device as possible. Category 1 ATC happens at system level, so the temperature of a generic part or the whole system, rather than a device, is controlled by means of system-wide policies, such as performance reduction, current derating or similar. Type 2 ATC operates at power controller level, thus the thermal management occurs by changing operating points of different system components, but without significant loss of functionality as perceived from the user. When the ATC is implemented by

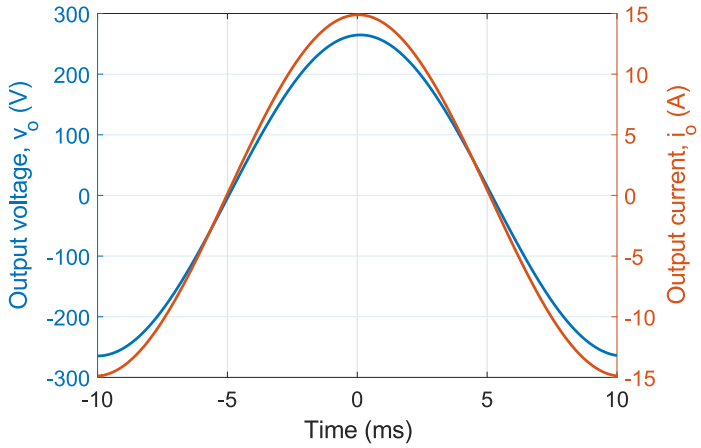


Figure 4.1: Half-bridge output waveforms used to generate the power loss diagrams of the ATC techniques analyzed.

Table 4.1: System parameters (simulation and experiment).

Parameter	Symbol	Value	Unit
DC bus voltage	V_{dc}	600	V
DC link capacitance	C_{dc}	235	μF
Output coltage (peak)	$V_{o,pk}$	270	V
Output current (peak)	$I_{o,pk}$	15	A
Output active power	P_{out}	2	kW
Load resistance	R_{load}	17	Ω
Load inductance	L_{load}	1	mH
Load frequency	f_{out}	50	Hz
PWM frequency	f_{pwm}	10	kHz

modifying the modulation pattern of the controller, level 3 ATC is obtained. Lastly, level 4 ATC is achieved by direct action on the power electronic switch; in this case an AGD is often used and the term "Active Gate Control" indicates that the result is obtained with the highest granularity, occurring at device level.

The level of the ATC used determines not only the applicability range and the possible techniques, but also its granularity, i.e. which is the dimension of the smallest part that can be controlled. The lower the level, the larger the part. For example, in level 1 the whole system temperature is controlled, in level 2, each subsystem composing the main one is controlled, in level 3 control is on the modulation unit (it can be a power bridge or part of it) and ultimately, in level 4, every single device can be controlled independently.

These considerations seem to hint at the highest level as a better candidate for general implementations, since the power device is the smallest unit; moreover, the resulting control is inherently distributed and being far from the user is expected to have the least impact on the perceived performance. These are the reasons why this work will address device level ATC.

4.1.1 Limitations in controlling a system with delay

Thermal systems usually present some peculiar characteristics when it comes to control. Firstly, the manipulated variable is usually a heat source, that is inherently asymmetric, unless a cooling unit is used. It is thus possible to increase the temperature fast, but the heat removal is usually slower, relying on the built-in cooling system only, designed to limit the maximum temperature rather than continuously operating on the thermal status of the system.

Moreover, the temperature dynamics is usually conditioned by important thermal capacitances, especially in case of bulky systems: this results in large time constants and considerable delays between the system excitation and the response. Controlling systems with important delays achieving large bandwidth is not an easy task, since it poses limits on the stability of the feedback loop.

The study of systems with delay has attracted the attention of many control engineers since the Fifties, and a vast reference is available in literature [78, 79, 80,

81, 82, 83], so the coverage of this topic is demanded to these works.

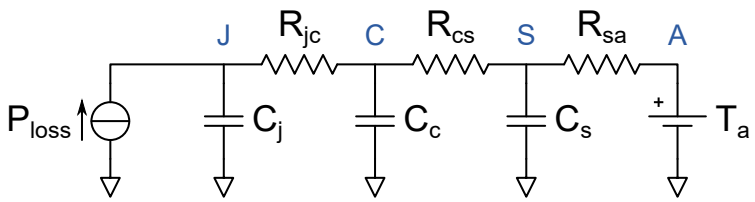
4.1.2 Thermal bandwidth

It is common practice to analyze and study thermal systems using an electric analogy, especially when conduction is the main heat transfer method. Starting from Fourier's law describing the heat exchange in solids, some results can be obtained: a linear relationship between the temperature difference of two points and the heat flow (power) exists. This results in an electric model where the temperature is represented by a voltage, the heat flow by a current and their proportionality is described by a (thermal) resistance. Similar results can be achieved, under some approximation, for the transient state: in this case the impossibility of immediate temperature change is described by a thermal capacitance.

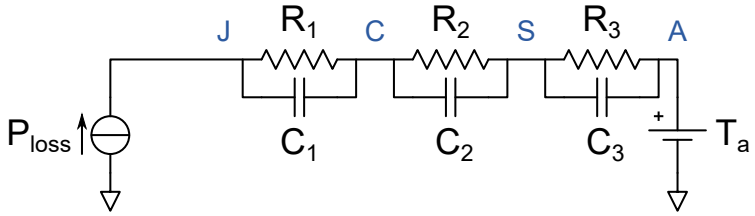
The system constituted by the power device with its internal parts and the sink can be decomposed into several items. Using the thermal-electric analogy, these can be described by cascaded networks of resistances and capacitances. Two models exist: Cauer networks and Foster networks; they are depicted in Figure 4.2.

Cauer networks, represented in Figure 4.2a, are characterized by an L-shaped arrangement of the sections: the upper branch is made by a resistance, with a capacitance connected between the output node and the reference one. These networks are useful because each component can be linked to physical parts of the thermal system. Foster networks are instead formed by sections with resistance and capacitance in parallel (see Figure 4.2b). A complex system results thus in a series of thermal impedances: the relationship between each impedance and the physical part is lost, but the resulting circuit equations are simplified and fitting operations can be performed more easily. Nonetheless, under the hypothesis of linearity, the two representations are equivalent, i.e. they can describe effectively the same system; nonetheless their parameters need to be changed during the transformation.

Once a complex RC thermal network is defined for a particular system, transfer functions for different quantities can be computed. This allows to draw a Bode diagram, thus representing the system response in the frequency domain. This helps in studying the thermal inertia between the power loading of the die and its temperature rise,



(a) Cauer network.



(b) Foster network.

Figure 4.2: Two different models of thermal RC networks that can represent the thermal system from device junction (J) to ambient (A), passing through case (C) and heatsink (S).

together with heat propagation towards the device case and sink.

Figure 4.3a reports a thermal Bode diagram between device power loss and junction temperature. This diagram can be constructed from a manufacturer-provided thermal network, or graphically from the thermal impedance as a function of pulse width. In fact, if this last graphic is provided in logarithmic scale, a reversal of the horizontal axis will provide the desired result; this can be appreciated comparing the red curve in Figure 4.3b with 4.3a, reversing the horizontal axis for one of the two.

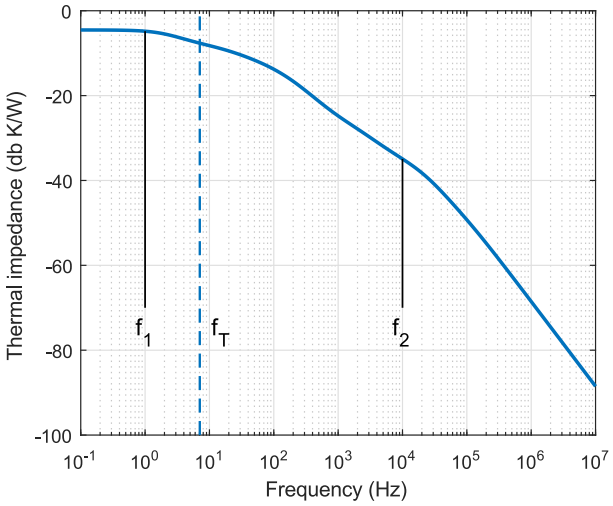
The most important result of the linear approximation of heat transfer is that the temperature measured across two different points is related to the harmonic content of the power waveform that causes the heating of the assembly. In this case, the Bode diagram helps in finding a cut-off frequency above which the change in temperature is widely reduced compared with the DC one. Below this frequency, power and temperature are directly connected. This means that indirect thermal control can be achieved by direct loss control, greatly simplifying the topologies and relaxing the constraints of temperature measurement.

4.1.3 Power control

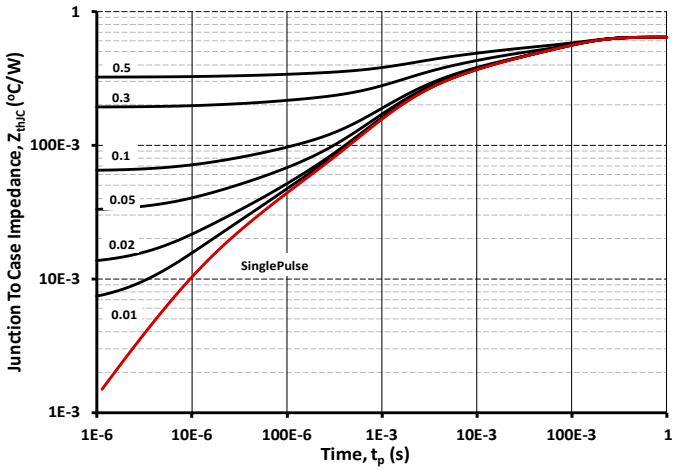
As already stated, direct temperature control, although possible, is made difficult by the intrinsic difficulties in junction temperature measurement and in the delay of the temperature change as measured from the case. The low-pass characteristic of the thermal network suggests to control temperature *indirectly*, working on the power losses. This strategy is applied effectively in [84], using an AGD that can generate a stepped gate voltage pattern. In this case, adjusting the duration and height of the intermediate step, it is possible to control both switching and conduction losses, thus achieving ATC indirectly, through the power loss.

If the cooling system characteristics do not change over time, the temperature is directly determined by losses in the DC case, and residual power ripple passes unaltered if in-band, or attenuated if out-of-band. This suggests to aim at constant power losses, independently of the electric load of the system, to achieve constant temperature of the device.

This approach is supposed to be greatly conservative, since the thermal bandwidth



(a) Thermal Bode diagram.



(b) Transient thermal response for a commercial SiC MOSFET.

Figure 4.3: Graphs representing the thermal behavior of the same SiC MOSFET in the frequency and time domain.

of common systems is usually in the order of several hertz, and in this case the control acts almost in DC. Moreover, when reliability issues are concerned, most of the degrading phenomena occur below several hertz, so reliability-oriented ATC can be neglected above this threshold.

4.1.4 Control architectures

Direct ATC can be implemented using traditional closed-loop techniques. This means that a relevant quantity (junction or case temperature) should be measured and compared to a proper reference value. A linear controller can be used, provided that the limited bandwidth of the plant is properly considered when case temperature is concerned. The block schematic of this control architecture is represented in Figure 4.4, where the red color of the inverse loss model denotes possible difficulties in the inversion.

Working on junction temperature allows a faster control, but much more effort is needed for the measurement. Junction temperature can be observed directly using thermal cameras and thermo fibers, or indirectly using observers or Temperature Sensitive Electric Parameters (TSEPs). The direct modes are expensive and difficult to implement in a practical environment, while the others need a deep knowledge of the system or some training method and commissioning phases on field.

Once a detailed model of the thermal system is known, the sensed temperature feedback can be omitted. If the model can be inverted, a pure feed-forward model can be realized, that determines directly the desired manipulated variables to achieve the desired temperature set-point. This control scheme is depicted in Figure 4.5: the inverse thermal model can be omitted if *indirect* ATC is implemented, since in this case the control happens directly on the temperature.

If the model cannot be readily inverted but a finite set of states can be actuated for each control cycle (as a Finite State AGD, FS AGD, does), a Model Predictive Control (MPC) strategy can be applied. This configuration is reported in Figure 4.6, where the *direct* loss model is used. The generation of the set of states and resulting outputs is needed to explore all configurations using an MPC algorithm.

Beside these implementations, it is also possible to integrate some measurement in

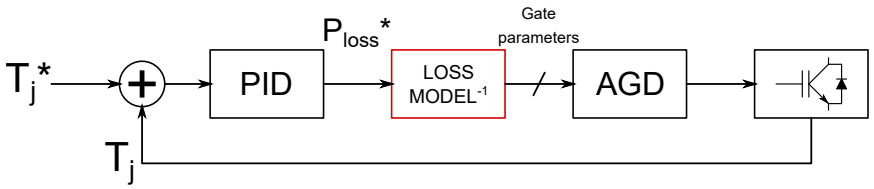


Figure 4.4: Block schematic of feedback ATC.

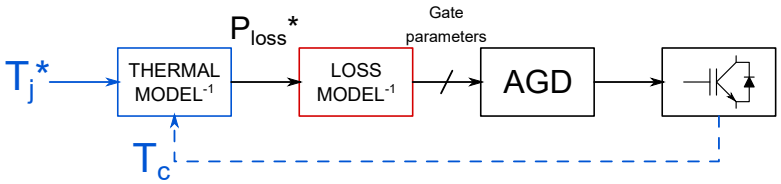


Figure 4.5: Block schematic of feed-forward ATC.

model-based controls. For example, if a model for the junction temperature is used, its accuracy can be improved by feeding it with a measurement of the case temperature. This is represented by the dashed lines in the previous figures: if the case temperature is known, it can be supplied to the thermal model to improve its performance.

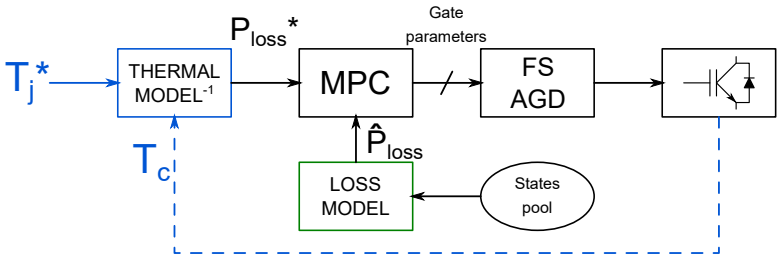


Figure 4.6: Block schematic of Model Predictive Control ATC.

4.2 Free-wheeling diode ATC

A simple way to control losses of power devices with embedded diode is by exploitation of the free-wheeling current flow as enabler of alternate loss distribution; this is called Free-Wheeling Diode ATC (FWD-ATC). In half-bridge converters it is customary to command the device turn-on even when it is discordant. This ensures loss minimization in the case of MOSFETs, and easy driving with IGBTs. Breaking this rule allows to make some current flow on the diode part of the device (if any), possibly increasing losses in a controlled way. In this case conduction losses are mainly involved. Moreover, losses can be localized in a precise part of the device, as it will be discussed later in more detail.

4.2.1 Conduction mode

Figure 4.7 reports the output characteristic of a SiC MOSFET with intrinsic body diode. It is clearly understood that when the device is discordant (i.e. drain current goes negative), the conduction can happen on the MOSFET part of the device or on the intrinsic diode, depending on the gate voltage level. The main difference is in the resulting voltage across the device, that is usually higher in the case of the diode. Moreover, MOSFETs exhibit symmetric characteristic and hence equal on-state resistance regardless of current direction only if fully on.

A simple strategy for ATC can be derived based on these assumptions. The half-bridge current can be monitored over time and whenever the selected device is discordant, proper action is undertaken. If losses are already at the desired value, the device control terminal is driven high, allowing MOSFET conduction and thus minimizing losses. If more losses are required, especially when the load current is low, the control terminal is driven low and diode conduction happens, increasing heat generation on the diode itself. The loss modulation can happen in time: depending on the desired average amount of losses, diode conduction is forced only in some PWM periods and not in others.

The result of this kind of modulation is reported in Figure 4.8: when device negative current occurs, the gate remains off. This is an unusual gate pattern, but it

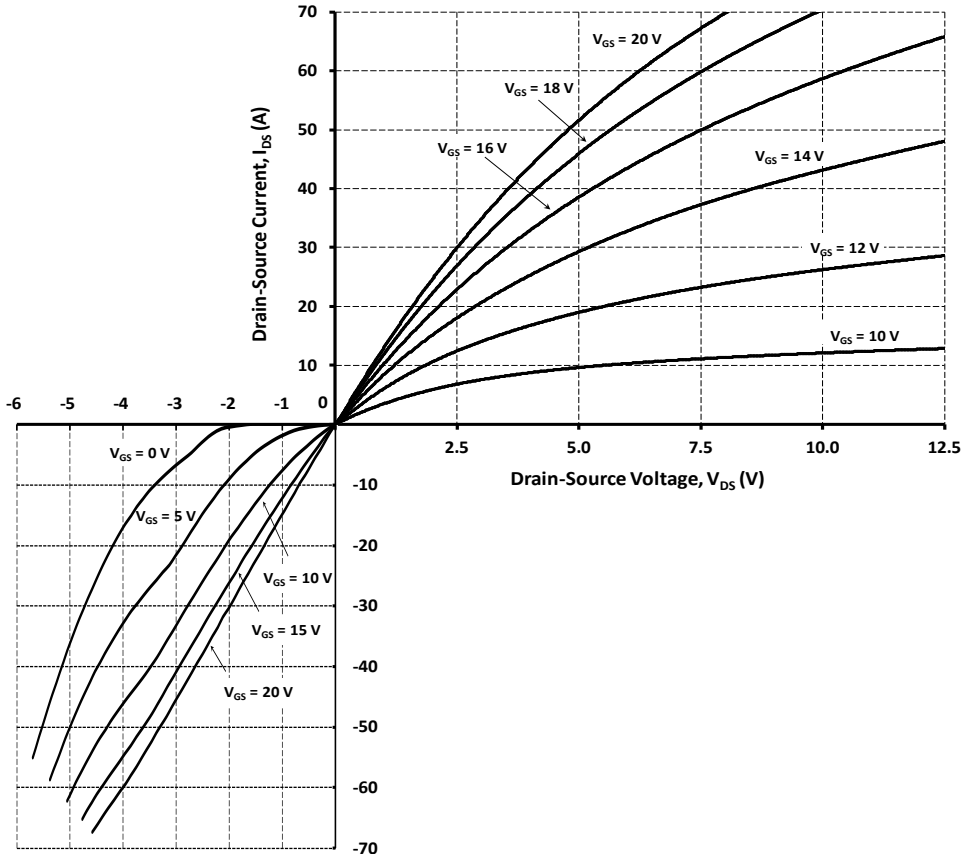


Figure 4.7: Forward and free-wheeling characteristics of Wolfspeed C2M0080120D SiC MOSFET.

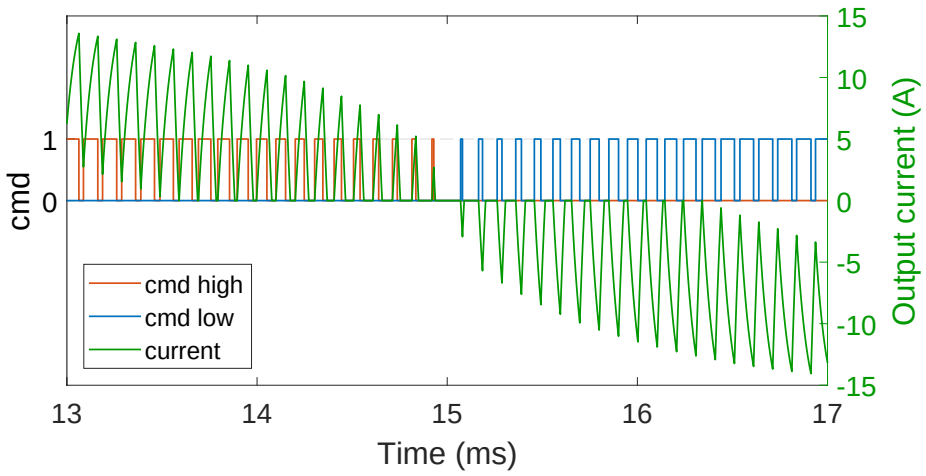


Figure 4.8: Gate patterns synchronized with the output current, with continuous and discontinuous mode of operation when using FWD-ATC.

can be actuated without any intervention on the gate driver. However, it is important to know the exact current direction, to avoid distortion of the output waveform, due to unexpected discontinuous mode. The loss control system described can be represented by two states: loss by MOSFET or loss by diode.

4.2.2 Applicability and limitations

A necessary prerequisite for the implementation of FWD-ATC is the existence of a free-wheeling diode. Another requirement is the negative-current conduction capability of the controlled switch. The free-wheeling diode is usually always present to deal with the inductive component of the load. The main issue relates to the origin and position of this diode. As already explained in Section 1.1, the diode can be a discrete component outside of the controlled power switch (mandatory for BJTs), the intrinsic diode of the MOSFET or the co-packed diode of an IGBT. Depending on the type, different results can be achieved.

In the case of a monolithic diode, FWD-ATC can be used to directly control the

power loss of this component, or to relieve stress on the main power switch, provided that this last can carry negative current. If the diode is intrinsic, FWD-ATC allows to partially control the device temperature, since both loss mechanisms (diode- and MOSFET-like conduction) occur in the same physical medium (the die) and the diode can deal with missing losses if heating of the device is needed. Co-packing of diodes usually adopted for commercial IGBTs is somehow in the middle: diode and IGBT losses occur in different dies, but they share the same baseplate, and hence have a limited temperature correlation. Nevertheless, since most of the IGBTs are not able to reverse conduct, FWD-ATC is not applicable, since the diode is always excited regardless of the gate signal of the controlled device.

A limitation of FWD-ATC is its possible effect on the output waveform when high current ripple characterizes the system. If the ripple is relatively high and the PWM modulation signal varies slowly, a change in the sign of the current can happen in the middle of a PWM period and repeat for many cycles, until the modulation signal reaches a sufficiently high value (higher than the peak ripple). Depending on the policy adopted for the no-trigger of the gate, reduced loss increase or waveform distortion can occur. The first happens when the device is fired for the half PWM period and current changes from positive to negative, while the second occurs if the gate is not fired and current changes from negative to positive. In this last case, the output waveform is distorted, because the output node is left in high-impedance state for a certain time amount.

This behavior can be ascribed to a discontinuous current mode operation of the half-bridge, and if properly compensated the output voltage can be made unaffected by this ATC technique.

FWD-ATC, like all ATC techniques that rely on current-induced losses, has limited control capability, since the higher bound of achievable losses is limited and related to the load. However, as Figure 4.9 shows, a limited improvement beyond the no-ATC case can be achieved. Moreover, this technique combined with others can be the only feasible if a separate diode is used and thermal control of this part is required.

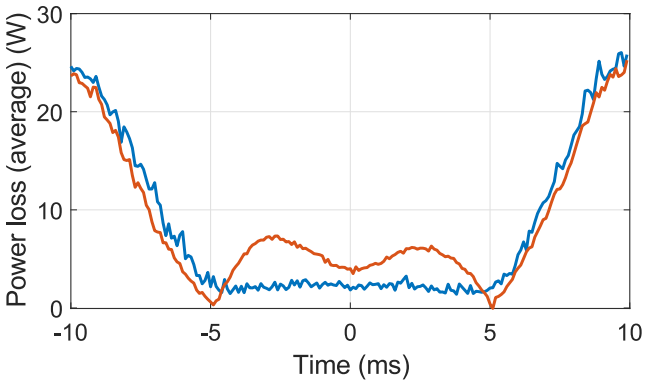


Figure 4.9: Power loss comparison for the low-side device in absence of ATC (blue) or with FWD-ATC (red), with sinusoidal output current.

4.3 Voltage and resistance ATC

One of the limitations of FWD-ATC and other ATCs that exist in literature is that they address only one type of losses [77, 85, 86, 87]. FWD-ATC works on free-wheeling loss (that can be interpreted ad a special kind of conduction loss), authors who change the gate voltage address conduction losses, while switching frequency change works on switching losses.

A possible starting point for a new ATC technique is in the integration of different types of loss, to expand the regulation capability. This produces the Voltage and Resistance ATC (VR-ATC) and its variant VRD-ATC, that embeds also the diode conduction presented in the previous section. Figure 4.10 represents the effects of a 2-state VR-ATC on the case temperature of a device undergoing a step load reduction; its intervention is able to reduce by 35% the thermal swing seen at the device periphery.

Here this ATC, already seen in literature (although in "separate" form, with voltage and resistance decoupled), embeds the FWD-ATC. The resulting VRD-ATC uses the high-level of the gate voltage to determine conduction loss, the output resistance of the gate driver (instead of the PWM carrier frequency) to regulate switching loss and the gate pattern to activate free-wheeling losses on the (intrinsic) free-wheeling diode.

A first consideration shall be made: the voltage-and-resistance part of the thermal

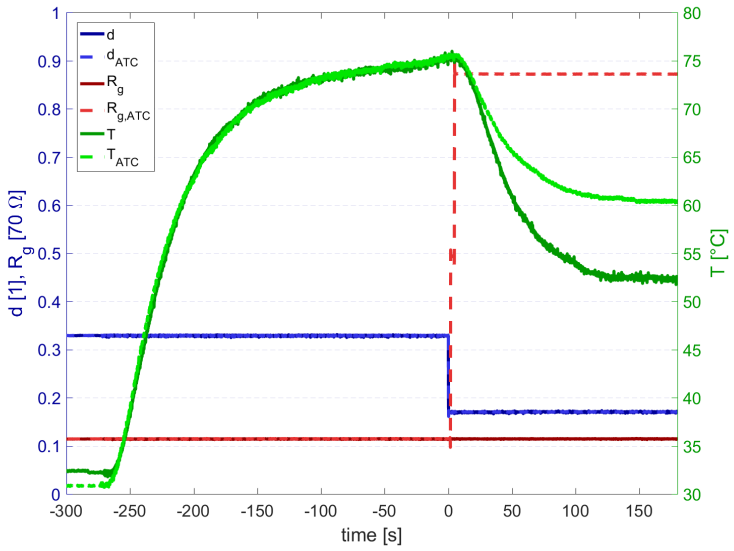


Figure 4.10: Experimental proof of concept of the VR-ATC: the case temperature of the device is sensed in correspondence with a load step, with and without ATC (in this case only two driver states are used).

control operates separately from the free-wheeling part. The first works when the device is concordant, while the latter suits the discordant moments. This means that the control is different for the two device conditions, but no cross-coupling between the two techniques occurs.

4.3.1 Model Predictive Control

Using MPC strategies to achieve good ATC performance is not a new idea: in [88] MPC is applied with success to achieve thermal control in a drive, acting on the modulation vector rather than using AGDs. In these control architectures, accurate knowledge of the results of a particular control choice are essential; for ATC this means that an accurate loss model is needed.

The purpose of correlating voltage and resistance values of the AGD to the

achievable power loss can be accomplished by using one of the models presented in Chapter 3. Moreover, since a Finite Control Set (FCS) is preferable for MPC implementation, only some AGDs architectures can be effectively employed to achieve the voltage and resistance regulation: if the discrete state gate driver proposed in Section 2.2 is used, the possible number of actuated values is finite. It is also expected that the number of possible states is limited, since it is strictly connected with gate driver size, cost and reliability.

Given a finite number of feasible states for the gate driver and a model relating this states to the device loss, a natural methodology to implement the thermal control is MPC. In fact, the chosen loss model can be evaluated on each of the states, described by a couple (V_{ggh}, R_G), and the state with the minimum error with respect to the target loss is chosen.

This solution exhibits many advantages. Firstly, it is quite simple to be implemented, once a loss model is available. Secondly, it acts as an inherent modulator, so it automatically switches between different states if an intermediate value is required and cannot be realized exactly by a specified state. Lastly, analytical models can be used *without any inversion*, since MPC requires the direct model only. Moreover, since the number of states is usually limited, the empirical models described in Section 3.3 can be simplified, requiring a lower number of steps or measures to be evaluated.

4.3.2 Working region

There are some theoretical limitations applicable to VR-ATC. These are connected with the fact that both types of loss are related to the load current and, hence, cannot vary on an arbitrary range. Using (3.6), the minimum conduction loss is achieved with the highest gate voltage, hence it is limited by the gate breakdown:

$$P_{on,max} = dI_\ell(V_{gs,max} - V_T)\left(1 - \sqrt{1 - I_\ell / I_{sat,max}}\right) \tag{4.1}$$

The achievable conduction loss is theoretically limited by (3.11), achieved in correspondence of $V_{gs} = V_M$, i.e. the desaturation limit of the power switch. Practically, this value is not reachable, and a margin of 10 to 20% should be accounted for on V_{gs},

giving:

$$P_{on,min} = dI_\ell(mV_M - V_T)\left[1 - \sqrt{1 - \frac{2I_\ell}{k(mV_M - V_T)^2}}\right] \tag{4.2}$$

where $m \in [1.1, 1.2]$ is a safety margin, depending on confidence of the Miller voltage model and accuracy of voltage actuation by the gate driver. Similar considerations applied to (3.27) and its dependencies show that the maximum switching loss occurs for high R_g and low V_{gs}, while minimum loss requires low R_g and high V_{gs}.

As already hinted above, both P_{on} and P_{sw} are infinitesimal as $I_\ell \to 0$, resulting in very small losses at low currents. This poses a strong limit to the applicability of the VR-ATC to the concordant device in AC applications. In these cases, the current is forced to cross the zero, to reverse and draw the sinusoidal (or similar) output. In this condition, VR-ATC is useless, since losses cannot be increased as desired.

Depending on the value of the load current, it is possible to use VR-ATC (without the need of VRD-ATC extension) in DC/DC converters, where the current can change on a wide range but without crossing zero. The effectiveness of VR-ATC in these cases depends on the feasible values of voltage and resistance: solving (3.6), (3.19), (3.22), (3.25) and (3.26) for the corner values of voltage and resistance, the power-to-current relationship can be found and the residual power ripple for the mission profile determined.

The limitations of this ATC emerge clearly in Figure 4.11 (simulation) and 4.12 (experiment), where the power loss of a MOSFET in the low-side of a half-bridge inverter with sinusoidal output is depicted. The VR-ATC curve (in yellow) is completely enclosed between the no-ATC curve (blue) and the red curve, representing the minimum feasible gate voltage. The red curve represents the most annoying limit, and the resistance contribution can help little; this could be a limitation of the test parameters used: the SiC device was used with $f_c = 10\,\text{kHz}$, so the contribution of switching loss is limited. The central part of the figure corresponds to the free-wheeling conduction phase: without embedding the FWD-ATC technique in the control, almost null power loss is noticed there, and VR-ATC cannot change the result, since it works only for the concordant device. The good accordance between the two figures denotes the correctness of the models used to assess the performance of the ATC.

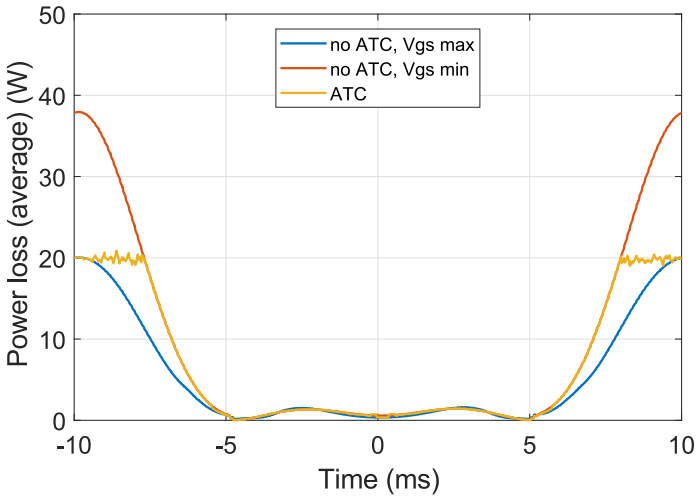


Figure 4.11: Simulation performance of VR-ATC of the low-side device of a half-bridge inverter with sinusoidal output current (yellow), no ATC result (blue), traditional gate driver with low output voltage (red).

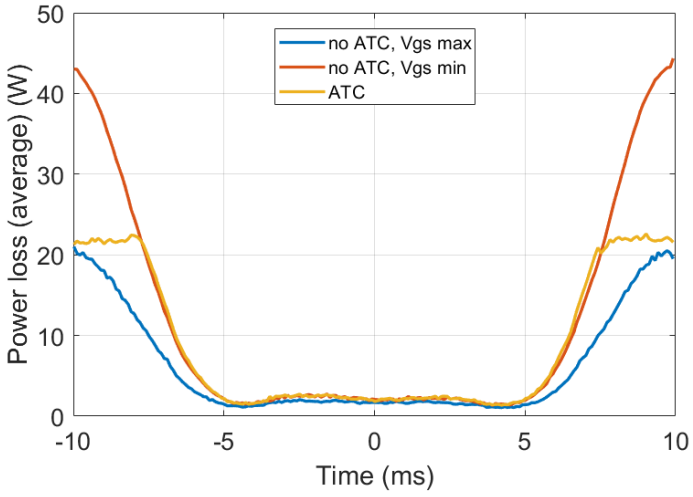


Figure 4.12: Experimental performance of VR-ATC of the low-side device of a half-bridge inverter with sinusoidal output current (yellow), no ATC result (blue), traditional gate driver with low output voltage (red).

4.3.3 Device loss distribution

From what has been discussed so far, the same amount of loss $P_{tot} = P_{on} + P_{sw}$ can be determined using different values of P_{on} and P_{sw}. If the gate driver has a finite number of states, this consideration is scarcely important, since the total loss value of each feasible working point is hardly redundant. In case of continuous range of attainable voltage and/or resistance, this redundancy can be exploited.

In this case, MPC is difficult to be implemented, and control schemes based on loss model inversion can be used. To have an injective function from P_{on} to (V_{ggh}, R_g), another parameter should be given, describing the *relative* amount of the two types of loss. The *Loss Distribution Coefficient* (LDC) r is thus defined as:

$$r = \frac{P_{sw}}{P_{tot}} = \frac{P_{sw}}{P_{on} + P_{sw}} \tag{4.3}$$

This means that $P_{sw} = rP_{tot}$ and $P_{on} = (1 - r)P_{tot}$. This simple approach can help in making the loss model invertible, allowing the use of continuous state gate drivers.

The definition of the LDC is far more than a mere mathematical expedient: it is related to the distribution of loss by type in the device and somehow connected to its fabrication parameters. Mathematically speaking, the LDC is limited by definition between 0 and 1. The extrema are not practically feasible, since $r = 0$ would result in a device without switching loss, and $r = 1$ would mean no conduction loss. This means that r is limited by both device parameters and working conditions: the range of valid values depends on many load parameters, such as switching frequency f_c and load current I_ℓ.

The "device-dependent" range of r is an indicator of the natural losses of the device, and can vary depending on its technology or designed target application; the "system-dependent" part is instead related to the working point chosen by the system designer. This means that the choice of r is not free, and fixing it to a special value could need some back-calculation in order to solve the inverse model.

Figure 4.13 reports some simulations that show the range of possible LDC values with respect to some load parameters. As it can be seen, the definition of the LDC is necessary, but of limited practical interest since little variability is possible. Nev-

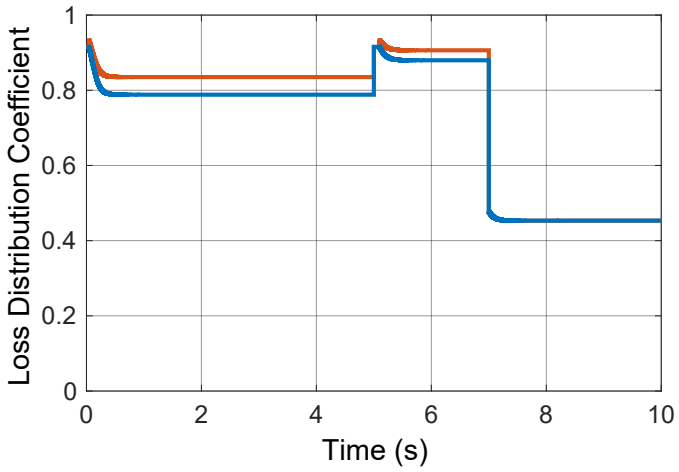


Figure 4.13: Loss distribution coefficient maximum (red) and minimum (blue). At $t = 5$ s a set-point step is commanded, while at $t = 7$ s a load step occurs.

ertheless, this result is partial and could be related to the particular device chosen or loss model adopted.

4.4 Shoot-through ATC

In Section 3.4 a new type of loss was introduced, other than those widely described in the previous part of this work. The feasibility of a gate driver to activate this type of loss, described in Section 2.3, suggests the possibility to control loss and hence temperature relying mainly on this heat generation mechanism. This is realized by Shoot-Through ATC (ST-ATC) [89].

The gate driver for ST-ATC is even simpler than that of VR-ATC, differing from a traditional driver only for the existence of the third voltage level. Moreover, since the heat is generated by a shoot-through current, its operation is transparent to the load, and very limited distortion or change in the output is noticed.

4.4.1 Loss model and driver control

To correctly control the power loss of the device, two models are needed, since the actuated losses are of different kind than the natural ones of the device. A simplified model tuned on the "usual" gate voltage and load parameters can be used to estimate the natural loss of the device. Then the difference between the target loss level and the natural one is computed. This differential loss can be obtained by the operation of the device in shoot-through mode: the detailed inverse model of Section 3.4.3 is used to obtain the shoot-through time, then actuated by the gate driver.

What is most interesting about ST-ATC is that the artificial loss mechanism can work under whatever load condition, even with null or negative current on the device, provided that enough margin is available in the duty-cycle. This means that a device need not to be concordant, and losses are not upper-bounded by the load current. Operation of ST-ATC supersedes also FWD-ATC, if the thermal problem is focused on the controlled device rather than the diode: shoot-through losses, being related to the current controlled working mode, occur in the die of the device itself.

All these benefits can easily be seen in Figure 4.14, where the loss profiles achieved by different ATC techniques in case of sinusoidal output current are collected. Two traces are present for the ST-ATC, one in the case of cold device and the other for the hot operating point. ST-ATC is effective in controlling power in both conditions. Moreover, the correct operation in the hot situation backs up the discussion of Section 3.3.3: the only requirement for a loss model tuned on a specific temperature is its stability in moving the system to the steady-state point.

4.4.2 Device and driver mismatch

In Section 3.4, shoot-through losses were modeled with explicit reference to the shoot-through current I_{st}. It should be noted that I_{st} is not directly determined by the gate driver, which instead acts on the gate voltage using the third, additional level. As it is clearly highlighted by the SH model and other device equations, high transconductance switches exhibit a steep relationship between the controlled quantity and the current. This implies high sensitivity between the primary quantity (control

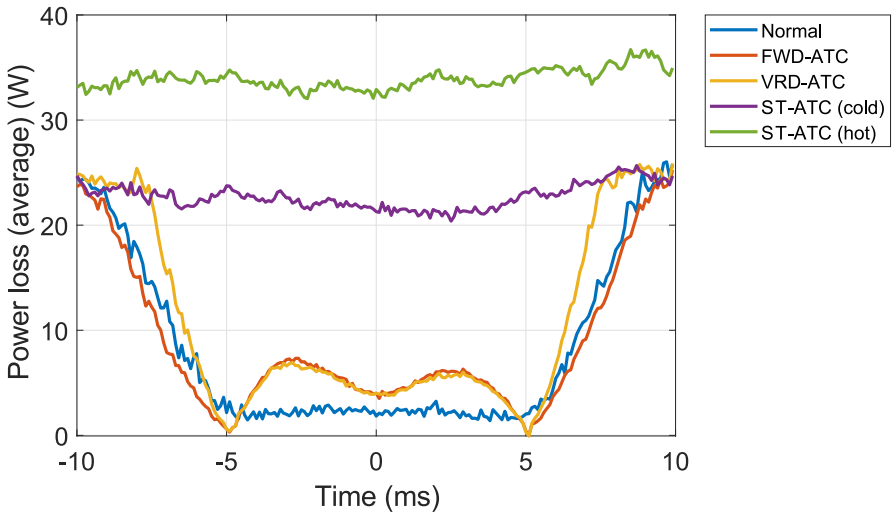


Figure 4.14: Measured power loss for different ATC techniques: normal driving operation (blue), free-wheeling diode ATC (red), voltage and resistance ATC (yellow), shoot-through ATC (purple and green, for cold and hot devices, respectively).

terminal voltage or current) and the power related one (the shoot-through current). The high sensitivity between the two quantities exposes the system to the effects of mismatch in the power device and its gate driver circuit: some tolerance on device threshold or transconductance, or in the value of the third gate voltage can result in different values of I_{st} for the high- and low-side devices on the half bridge.

Mismatch is probably the main critical point of ST-ATC: asymmetric shoot-through current for the two devices of a leg can result in a high imbalance of the shoot-through times, that in turn limits the maximum duty-cycle. Since in AC drives the output should be symmetric, the tightest limit on duty cycle will be adopted also for the companion device, resulting in suboptimal performance.

Moreover, a symmetric I_{st} for the two parts of a leg would result in simplified control: the shoot-through time would be symmetrical, too, and computation of the optimal value could be performed only for one switch and repeated, shifted in time, for the other.

When mismatch cannot be avoided, some countermeasures can be adopted. Focusing on the minimization and equalization of the shoot-through times, the gate driver structure can be modified in order to be able to *tune* the difference between the fully-on level and the shoot-through voltage. Of course, a gate driver as in Figure 2.13 is not suitable, since the voltage drop across the Zener diode cannot be varied without modifying the hardware.

The third voltage can be moved until the shoot-through current is almost equal for the two components of the same leg, at least for a given temperature. A tuning procedure can be performed as follows: a shoot-through pulse is fired for each device using a first tentative value, measuring the resulting current; other pulses are fired changing the shoot-through voltage, until the currents are equalized. Some fine tuning can be performed once the device has reached its target temperature.

In general, some mismatch should be accounted for, since it is difficult to completely compensate device differences under a wide temperature range.

4.4.3 Safety and lifetime considerations

It is natural to perceive operation in shoot-through condition as potentially harmful for the devices. Firstly, it is well known that the short-circuit withstand capability of IGBTs, despite being of some microseconds, is limited by the number of occurrences, that should not exceed one thousand. Moreover, the short-circuit capability of many MOSFETs can be of few microseconds, and this could suggest an upper limit for the pulse duration [31, 90, 91, 92].

In practical terms, it must be noted that the shoot-through condition is very different from a real short-circuit, despite both revealing themselves as a current flowing along the bridge leg. In short-circuit, the device is forced in the saturation region by clamping the drain, while the gate is fully on, this implies that the current is limited only by the number of carriers available in the channel and can reach very high values. On the other hand, in shoot-through, the gate is driven at an intermediate value, and the operation of the device is limited by a pinched channel. This suggests, and the experimental outcomes confirm, that from the point of view of the potential damage the two conditions are radically different.

During the tests, a commercial SiC MOSFET (Wolfspeed C2M0080120D) survived more than 3 millions shoot-through cycles without any noticeable damage. This proves that the two conditions are not equivalent and specific qualification of the device from the shoot-through point of view should be performed.

Another concern is related to the possibility of thermal runaway and subsequent secondary breakdown of the device due to the limited gate voltage during the shoot-through phase. It is known that a poor gate voltage could result in uneven current distribution across the cells of the power device, leading to the current-crowding phenomenon. For majority-carrier devices this should not be a problem due to the inherent negative feedback provided by the thermal coefficient of the conductance, but repetitive operation under these conditions could reduce the lifetime of the device, or reduce its current capability at constant lifetime.

At present, there are no known motivations for the device not suffering the shoot-through. A possible theory, that still needs to be verified, is that the ST pulses always alternate with fully-on phases: the author believes that the strong pulses contribute to a carrier distribution "reset", equalizing the local properties across all the cells of the die. This could greatly improve the resilience of the device to the condition.

4.5 Reliability-efficiency trade-off

All kinds of device level ATC rely on device loss to control the temperature. This loss are usually additive, i.e. they are induced on purpose and would not exist in the base circuits. Using power to heat the devices has the result of reducing the converter efficiency and this is usually undesired, because of its many negative consequences.

The only situation under which this is tolerable or even positive is when the efficiency reduction is counterbalanced by an improvement of some other performance indexes. Reliability is surely one of these, but others are possible, such as the startup time, the operating range of the system and the insensitiveness to some disturbances.

When ATC is used in the attempt to improve lifetime of a power converter, the sensitivity of reliability improvement towards the temperature swing reduction should be evaluated. This supports the system designer in understanding the amount of power

loss correction that is needed to achieve the target reliability. Of course this works as far as temperature cycling is the main reliability bottleneck. This depends on many factor, such as: environment, design margin, working cycle, dispersion of production parameters and many others [93].

Establishing accurate metrics to link ATC intervention to the achievable reliability level is outside the scope of this work, but it is gaining more interest from the scientific community. This is related to the effort of exploiting the potential of electronics in areas where its widespread adoption is limited by reliability issues.

What can clearly be stated here is that many different ATC techniques exist, but only some of them are able to force the device into a constant power loss condition. The zero power ripple feature is not a strict requirements for ATC: since the sensitivity between temperature swing amplitude and achievable lifetime extension is supposed to be high, if only minor improvement is needed, even a small reduction in temperature fluctuation could be sufficient. Nonetheless, the swing reduction should be computed against a realistic working cycle and thus it is difficult to determine which kind of ATC best suits each application [94].

4.5.1 Relative Power Ripple as figure of merit

Ascribing the choice of ATC type and working load to the final application does not mean that some discussion about it is not possible. First, some metrics should be defined to quantitatively describe the many, different ATC techniques employed and presented here or elsewhere.

In this attempt, a system-global metric is defined, in order to describe the possibility for a particular ATC technique, implemented in a specific system, to attain the desired reduction in power ripple, being this strictly connected to the temperature ripple (see Section 4.1.2 and following).

This is the *Relative Power Ripple* (RPR) and it can be computed from simulations or experimental results, showing the power loss profile as a function of the load. The working cycle of the converter should be meaningful for the application (e.g. a low-frequency sinusoid for a drive, a stepped square wave for a DC/DC converter with impulsive load, . . .) and the total device loss for a single power switch should

Table 4.2: Quantitative comparison of various ATC techniques.

ATC type	Efficiency	μ_{loss}	σ_{loss}	RPR
None	0.992	8.17	8.16	1.0
FWD-ATC	0.992	8.68	6.88	0.79
VRD-ATC	0.989	10.9	8.84	0.81
ST-ATC (cold)	0.977	22.7	1.17	0.051
ST-ATC (hot)	0.966	33.9	0.942	0.028

be evaluated. Then, loss average value (η_{loss}) and standard deviation (σ_{loss}) are computed. The RPR metric is hence defined as:

$$RPR = \frac{\sigma_{loss}}{\eta_{loss}} \tag{4.4}$$

This metric is *global* since it is computed on a wide working range rather than in a single point; RPR is *positive-defined*, since it is the ratio of non-negative quantities; it points at better ATC performance as it tends to zero. Moreover, practical measurements demonstrated that for a common drive without any ATC technique $RPR \approx 1$; of course, if zero power ripple is achieved, $RPR = 0$. Table 4.2 reports the results of the RPR metric for the different ATC techniques examined: lower values point at better ATC performance. ST-ATC achieves almost zero power ripple with both cold and hot device.

Despite its advantages, RPR is an aggregated metric, an this causes some information loss. In fact, it lacks an explicit relationship with the thermal bandwidth of the system; thus it cannot be directly related to the temperature ripple, unless very slow working cycles are supposed, thus guaranteeing in-band operation on the thermal Bode diagram of the system.

To assess the achievable improvement in the system lifetime, some preliminary simulations can be performed. They need a model of the chosen ATC technique, a thermal RC network of the system analyzed and a reliability model to correlate

temperature behavior to the system lifetime. These will be briefly discussed in the following.

4.5.2 Lifetime estimation models

Correlating the lifetime of a complex system to its environmental and operating parameters has been a long effort in literature [93, 95, 76]. Many models in this field are empirical, yet used effectively in the academic and industry world [96]. In some of these, many system variables are managed, and an important number of tests is needed to tune the model parameters. One simple yet well known and established method to forecast system lifetime when the temperature is considered as the main stress factor is the combination of Coffin-Manson and Arrhenius models, that can sometimes be referred to as Norris-Landzberg model, if the cycle frequency is neglected:

$$N_f = A \cdot \Delta T_j^{\alpha} \cdot \exp\left(\frac{Q}{R\,T_{j,avg}}\right) \tag{4.5}$$

where N_f is the number of temperature cycles to failure, ΔT_j is the cycle amplitude, $T_{j,avg}$ the average temperature, A, α and Q are specific constants of the process and R is the gas constant. This model can be used effectively when failure mechanisms such as bond wire lift-off and solder joint fatigue are considered. If more accuracy is needed, other factors can be considered in the model, resulting in the Bayerer model [97].

Despite its simplicity, this model shows one of the most important considerations that can be made on the reliability issues connected to thermal stress: the lifetime of the system depends *exponentially* on the reciprocal of the average temperature, and with a power law on the cycle span. Depending on the values of the parameters and on the specific range of interest for power electronics devices, one contribution can be higher than the other. Literature results show that thermal cycle amplitude has great impact on the lifetime, and simulations can help in forecasting the achievable benefits.

Figures 4.15 and 4.16 show some simulations that were set up to assess the achievable reliability improvement made possible by various ATC techniques under some practical working load profiles. The two figures highlight power loss and estimated

junction temperature when the VR-ATC is used with sinusoidal or square-wave loads. Depending on the power set-point used for the ATC, the load current profile and the intrinsic effectiveness of the particular technique analyzed, different temperature profiles are obtained. Using the aforementioned reliability model, the expected lifetime of the system can be inferred; results are described in Table 4.3, where the expected time to failure is computed from the number of cycles in (4.5) distrubuted on a typical working cycle. The result marked with an asterisk is obviously a degeneration of the model: such a long lifetime is hardly possible, and the explanation behind the result could be in the missing reliability modeling of the driver, the incorrect parameters (that come from [93] rather than being tuned on the particular device used) or some asymptotic behavior of the model itself, that cannot describe correctly aging mechanisms of non-thermal origin. What is true is that ATC can bring an important relative change in the expected lifetime.

These results show that the same type of ATC can improve or even deteriorate reliability. Mostly important, the zero power ripple condition, when possible (due to a special ATC technique or a particular load profile), can be also unneeded, since it lowers the efficiency while incrementing the lifetime beyond the limit of practical interest (the target system useful life).

The strong result of this kind of simulation, despite the limits of the reliability models and parameters, is that the "amount" of ATC used in the application can *adjust* the balance between reliability improvement and efficiency decrease. This opens up a wide range of possibilities, since it points out that Active Gate Drivers and Active Thermal Control can participate in the Design-for-Reliability of modern power conversion systems. To practically implement this aspect, more quantitative knowledge about the trade-off should be collected. This is outside the scope of this work, but it represents one of the strongest suggestions for the continuance of the research in this field.

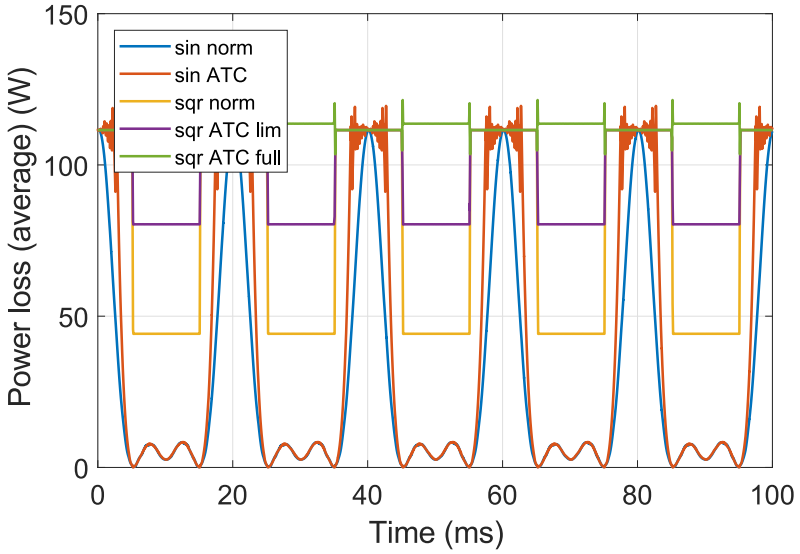


Figure 4.15: PWM-average power loss profile of systems with different loads and ATC intervention: sinusoidal load and no ATC (blue), sinusoidal load with VR-ATC (red), square-wave load without ATC (yellow), same load with partial (purple) and full (green) VR-ATC.

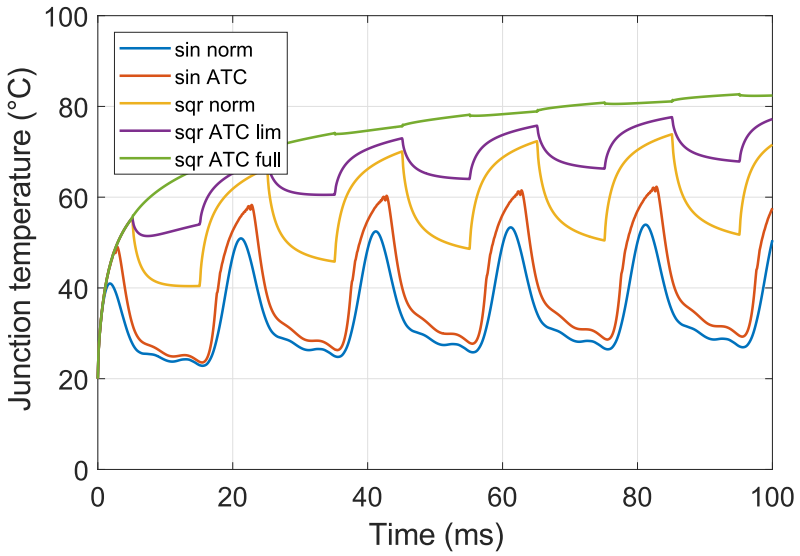


Figure 4.16: Simulated junction temperature profile of systems with different loads and ATC intervention: sinusoidal load and no ATC (blue), sinusoidal load with VR-ATC (red), square-wave load without ATC (yellow), same load with partial (purple) and full (green) VR-ATC.

Table 4.3: Expected time to failure for the power device under different load conditions and ATC levels (simulation data). The asterisk denotes numerical values that need special considerations.

Test case	P_{loss} [W]	$T_{j,avg}$ [°C]	ΔT_j [K]	η [%]	Exp. lifetime [years]
sin norm	28	36	27	98.8	1.5
sin ATC	39	42	33	98.4	0.3
sqr norm	78	63	23	98.9	0.3
sqr ATC lim	96	73	11	98.6	7.0
sqr ATC full	112	82	1	98.4	996000*

Conclusions

This work started with an overview about the layouts of the main power electronic switches, in order to understand the differences among them and to figure out if and where modern wide band-gap devices deviate from traditional parts. Some gate drivers from literature were presented as well, together with a general model suitable for the study of the switching behavior of devices working inside different converter architectures. This model was identified in the half-bridge, that can be easily discovered inside buck, boost, full bridges and simple three-phase converters.

The state of the art in gate drivers showed that this ancillary circuit is essential for the exploitation of performance of both traditional and wide band-gap devices. Depending on the requirements of the application, they can be used to simply switch on and off the device in safe conditions, or to control the EMI profile, shape the slew-rate of their waveforms, control their losses, determine their condition or even measure some stress and temperature internal parameters.

After that, special attention was paid to the possibility to control the time derivatives of the switched quantities (voltage and current), in order to restrict overshoot or ringing phenomena, more common as devices speed up. Starting from literature work, extensive simulations showed that limiting the extension of the working area of a device is not simple; especially when the art was not well described. This led to the identification of some key points for the understanding of the switching behavior and to the synthesis of a state machine that could easily determine how to react to the transitions of the switching device. Moreover, the Switching Locus Area Ratio (SLAR) was identified as an interesting figure of merit, since it is capable to concentrate in a

single number how much a gate driver can move the working trajectory of a switch close to its ideal location.

With this expertise, the development of new Active Gate Drivers was started. The Voltage Controlled Power Resistor (VCPR) aimed at a continuous range of variation of the gate resistance, but its study revealed itself as cumbersome and too slow for WBG devices. Merging two different types of stepped gate driver, simultaneous voltage and resistance variation was concentrated in a single AGD, making a small step with respect to the state of the art. The major advancement was made by the introduction of a very fast and simple gate driver, that differs from traditional ones only for the possibility to generate narrow pulses with an intermediate voltage between fully-on and fully-off. These gate drivers were implemented, tested and modeled, in order to determine their limits and optimizing their design to obtain the desired performance level.

The desire to employ AGDs for Active Thermal Control called for an accurate computation of natural and forced losses in power devices, taking into account the types of load and the different loss mechanisms activated. The simple SH model was firstly applied to identify essential trends and limits; the results were then compared to more accurate yet less theoretically sound empirical models. The "brute force" SPICE model is supposed to yield best accuracy, but the much simpler extension of datasheet parameters, if performed properly, can satisfy the loss forecast requirements.

The knowledge about loss was boosted by the study of the shoot-through conduction mode, that is possible only for devices in half-bridge configuration. This new, unusual mode was modeled directly and quantitatively characterized by sound theoretical work. This showed that the ST conduction is the only mechanism known so far to make device loss independent of the load current.

ATC performance comparison and evaluation is the natural consequence of the study about loss modeling and AGDs. Three ATC techniques that were not yet examined in literature were studied. The Free-Wheeling diode ATC revealed itself as a simple, AGD-free technique, but with very limited range of application. Literature work about uncoupled gate voltage and gate resistance control was merged in a simultaneous variation of both parameter, made possible by the developed gate driver:

no essential improvement was found.

Simulations and experiments on Shoot-Through ATC showed that this technique can lead to almost null power ripple, regardless if the device is carrying positive, negative or even no current at all. As such, ST-ATC is believed to be the most promising result of the present work, opening possibilities for the reliability improvement of converters which lifetime is limited by the thermal stress induced by power cycling.

To support these results, the relationship between power loss and temperature was analyzed; the link between temperature and lifetime was modeled using literature equations and the resulting simulations proposed for the design of ATC under a particular application. The Relative Power Ripple metric was introduced as a partial yet effective indicator of the quality of ATC correction.

This approach showed the possibility to improve reliability by the use of ATC, but further experimental work is needed to prove the result. In particular, little results were found about lifetime of modern WBG devices and this is supposed to be consequence of the relative novelty of these devices. Using old parameters valid for old technologies can highlight many trends that could be still valid, but no final assumptions can be made.

Moreover, loss modeling and junction temperature measurement require further research and interest. One possible track of future research could investigate the possibility to derive a loss model from analytical equations that better describe the Vertical MOSFETs and IGBTs: this would be something similar to what was done with SH equations, but better accuracy is expected, due to the natural improved behavior of models developed for a particular device layout. The EKV model is already proposed by some manufacturers into their SPICE cards for SiC MOSFETs, and BSIM or Hefner IGBT model could be investigated as well. Also inversion of the resulting equations can be a non-trivial task, and special expedients could be needed.

The possibility to compare the junction temperature under different measurements or estimation is also very interesting. The current work is based on the assumption that constant loss is sufficient to achieve constant temperature, but comparing the observer-based junction temperature with direct and indirect measures can strengthen the theoretical outcome. In particular, beside the traditional TSEPs, the use of shoot-

through current as indicator of the junction temperature will be addressed. This could help in the automatic tuning of the AGD if mismatch is to be minimized.

What emerges looking at this work from a high-level perspective is that in order to address the challenges posed by the new WBG devices and by the newest silicon designs, a transversal approach is required. Deep knowledge of the device, assumptions about working load and environmental conditions, as well as expertise in the implementation of fast analog and digital circuitry should be in the backpack of the power electronics engineer who wants to fully exploit the potential of the newer devices.

Moreover, EMI issues, mostly neglected here, need special and thorough investigation, since their contribute is expected to be wider as switches work faster. The trend towards high density pushes waveform edges to become steeper, but this moves interest towards passive and parasitic components: in the future, more than today, the performance of a switching circuit will be determined and possibly limited by the interconnections rather than the part itself. This is why the new direction is towards the integration of gate drivers and ancillary circuits together with the power device.

Understanding and controlling finely the switching and conduction behavior of modern power electronics device is one of the key points for the widespread adoption of electronics into those areas were it is still marginal. Much interest is expected in both industry and academia especially in the field of transportation: More Electric Aircraft, More Electric Ships and Electric Vehicles are supposed to be the drivers of the electronic development in the future decades. The author hopes that this work is just the first of many contributes that he will give to this field.

Appendix A

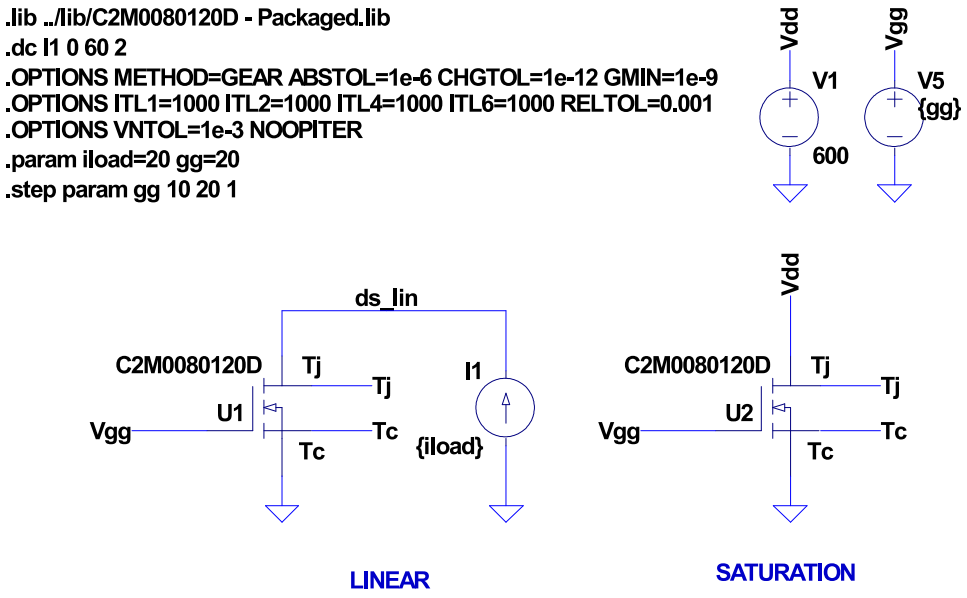
Circuit diagrams

A.1 Simulation bench for power loss modeling

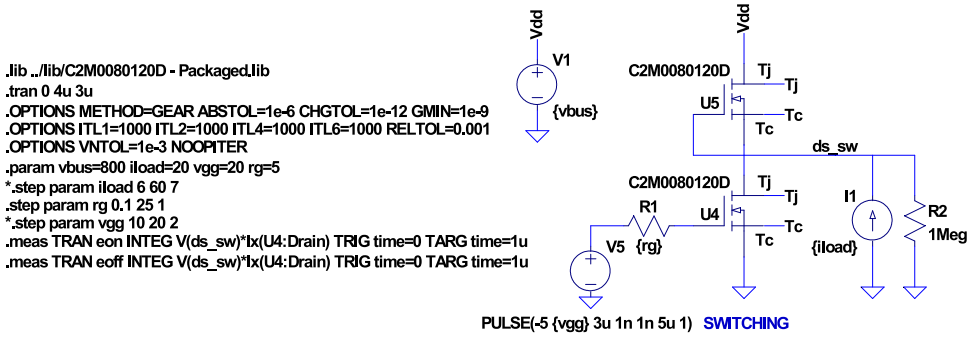
In this section the SPICE circuits used to collect the loss data set needed to implement the fitted model are reported.

A.2 Voltage-Resistance stepped gate driver

In this part of the appendix the circuit diagrams of the voltage-resistance stepped gate driver are reported. This is a hierarchical schematic, where Figure A.2 represents the top-level. This circuit can be easily adapted to become the shoot-through-ready gate driver, by modification of its output stage (Figure A.7).



(a) Conduction and shoot-through loss.



(b) Switching loss.

Figure A.1: Simulation benches to obtain data for loss modeling.

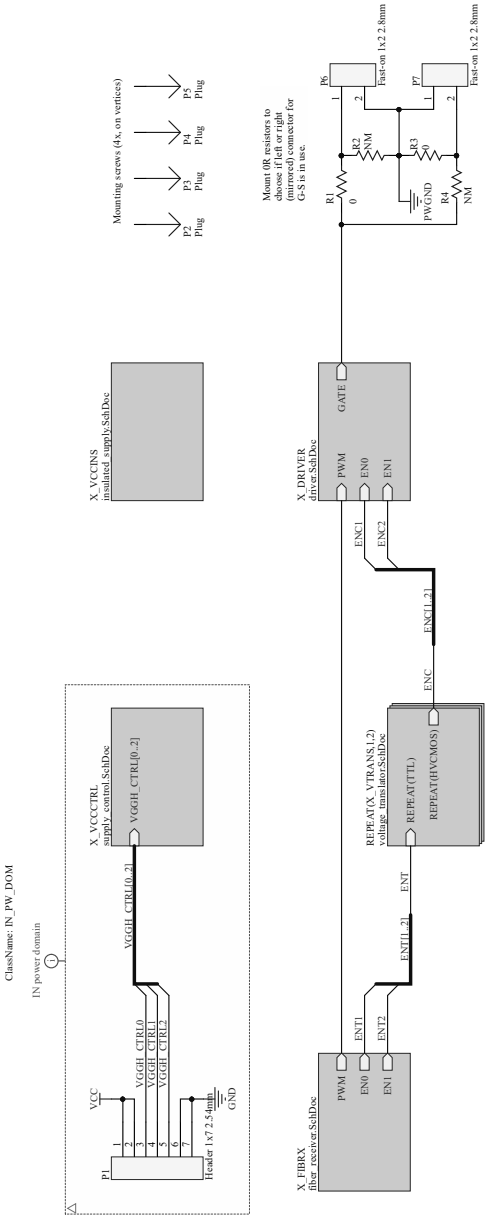


Figure A.2: Top-level schematic of the gate driver with discrete states.

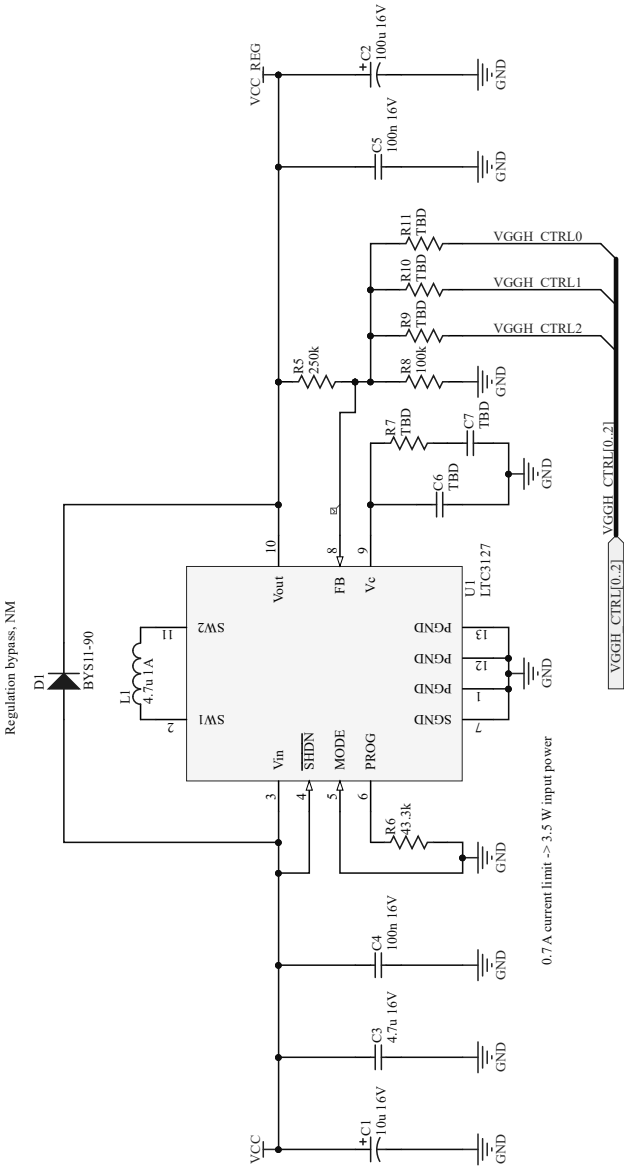


Figure A.3: Variable primary DC supply to regulate the on-state voltage on eight levels.

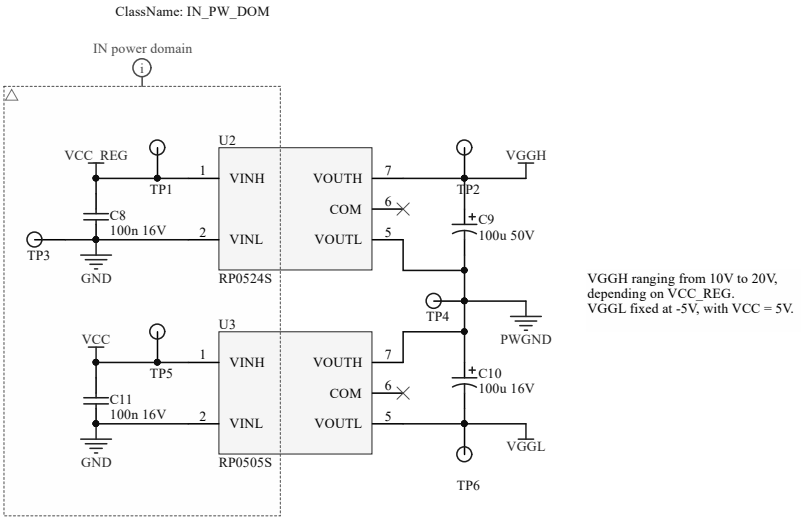


Figure A.4: Isolated DC/DC converter to adapt voltage level to the MOSFET.

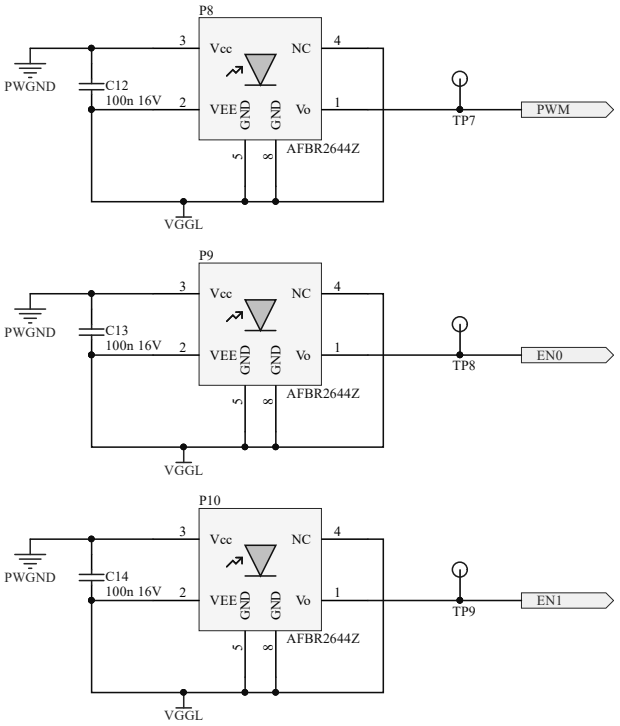


Figure A.5: Fiber-optic command signals.

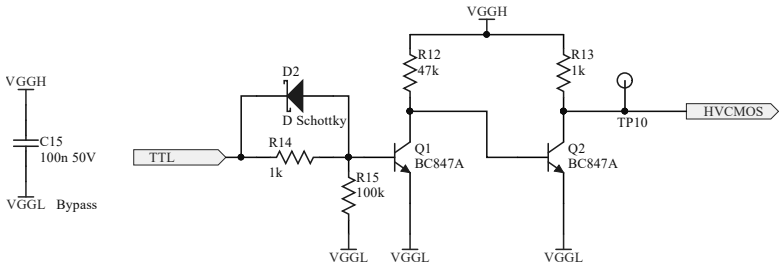


Figure A.6: Level shifter for the enable signals.

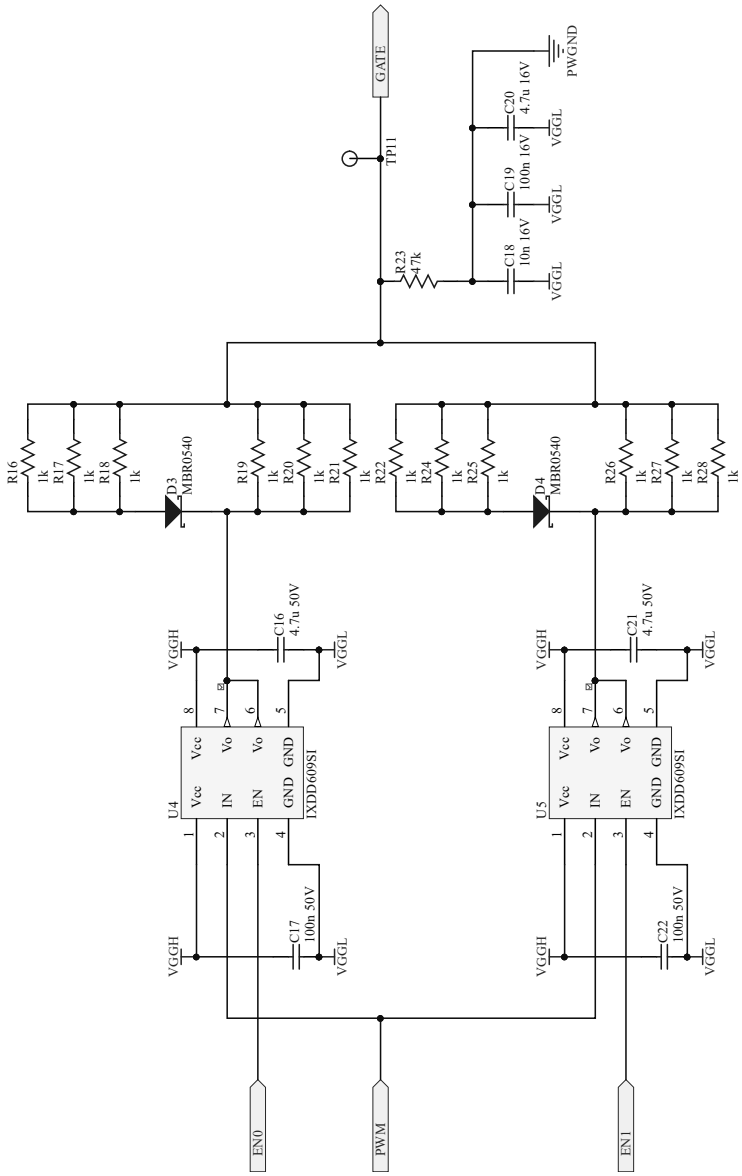


Figure A.7: Output stage with double gate amplifiers in order to actuate three different resistance values.

Appendix B

MATLAB scripts

B.1 Loss models and MPC control

```
function plin = plin_dir(id,vgg,mos,model)
%PLIN_DIR Direct loss model for linear region (on-state)
    if lower(string(model)) == "sh"
        % Neglecting channel modulation effect
        plin = id.*(vgg-mos.Vt_lin).*(1-sqrt(1-2*id./(mos.k_lin*(vgg-mos.Vt_lin)^2)));
    elseif lower(string(model)) == "emp"
        plin = 0.1164*id.^2;
    elseif lower(string(model)) == "emp2"
        load('conduction_25deg.mat')
        vdslin = interp2(vgg_lut,id_lut,vdslin_lut,vgg,id)';
        plin = id.*vdslin;
    else
        error('Invalid model for linear region power!')
    end
end
```

```
function psat = psat_dir(vbus,vgg,mos,model)
%PSAT_DIR Direct loss model for saturation region (VCCS)
    if lower(string(model)) == "sh"
        psat = vbus.*0.5*mos.k_sat.*(vgg - mos.Vt_sat).^2;
    else
        error('Invalid model for saturation power!')
    end
end
```

```
function esw = esw_dir(id,vbus,vggh,vggl,rgh,rgl,mos,model)
%ESW_DIR Direct loss model for the switching phase
    if lower(string(model)) == "sh"
        % Approximated SH equations... not so good!
        Vm = miller_volt(id,mos,'sh');
        Ecr =  1/3*rgh*mos.Cgs.*id.*vbus.*log((vggh-mos.Vt_lin)./(vggh-Vm));
        Evf =  1/2*rgh*mos.Cgd.*id.*vbus.^2./(vggh-Vm);
        Evr = -1/2*rgl*mos.Cgd.*id.*vbus.^2./(vggl-Vm);
        Ecf = -1/3*rgl*mos.Cgs.*id.*vbus.*log((mos.Vt_lin-vggl)./(Vm-vggl));
        esw = sum([Ecr Evf Evr Ecf]);
    elseif lower(string(model)) == "emp"
        % Empirical model with polynomial fitting
        eon = 3.049e-07*id.^2 + 1.206e-05*id + 3.575e-05;
        eoff = -6.62e-10*id.^4 + 3.602e-08*id.^3 + -3.794e-07*id.^2 + 1.221e-06*id + 1.683
             e-05;
        esw = eon + eoff;
    elseif lower(string(model)) == "emp2"
        load('mos_model_switching_fit.mat')
        esw = 5e-7*(eon_fit(rgh,vggh) + eoff_fit(rgl,vggl)).*id.^2/400;
    elseif lower(string(model)) == "emp3"
        load('energy_sw_4d_25deg.mat')
        esw = interp3(vgg_lut,id_lut,rg_lut,eon_lut,vggh,id,rgh) + ...
            interp3(vgg_lut,id_lut,rg_lut,eoff_lut,vggh,id,rgl);
    else
        error('Invalid model for switching loss energy!')
    end
end
```

```
function [vgg,rg,pmax,pmin,pout,ptest] = atcp_mpc(pset,id,vbus,dutycon,r,fpwm,mos,driver)
%ATCP_MPC Model predictive control for the concordant device VR-ATC
    % Initialization
    Vm = miller_volt(id,mos,'sh');
    n_pt = length(id);
    n_Vgg = length(driver.Vgg_steps);
    n_Rg = length(driver.Rg_steps);
    n_states = n_Vgg*n_Rg;
    states = zeros(n_Vgg*n_Rg,2);
    for vv=1:n_Vgg
        for rr=1:n_Rg
            states((vv-1)*n_Rg + rr,:) = [driver.Vgg_steps(vv), driver.Rg_steps(rr)];
        end
    end
    % Prediction for all states
```

```
    init0m = zeros(n_states,n_pt);
    valid = init0m;
    Plin = init0m;
    Psw = init0m;
    for ii=1:n_states
        vgg = states(ii,1);
        rg = states(ii,2);
        valid(ii,:) = 1.1*Vm < vgg;
        Plin(ii,:) = dutycon.*plin_dir(id,vgg,mos,'emp2');
        Psw(ii,:) = fpwm*esw_dir(id,vbus,vgg,driver.Vgg_min,rg,rg,mos,'emp3');
    end
    Plin = Plin.*valid;
    Psw = Psw.*valid;
    Pon = Plin + Psw;
    pmax = max(Pon,[],1);
    ptest = Pon(:,round((n_pt-1)/2));
    Pon = Pon + 1e9*~valid;
    pmin = min(Pon,[],1);
    % "Immediate" cost function
    cost = (Pon-pset).^2;
    % MPC selection based on minimization of cost function
    [~, idx] = min(cost,[],1);
    % Prepare output
    pout = Pon(sub2ind(size(Pon),idx,1:n_pt));
    vgg = states(idx,1);
    rg = states(idx,2);
end
```

B.2 ATC simulation

```
function [out_hc, out_ld] = hilo2condis(hicon,lodis,conh)
%HILO2CONDIS Hihg- and low-side device commands to concordant/discordant
    out_hc = hicon.*conh + lodis.*~conh;
    out_ld = hicon.*~conh + lodis.*conh;
end
```

```
%% Generation of gate signals for different ATCs, for the SPICE simulation

%% General cleaning and formatting
clear
clc
```

```
format short

%% System parameters
F_s          = 100e6;    % Traces sampling frequency
F_pwm        = 10e3;     % PWM frequency
Dead_time    = 200e-9;   % PWM dead time
F_mod        = 50;       % Modulation signal frequency
T_stop       = 30e-3;    % Observed time
V_bus        = 600;      % DC link voltage
% Angle in degrees. Use from [0 30 -30 120] to see R,L,C,regenL loads.
Phi          = 1;        % Load current angle
Imax         = 35;       % Load current peak value
P_set        = 90;       % Power set-point for ATC
Ldc          = 0.5;      % Loss Distribution Coefficient
N_types      = 6;        % Types of different controls
Out_name     = 'spice_signals.wav'; % Traces file name
To_plot      = [1 5 6];
signal = 'sqr';
Imin = 24;
% Same order as experimental results (for comparison).
ctrl_names  = {...
    'Normal',...
    'FWD-ATC',...
    'VRD-ATC',...
    'SC-ATC',...
    'Max loss',...
    'VR-ATC',...
    };

%% Parts parameters
mos = struct(...
    'Vt_sat', 2.589 ,...
    'k_sat' , 1.941,...
    'Vt_lin', 1.1 ,...
    'k_lin' , 0.6891 ,...
    'Vt_mil', 2.474 ,...
    'k_mil' , 1.144 ,...
    'Vf_dio', 2.857 ,...
    'Rf_dio', 29.37e-3 ,...
    'Cgs'   , 1e-9 ,...
    'Cgd'   , 10e-12 ...
    );
driver = struct(...
    'Vgg_max'  , 20 ,...
```

```
    'Vgg_min'   , -5 ,...
    'Vgg_steps', linspace(10,20,8) ,...
    'Rg_steps' , [16 27 43] ,...
    'Tau_l'     , 30e-9 ...
    );
Vgg_cc = 6; %min(driver.Vgg_steps);

%% Main PWM signals generation
% Discretization and time
t_s = 1/F_s;
n_car = round(F_s/F_pwm); % number of samples per period
n_stop = round(T_stop*F_s);
n_car2 = round(n_car/2);
n_per = floor(n_stop/n_car); % number of periods
n_dt = floor(Dead_time*F_s);
ntaum = 100e-9*F_pwm;
t_per = linspace(0,T_stop,n_per+1);
t = linspace(0,T_stop,n_stop+1);

% Electrical quantities (period average)
if strcmp(signal, 'sin')
    idx_per = 0.95*sin(2*pi*F_mod*t_per);
    iload_per = Imax * sin(2*pi*F_mod*t_per - pi*Phi/180);
elseif strcmp(signal, 'sqr')
    sqr_wave = sign(sin(2*pi*F_mod*t_per));
    ksqr = Imin/Imax;
    idx_per = 0.95*0.5*(1+ksqr + (1-ksqr)*sqr_wave);
    iload_per = Imax*0.5*(1+ksqr + (1-ksqr)*sqr_wave);
end
dutyh_per = 0.5*(idx_per + 1);
dutyl_per = 1 - dutyh_per;
vout_id_per = 0.5*V_bus*idx_per;
vout_dt_per = vout_id_per - V_bus*Dead_time*F_pwm*sign(iload_per);

% Upsample period data to SPICE frequency
idx = interp1(t_per,idx_per,t,'previous');
dutyh = interp1(t_per,dutyh_per,t,'previous');
dutyl = interp1(t_per,dutyl_per,t,'previous');
% Fix problem with current waveform
% (stepped waveform preferred by LTSPICE)
iload_wav = interp1(t_per,iload_per,t,'previous');

% PWM generation (with dead time)
% Carrier
```

```
car = linspace(1,-1,n_car2+1);
car = [car(1:end-1) -car(1:end-1)];
car = repmat(car,1,n_per);
car = [car car(1)];
% Dead time insertion
h_dt2 = 2*Dead_time*F_pwm;
pwmh = idx > car+h_dt2;
pwml = idx < car-h_dt2;

% Electric quantities (SPICE domain)
iload = Imax * sin(2*pi*F_mod*t - pi*Phi/180);
vout = 0.5*V_bus*(pwmh - pwml) - 0.5*V_bus*(~pwmh & ~pwml).*sign(iload);
vout_avg = movavgnc(vout, n_car);

%% Find concordant & discordant devices
% Conventional sign of bridge current positive if sourcing (going out) from
% from output node.
conh_per = iload_per > 0;
conh = interp1(t_per,double(conh_per),t,'previous');
conh = conh > 0;
% Produce quantities for concordant & discordant devices
[dutyc, dutyd] = hilo2condis(dutyh,dutyl,conh);
[dutyc_per, dutyd_per] = hilo2condis(dutyh_per,dutyl_per,conh_per);
[pwmc, pwmd] = hilo2condis(pwmh,pwml,conh);
[iloadc_per, iloadd_per] = hilo2condis(iload_per,-iload_per,conh_per);
[iloadc, iloadd] = hilo2condis(iload,-iload,conh);

%% Multilevel patterns
per_cnt = mod(0:n_per,2);
per_cnt = interp1(t_per,per_cnt,t,'previous');

%% Devices control and modulation
% Sizing of vectors
init0 = zeros(1,n_stop+1);
init1 = ones(1,n_stop+1);
init0m = zeros(N_types,n_stop+1);
railhc = init0m;
raillc = init0m;
railhd = init0m;
railld = init0m;
rgc = init0m;
rgd = init0m;
cmdc = init0m;
cmdd = init0m;
```

```
138
139 % Normal: no ATC, MOS reverse conduction (dead-time inserted)
140 railhc(1,:) = driver.Vgg_max*init1;
141 raillc(1,:) = driver.Vgg_min*init1;
142 railhd(1,:) = driver.Vgg_max*init1;
143 railld(1,:) = driver.Vgg_min*init1;
144 rgc(1,:) = min(driver.Rg_steps)*init1;
145 rgd(1,:) = min(driver.Rg_steps)*init1;
146 cmdc(1,:) = pwmc;
147 cmdd(1,:) = pwmd;
148
149 % FWD-ATC: ATC by diode reverse conduction (no dead-time)
150 railhc(2,:) = railhc(1,:);
151 raillc(2,:) = raillc(1,:);
152 railhd(2,:) = driver.Vgg_min*init1;
153 railld(2,:) = railld(1,:);
154 rgc(2,:) = min(driver.Rg_steps)*init1;
155 rgd(2,:) = min(driver.Rg_steps)*init1;
156 cmdc(2,:) = pwmc;
157 cmdd(2,:) = init0; % here is where MOS is kept off
158
159 % VRD-ATC: voltage-resistance-diode ATC, discrete levels, MPC
160 % Control
161 [vgg_mpc, rg_mpc, pmax, pmin, pout, ptest] = ...
162     atcp_mpc(P_set,iloadc_per,V_bus,dutyc_per,Ldc,F_pwm,mos,driver);
163 % Modulation
164 railhc(3,:) = interp1(t_per,vgg_mpc,t,'previous');
165 raillc(3,:) = raillc(2,:);
166 railhd(3,:) = railhd(2,:);
167 railld(3,:) = railld(2,:);
168 rgc(3,:) = interp1(t_per,rg_mpc,t,'previous');
169 rgd(3,:) = min(driver.Rg_steps)*init1;
170 cmdc(3,:) = pwmc;
171 cmdd(3,:) = pwmd;
172
173 % AT7: ATC with partial shoot-through in time for both devices
174 % Control
175 P_mosrev = dutyd_per.*plin_dir(iloadd_per,driver.Vgg_max,mos,'emp');
176 cc_per = (P_set - P_mosrev)/psat_dir(V_bus,Vgg_cc,mos,'sh');
177 % cc_per = cc_per./(1 - (1-exp(-cc_per/ntaum))*ntaum./cc_per);
178 for ii=1:length(t_per)
179     fun = @(x) (1 - ntaum/x*(1-exp(-x/ntaum))) - cc_per(ii)/x;
180     cc_per(ii) = fzero(fun,3*cc_per(ii));
181 end
```

```
cc_per = min(cc_per,dutyd_per);
cc = interp1(t_per,cc_per,t,'previous');
sth = car > 1-2*cc;
stl = car < 2*cc-1;
[~, std] = hilo2condis(sth,stl,conh);
% Concordant device is used with GD set at best efficiency. ST is used to
% achieve complete ATC for its better linearity and stability (what about
% thermal runaway?!?)
P_on = ...
    dutyc_per.*plin_dir(iloadc_per,driver.Vgg_max,mos,'emp') + ...
    F_pwm*esw_dir(iloadc_per,V_bus,1,1,1,1,mos,'emp');
cc_per = (P_set - P_on)/psat_dir(V_bus,Vgg_cc,mos,'sh');
% cc_per = cc_per./(1 - (1-exp(-cc_per/ntaum))*ntaum./cc_per);
for ii=1:length(t_per)
    fun = @(x) (1 - ntaum/x*(1-exp(-x/ntaum))) - cc_per(ii)/x;
    cc_per(ii) = fzero(fun,3*cc_per(ii));
end
cc_per = min(cc_per,dutyc_per);
cc = interp1(t_per,cc_per,t,'previous');
sth = car > 1-2*cc;
stl = car < 2*cc-1;
[stc, ~] = hilo2condis(sth,stl,conh);
% Modulation
railhc(4,:) = railhc(1,:);
raillc(4,:) = raillc(1,:);
railhd(4,:) = railhd(1,:);
railld(4,:) = railld(1,:);
rgc(4,:) = min(driver.Rg_steps)*init1;
rgd(4,:) = min(driver.Rg_steps)*init1;
cmdc(4,:) = pwmc + Vgg_cc./railhc(4,:).*stc;
cmdd(4,:) = pwmd + Vgg_cc./railhd(4,:).*std;

% Max heat: worst gate condition in normal driving
% Modulation
railhc(5,:) = min(driver.Vgg_steps)*init1;
raillc(5,:) = raillc(1,:);
railhd(5,:) = railhd(1,:);
railld(5,:) = railld(1,:);
rgc(5,:) = max(driver.Rg_steps)*init1;
rgd(5,:) = min(driver.Rg_steps)*init1;
cmdc(5,:) = pwmc;
cmdd(5,:) = pwmd;

% VR-ATC: voltage-resistance ATC, discrete levels, MPC
```

```
% Modulation
railhc(6,:) = railhc(3,:);
raillc(6,:) = raillc(3,:);
railhd(6,:) = railhd(1,:);
railld(6,:) = railld(1,:);
rgc(6,:) = rgc(3,:);
rgd(6,:) = rgd(1,:);
cmdc(6,:) = pwmc;
cmdd(6,:) = pwmd;

%% Conversion of concordant/discordant waveforms to high and low ones
vggc = railhc.*cmdc + raillc.*~cmdc;
vggd = railhd.*cmdd + railld.*~cmdd;
vggh = vggc.*conh + vggd.*~conh;
vggl = vggc.*~conh + vggd.*conh;
rgh = rgc.*conh + rgd.*~conh;
rgl = rgc.*~conh + rgd.*conh;

%% Normalization and WAV file generation
knorm = [0.5*V_bus; Imax; max(driver.Vgg_steps); max(driver.Rg_steps)];
traces = zeros(4*N_types+2,n_stop+1);
traces(1,:) = vout_avg  ./knorm(1);
traces(2,:) = iload_wav ./knorm(2);
for ii=1:N_types
    traces(4*ii-1,:) = vggh(ii,:)./knorm(3);
    traces(4*ii  ,:) = vggl(ii,:)./knorm(3);
    traces(4*ii+1,:) = rgh(ii,:) ./knorm(4);
    traces(4*ii+2,:) = rgl(ii,:) ./knorm(4);
end
traces = traces';
audiowrite(Out_name,traces,F_s);
```

```
%% Post-processing of data coming from the SPICE simulation

%% Cleaning
clc

%% Parameters
Nper_mean = 1;
T_view = 20e-3;
T_ds = 5e-3;
T_df = T_ds + T_view;
disp_used = To_plot;
tau = 10e-6;
```

```
flt = (t >= T_ds) & (t <= T_df);
log_name = 'atc_soft_device.txt';

%% Import SPICE waveforms
% Analyze traces file to find limits
fprintf('Scanning log file...\n');
fid = fopen(log_name);
iiline = 0;
jj = 0;
tline = fgets(fid);
iiline = iiline+1;
while ischar(tline)
    if length(tline) >= 4
        if tline(1:4) == 'time'
            name = tline;
        elseif tline(1:4) == 'Step'
            if jj > 0
                stop(jj) = iiline-1;
            end
            jj = jj+1;
            start(jj) = iiline+1;
            step{jj} = tline;
        end
    end
    tline = fgets(fid);
    iiline = iiline+1;
end
stop(jj) = iiline-1;
fclose(fid);

% Effectively import data
n_steps = length(start);
for ii=1:n_steps
    fprintf('Importing step %d/%d...\n', ii,n_steps);
    fid = fopen(log_name);
    C{ii} = textscan(fid,'%f %f %f',stop(ii)-start(ii)+1,'HeaderLines',start(ii)-1);
    fclose(fid);
end

% Convert data to timeseries format
praw = cell(1,n_steps);
presamp = cell(1,n_steps);
pmean = cell(1,n_steps);
pfilt = cell(1,n_steps);
```

```
pview = cell(1,n_steps);
for ii=1:n_steps
    for jj=1:2
        praw{jj,ii} = timeseries(C{ii}{1,jj+1},C{ii}{1,1});
        fprintf('Processing trace %d/%d...\n',(ii-1)*2+jj,2*n_steps);
        presamp{jj,ii} = resample(praw{jj,ii}, t);
        pmean{jj,ii} = filter(presamp{jj,ii}, 1/(Nper_mean*n_car)*ones(1,Nper_mean*n_car),
              1);
        % 1st-order filter
        pfilt{jj,ii} = filter(pmean{jj,ii},t_s,[(t_s+tau) -tau]);
        pfilt{jj,ii} = getsampleusingtime(pfilt{jj,ii},T_ds,T_df);
        pfilt{jj,ii}.Time = 1e3*(t(t <= T_view) - T_view/2);
        pfilt{jj,ii}.TimeInfo.Units = 'milliseconds';
        % PWM period filter
        pview{jj,ii} = getsampleusingtime(pmean{jj,ii},T_ds,T_df);
        pview{jj,ii}.Time = 1e3*(t(t <= T_view) - T_view/2);
        pview{jj,ii}.TimeInfo.Units = 'milliseconds';
    end
end

%% Superimposed comparison of power over time
fig = figure;
hold on
for ii = 1:n_steps
    plot(pfilt{2,ii},'LineWidth',1.5)
end
% legend(ctrl_names{disp_used(1:n_steps)},'Location','northeastoutside')
legend({'no ATC, Vgs max','no ATC, Vgs min','ATC'},'FontSize',12,'Location','north')
axis([-10 10 0 300])
xlabel('Time (ms)')
ylabel('Power loss (average) (W)')
ax = gca;
ax.Box = 'on';
ax.FontSize = 16;
ax.XTick = [-10 -5 0 5 10];
grid on
fig.Units = 'centimeters';
fig.Position = [8 4 18 12];
print('atc_pattern_high','-depsc')

%% Metrics
clear std
std_l = zeros(1,n_steps);
avg_l = zeros(1,n_steps);
```

```
avg_h = zeros(1,n_steps);
std_h = zeros(1,n_steps);
for ii=1:n_steps
    avg_l(ii) = mean(pview{1,ii});
    std_l(ii) = std(pview{1,ii});
    avg_h(ii) = mean(pview{2,ii});
    std_h(ii) = std(pview{2,ii});
end
fom_l = std_l./avg_l
fom_h = std_h./avg_h
```

B.3 Experimental data post-processing

```
%% Post-processing of experimental data

%% General cleaning
clear
clc

%% System parameters and (analytical) starting values
run_names = {...
    'BL2_600V_17ohm_vg20_rg27.csv' ...
    'BL1_600V_17ohm_vg20_rg27_comp.csv' ...
    'AT1_600V_17ohm_vg20_rg27_atcfull_revd.csv' ...
    'AT3_600V_17ohm_10_zen15_cold.csv' ...
    'AT3_600V_17ohm_15_zen15_hot.csv' ...
    };

run_num = length(run_names);
F_pwm0 = 10e3; % FW theoretical PWM frequency
F_load0 = 50; % FW theoretical modulation frequency
TAU_on_circ = 10e-6; % response of Vds,on sensing circuit
N_denoise = 10; % number of samples for denoising filtering
N_diode = 80;

%% Saved data for each test run and complete table
ATC_info = struct(...
    'Control'    , 'aaa', ...
    'Vbus'       , 0, ...
    'BusRipplePP', 0, ...
    'Vout'       , 0, ...
    'Iout'       , 0, ...
```

```
    'Pout'       , 0, ...
    'PhiDeg'     , 0, ...
    'Rdson'      , 0, ...
    'Rload'      , 0, ...
    'Lload'      , 0, ...
    'ONloss'     , 0, ...
    'SWloss'     , 0, ...
    'eta'        , 0, ...
    'LossAVG'    , 0, ...
    'LossSTD'    , 0, ...
    'ATCfom'     , 0);
ATC_results = repmat(struct2table(ATC_info),run_num,1);
power_per = zeros(200,run_num);
rds_per = power_per;
vd_per = power_per;

%% Main processing
for ii = 1:run_num
    %% Collect and rename data
    fprintf('Loading run %d/%d...\n',ii,run_num)
    % Import data from scope log file
    test = load_data_tex(run_names{ii});
    ATC_info.Control = run_names{ii}(1:3);
    fprintf('Processing run %d/%d...\n',ii,run_num)
    % Time needs to be resampled because Tek data is not evenly spaced in the
    % log file (?!?)
    t = linspace(min(test.TIME),max(test.TIME),length(test.TIME))';
    vdsh  = test.CH1;
    id    = test.CH2;
    iload = test.CH3;
    vdsl  = test.CH4;
    clear test
    dt = t(2)-t(1); % time resolution
    Np = round(1/F_pwm0/dt); % samples in PWM period
    Nper = round(length(t)/Np); % number of periods

    %% Skim through traces to determine variable thresholds
    % Vds "high" and "low" values
    % Multimodal distribution, since a whole period is observed, but
    % possible discontinuous mode when diode conduction is used, with
    % central node value appearing on output and device drain.
    dist_vdsh = fitgmdist(vdsh,3);
    [vdsh_low, low_idx] = min(dist_vdsh.mu);
    [vdsh_high, high_idx] = max(dist_vdsh.mu);
```

```
74  idxs = 1:3;
75  cnt_idx = idxs(idxs ~= low_idx & idxs ~= high_idx);
76  vdsh_center_min = icdf('Normal',0.01,dist_vdsh.mu(cnt_idx),sqrt(dist_vdsh.Sigma(
        cnt_idx)));
77  if (vdsh_center_min < vdsh_low)
78      vdsh_center_min = 0.5*(vdsh_high + vdsh_low);
79  end
80  vdsh_center_max = icdf('Normal',0.99,dist_vdsh.mu(cnt_idx),sqrt(dist_vdsh.Sigma(
        cnt_idx)));
81  if (vdsh_center_max > vdsh_high)
82      vdsh_center_max = 0.5*(vdsh_high + vdsh_low);
83  end
84  vds_low_max = icdf('Normal',0.999,dist_vdsh.mu(low_idx),sqrt(dist_vdsh.Sigma(low_idx))
        );
85  % Some denoising to have more robust thresholding
86  vdsh_denoise = filtfilt((1/N_denoise)*ones(1,N_denoise),1,vdsh);
87  id_denoise = filtfilt((1/N_denoise)*ones(1,N_denoise),1,id);
88  % PWM reconstruction (approximate) related to output, FWD contribute!
89  dev_pwm = vdsh < vdsh_center_min;
90  dev_bus = vdsh > vdsh_center_max;
91
92  %% Qualify ripple to fine-tune thresholds
93  fitt_cos_off = fittype(...
94      'ampl*cos(2*pi*freq*t + phi)+off',...
95      'coefficients',{'ampl','freq','phi','off'},...
96      'dependent','x',...
97      'independent','t');
98  fito_vb = fitoptions(...
99      'Method', 'NonlinearLeastSquares',...
100     'Lower',      [          0, 1.8*F_load0, -pi, 0.5*vdsh_high],...
101     'Upper',      [vdsh_high/3, 2.2*F_load0,  pi, 1.5*vdsh_high],...
102     'StartPoint', [          1, 2.0*F_load0,   0,     vdsh_high]);
103 vbfit = fit(t(dev_bus),vdsh_denoise(dev_bus),fitt_cos_off,fito_vb);
104 ATC_info.Vbus = vbfit.off;
105 ATC_info.BusRipplePP = 2*vbfit.ampl;
106 vbus = vbfit(t);
107 % Dynamic threshold for device off voltage
108 vds_off_ths = 0.95*vbus;
109
110 %% Fit load current and voltage to sinusoid
111 fito_ifit = fitoptions(...
112     'Method','NonlinearLeastSquares',...
113     'Lower', [0, 0, -pi, -Inf],...
114     'Upper', [Inf, Inf, pi, Inf],...
```

```
        'StartPoint', [0.5*(max(iload)-min(iload)), F_load0, 0, 0]);
    ifit = fit(t,iload,fitt_cos_off,fito_ifit);
    fito_vfit = fitoptions(...
        'Method','NonlinearLeastSquares',...
        'Lower', [0, ifit.freq, -pi, -Inf],...
        'Upper', [Inf, ifit.freq, pi, Inf],...
        'StartPoint', [0.5*(vdsh_high-vdsh_low), ifit.freq, 0, mean(vdsh)]);
    vfit = fit(t,vdsh,fitt_cos_off,fito_vfit);
    % Off-device typical current (depending on peak one)
    id_off_ths = 0.1; %0.02*ifit.ampl;

    %% Detect PWM pattern and device status
    % Device status flags
    dev_off = (abs(id_denoise) <= id_off_ths) & (vdsh_denoise > vds_off_ths);
    dev_on = (vdsh_denoise <= vds_low_max);
    pwm_rise = not(dev_pwm(1:end-1)) & dev_pwm(2:end);
    pwm_rise = [pwm_rise(1); pwm_rise]; % make same length as other vectors
    pwm_fall = dev_pwm(1:end-1) & not(dev_pwm(2:end));
    pwm_fall = [pwm_fall(1); pwm_fall];
    % T_pwm_rise and T_pwm_fall oscillating because of sinusoidal
    % modulation: difference between rise and fall period is proportional
    % to rate of change in duty cycle, thus follows time derivative of
    % modulation signal.
    T_pwm_rise = diff(t(pwm_rise));
    T_pwm_fall = diff(t(pwm_fall));
    T_pwm = 0.5*mean(T_pwm_rise + T_pwm_fall); % measured average PWM period
    F_pwm = 1/T_pwm; % measured average PWM frequency

    %% Determine Rdson
    N_on_circ = round(TAU_on_circ/dt); % samples in circuit delay
    vdsl_ok_start = circshift(pwm_rise,N_on_circ);
    vdsl_ok_stop = circshift(pwm_fall,-N_diode); % just some margin to avoid noise
    vdsl_ok_diff = vdsl_ok_start - vdsl_ok_stop;
    vdsl_ok = cumsum(vdsl_ok_diff);
    vdsl_ok_ths = mode(vdsl_ok);
    vdsl_ok = vdsl_ok - vdsl_ok_ths;
    % vdsl_ok is negative when stop precedes start -> no valid range
    vdsl_ok = vdsl_ok.*(vdsl_ok >= 0);
    vdsl_ok = logical(vdsl_ok);
    % Use pure resistance model, suitable for MOSFETs
    fitt_rds = fittype('poly1');
    fito_rds = fitoptions( 'Method', 'LinearLeastSquares' );
    fito_rds.Lower = [0 -5];
    fito_rds.Upper = [5 0];
```

```
    wind = [ones(Np,1); zeros(Np*(Nper-1),1)];
    wind = logical(wind);
    % First phase shift to sync with PWM
    nph_first = round(0.5*(find(pwm_rise,1)+find(pwm_fall,1)));
    wind =  circshift(wind,nph_first);
    % One fitting for each period, sync with PWM
    for jj = 1:Nper
        flt = logical(wind.*vdsl_ok);
        if sum(flt) >= 100
            rdsdyn_fit = fit(id_denoise(flt),vdsl(flt),fitt_rds,fito_rds);
            rds_per(jj,ii) = rdsdyn_fit.p1;
            vd_per(jj,ii) = rdsdyn_fit.p2;
        elseif jj == 1
            rds_per(jj,ii) = 0;
            vd_per(jj,ii) = 0;
        else
            rds_per(jj,ii) = rds_per(jj-1,ii);
            vd_per(jj,ii) = vd_per(jj-1,ii);
        end
        wind =  circshift(wind,Np);
    end
    ATC_info.Rdson = mean(rds_per(:,ii));

    %% Compute more accurate Vds
    % Reconstruct Vdson from Id and Rdson
    t_per = downsample(t,Np);
    rds = interp1(t_per,rds_per(:,ii),t,'previous','extrap');
    rds = circshift(rds,nph_first);
    vd = interp1(t_per,vd_per(:,ii),t,'previous','extrap');
    vd = circshift(vd,nph_first);
    vdsl_rds = vd + id_denoise.*rds;
    % Blend high and low Vds values (HDR)
    vds = vdsh.*not(dev_on) + vdsl_rds.*dev_on;

    %% Device power loss
    % Zero current when device is fully off
    id_nullified = id.*(abs(id_denoise) > id_off_ths);
    % Compute instantaneous power
    power = vds.*id_nullified;
    % Remove negative noise
    power = max(power,0);
    % Period average
    power_per(:,ii) = decimate(power,Np);
    % Global losses
```

```
    ATC_info.ONloss = mean(power.*dev_on);
    ATC_info.SWloss = mean(power.*not(dev_on));

    %% Load parameters (through fitting)
    vload_fit = vfit.ampl*cos(2*pi*vfit.freq.*t + vfit.phi);
    iload_fit = ifit.ampl*cos(2*pi*ifit.freq.*t + ifit.phi);
    power_load = vload_fit.*iload_fit;
    Phi = ifit.phi - vfit.phi;
    Cos_phi = cos(Phi);
    % Analytical power computation because average is not on exact period and
    % could lead to artifacts
    ATC_info.Vout   = vfit.ampl;
    ATC_info.Iout   = ifit.ampl;
    ATC_info.Pout   = 0.5*vfit.ampl*ifit.ampl*Cos_phi;
    ATC_info.PhiDeg = 180/pi*Phi;
    ATC_info.Rload  = vfit.ampl/ifit.ampl*Cos_phi;
    ATC_info.Lload  = vfit.ampl/ifit.ampl*sqrt(1-Cos_phi^2)/(2*pi*vfit.freq);
    % For conversion efficiency, remember there are two devices!
    ATC_info.eta    = ATC_info.Pout/(ATC_info.Pout + 2*(ATC_info.ONloss+ATC_info.SWloss));
    % Quantitative FOM for ATC
    ATC_info.LossAVG = mean(power_per(:,ii));
    ATC_info.LossSTD = std(power_per(:,ii));
    ATC_info.ATCfom = ATC_info.LossSTD/ATC_info.LossAVG;

    %% Save run data
    ATC_results(ii,:) = struct2table(ATC_info);

end

%% Power-time chart
fig = figure;
plot(t_per*1e3,power_per,'LineWidth',2)
legend({'Normal','FWD-ATC','VRD-ATC','SC-ATC (cold)','SC-ATC (hot)'},'FontSize',12,'
    Location','northeastoutside','Interpreter','none')
xlabel('Time (ms)')
ylabel('Power loss (average) (W)')
ax = gca;
ax.Box = 'on';
ax.FontSize = 16;
ax.XTick = [-10 -5 0 5 10];
grid on
fig.Units = 'centimeters';
fig.Position = [8 4 22 12];
print('atc_pattern_high','-depsc')
```

```
246
247 %% Experimental gate patterns
248 test = load_data_tex('AT3_600V_17ohm_15_zen15_cold_vgs.csv');
249 vgsl = test.CH2;
250 vgsh = test.CH3 - 1.5;
251 flt0 = -6e-3;
252 fltW = 1/F_pwm0;
253 flt = (t >= flt0-fltW) & (t < flt0+fltW);
254 fig = figure;
255 plot(t(flt)*1e3,vgsl(flt),t(flt)*1e3,vgsh(flt),'LineWidth',2)
256 legend({'v_{gs,low}','v_{gs,high}'},'FontSize',12,'Location','southeast','Interpreter','
      tex')
257 xlabel('Time (ms)')
258 ylabel('Gate-source voltage (V)')
259 ax = gca;
260 ax.Box = 'on';
261 ax.FontSize = 16;
262 ax.XTick = [-6.1 -6.05 -6 -5.95 -5.9];
263 grid on
264 fig.Units = 'centimeters';
265 fig.Position = [8 4 18 12];
266 print('gate_pattern_exp','-depsc')
```

Bibliography

[1] G. Constable and B. Somerville. *A Century of Innovation: Twenty Engineering Achievements that Transformed Our Lives*. Joseph Henry Press, 2003. URL: https://books.google.it/books?id=IyVFweSZu0cC.

[2] A. Anderson, P. Loomba, I. Orajaka, J. Numfor, S. Saha, S. Janko, N. Johnson, R. Podmore, and R. Larsen. Empowering Smart Communities: Electrification, Education, and Sustainable Entrepreneurship in IEEE Smart Village Initiatives. *IEEE Electrification Magazine*, 5(2):6–16, June 2017. doi:10.1109/MELE.2017.2685738.

[3] C. Crawford, A. Franca, J. J. W. Daniel Clancy, A. Ivanova, N. Tehrani, P. Amid, S. Behboodi, D. Chassin, and N. Djlali. Addressing key challenges in transportation mode electrification. In *2016 IEEE Canadian Conference on Electrical and Computer Engineering (CCECE)*, pages 1–4, May 2016. doi:10.1109/CCECE.2016.7726748.

[4] D. Tan. Transportation Electrification: Challenges and opportunities. *IEEE Power Electronics Magazine*, 3(2):50–52, June 2016. doi:10.1109/MPEL.2016.2551800.

[5] D. Bortis, D. Neumayr, and J. W. Kolar. np-Pareto optimization and comparative evaluation of inverter concepts considered for the GOOGLE Little Box Challenge. In *2016 IEEE 17th Workshop on Control and Modeling for Power Electronics (COMPEL)*, pages 1–5, June 2016. doi:10.1109/COMPEL.2016.7556767.

[6] J. W. Kolar, D. Bortis, and D. Neumayr. The ideal switch is not enough. In *2016 28th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, pages 15–22, June 2016. doi:10.1109/ISPSD.2016.7520767.

[7] Y. Lei, C. Barth, S. Qin, W. C. Liu, I. Moon, A. Stillwell, D. Chou, T. Foulkes, Z. Ye, Z. Liao, and R. C. N. Pilawa-Podgurski. A 2-kW Single-Phase Seven-Level Flying Capacitor Multilevel Inverter With an Active Energy Buffer. *IEEE Transactions on Power Electronics*, 32(11):8570–8581, November 2017. doi:10.1109/TPEL.2017.2650140.

[8] A. S. Morsy, M. Bayern, and P. Enjeti. High power density single phase inverter using GaN FETS and active power decoupling for Google little box challenge. In *2015 IEEE 3rd Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, pages 323–327, November 2015. doi:10.1109/WiPDA.2015.7369287.

[9] L. Zhang, R. Born, X. Zhao, and J. S. Lai. A high efficiency inverter design for Google little box challenge. In *2015 IEEE 3rd Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, pages 319–322, November 2015. doi:10.1109/WiPDA.2015.7369302.

[10] H. Kim, H. Chen, D. Maksimović, R. Erickson, Z. Cole, B. Passmore, and K. Olejniczak. SiC-MOSFET composite boost converter with 22 kW/L power density for electric vehicle application. In *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, pages 134–141, March 2017. doi:10.1109/APEC.2017.7930684.

[11] I. Krastev, P. Tricoli, S. Hillmansen, and M. Chen. Future of Electric Railways: Advanced Electrification Systems with Static Converters for ac Railways. *IEEE Electrification Magazine*, 4(3):6–14, September 2016. doi:10.1109/MELE.2016.2584998.

[12] G. Sulligoi, A. Vicenzutti, and R. Menis. All-Electric Ship Design: From Electrical Propulsion to Integrated Electrical and Electronic Power Systems. *IEEE Transactions on Transportation Electrification*, 2(4):507–521, December 2016. doi:10.1109/TTE.2016.2598078.

[13] P. Wheeler and S. Bozhko. The More Electric Aircraft: Technology and challenges. *IEEE Electrification Magazine*, 2(4):6–12, December 2014. doi:10.1109/MELE.2014.2360720.

[14] J. Millán and P. Godignon. Wide Band Gap power semiconductor devices. In *2013 Spanish Conference on Electron Devices*, pages 293–296, February 2013. doi:10.1109/CDE.2013.6481400.

[15] C. Bailey, P. Rajaguru, and H. Lu. Impact of wide band gap devices on power electronics packaging designs. In *2017 Pan Pacific Microelectronics Symposium (Pan Pacific)*, pages 1–6, February 2017.

[16] Y. Liu, C. Farnell, S. Ahmed, J. C. Balda, and H. A. Mantooth. 750-kW interleaved buck converter dc supply control implementation in a low-cost FPGA. In *2015 IEEE Applied Power Electronics Conference and Exposition (APEC)*, pages 2852–2858, March 2015. doi:10.1109/APEC.2015.7104755.

[17] H. Amemiya. Analysis of drivers for single-ended push-pull stage. *IRE Transactions on Audio*, AU-3(5):162–167, September 1955. doi:10.1109/TAU.1955.1165441.

[18] J. R. Macdonald. Active-Error Feedback and Its Application to a Specific Driver Circuit. *Proceedings of the IRE*, 43(7):808–813, July 1955. doi:10.1109/JRPROC.1955.278145.

[19] R. L. Bright. Junction transistors used as switches. *Transactions of the American Institute of Electrical Engineers, Part I: Communication and Electronics*, 74(1):111–121, March 1955. doi:10.1109/TCE.1955.6372253.

[20] P. L. Hower, S. Pendharkar, and T. Efland. Current status and future trends in silicon power devices. In *2010 International Electron Devices Meeting*, pages 13.1.1–13.1.4, December 2010. doi:10.1109/IEDM.2010.5703352.

[21] P. A. Gargini. How to successfully overcome inflection points, or long live Moore's law. *Computing in Science Engineering*, 19(2):51–62, March 2017. doi:10.1109/MCSE.2017.32.

[22] P. Gammon. Silicon and the wide bandgap semiconductors, shaping the future power electronic device market. In *2013 14th International Conference on Ultimate Integration on Silicon (ULIS)*, pages 9–13, March 2013. doi:10.1109/ULIS.2013.6523479.

[23] Julius Edgar Lilienfeld. Device for controlling electric current, March 1933. URL: https://www.google.com/patents/US1900018.

[24] R. K. Williams, M. N. Darwish, R. A. Blanchard, R. Siemieniec, P. Rutter, and Y. Kawaguchi. The Trench Power MOSFET: Part I - History, Technology, and Prospects. *IEEE Transactions on Electron Devices*, 64(3):674–691, March 2017. doi:10.1109/TED.2017.2653239.

[25] T. Fujihira and Y. Miyasaka. Simulated superior performances of semiconductor superjunction devices. In *Power Semiconductor Devices and ICs, 1998. ISPSD 98. Proceedings of the 10th International Symposium on*, pages 423–426, June 1998. doi:10.1109/ISPSD.1998.702736.

[26] L. Lorenz, G. Deboy, A. Knapp, and M. Marz. COOLMOS-a new milestone in high voltage power MOS. In *Power Semiconductor Devices and ICs, 1999. ISPSD '99. Proceedings., The 11th International Symposium on*, pages 3–10, 1999. doi:10.1109/ISPSD.1999.764028.

[27] R. Sodhi, R. Malik, D. Asselanis, and D. Kinzer. High-density ultra-low Rdson 30 volt N-channel trench FETs for DC/DC converter applications. In *Power*

Semiconductor Devices and ICs, 1999. ISPSD '99. Proceedings., The 11th International Symposium on, pages 307–310, 1999. doi:10.1109/ISPSD.1999.764123.

[28] J. Lutz, H. Schlangenotto, U. Scheuermann, and R. De Doncker. *Semiconductor Power Devices: Physics, Characteristics, Reliability*. Springer Berlin Heidelberg, 2011. URL: https://books.google.it/books?id=345uBEHneEgC.

[29] T. Krone, C. Xu, and A. Mertens. Fast and Easily Implementable Detection Circuits for Short Circuits of Power Semiconductors. *IEEE Transactions on Industry Applications*, 53(3):2871–2879, May 2017. doi:10.1109/TIA.2016.2618785.

[30] M. Pfost, C. Unger, G. Cretu, M. Cenusa, K. Büyüktas, and U. Wahl. Short-circuit safe operating area of superjunction MOSFETs. In *2016 28th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, pages 335–338, June 2016. doi:10.1109/ISPSD.2016.7520846.

[31] J. Sun, H. Xu, X. Wu, and K. Sheng. Comparison and analysis of short circuit capability of 1200v single-chip SiC MOSFET and Si IGBT. In *2016 13th China International Forum on Solid State Lighting: International Forum on Wide Bandgap Semiconductors China (SSLChina: IFWS)*, pages 42–45, November 2016. doi:10.1109/IFWS.2016.7803752.

[32] B.J. Baliga. *Modern power devices*. A Wiley-Interscience publication. Wiley, 1987. URL: https://books.google.it/books?id=5xxTAAAAMAAJ.

[33] H.W. Becke and C.F. Wheatley. Power MOSFET with an anode region, December 1982. URL: https://www.google.com/patents/US4364073.

[34] J. P. Russell, A. M. Goodman, L. A. Goodman, and J. M. Neilson. The COMFET: A new high conductance MOS-gated device. *IEEE Electron Device Letters*, 4(3):63–65, March 1983. doi:10.1109/EDL.1983.25649.

[35] B. J. Baliga. Analysis of insulated gate transistor turn-off characteristics. *IEEE Electron Device Letters*, 6(2):74–77, February 1985. doi:10.1109/EDL.1985.26048.

[36] Takahashi, Kaneda, and Minato. 1200v class reverse blocking IGBT (RB-IGBT) for AC matrix converter. In *2004 Proceedings of the 16th International Symposium on Power Semiconductor Devices and ICs*, pages 121–124, May 2004. doi:10.1109/WCT.2004.239841.

[37] H. Yilmaz, J. L. Benjamin, R. F. Dyer, L. S. S. Chen, W. R. Van Dell, and G. C. Pifer. Comparison of the Punch-Through and Non-Punch-Through IGT Structures. *IEEE Transactions on Industry Applications*, IA-22(3):466–470, May 1986. doi:10.1109/TIA.1986.4504744.

[38] B. J. Baliga. Power semiconductor device figure of merit for high-frequency applications. *IEEE Electron Device Letters*, 10(10):455–457, October 1989. doi:10.1109/55.43098.

[39] J. L. Hudgins, G. S. Simin, E. Santi, and M. A. Khan. An assessment of wide bandgap semiconductors for power devices. *IEEE Transactions on Power Electronics*, 18(3):907–914, May 2003. doi:10.1109/TPEL.2003.810840.

[40] H. G. Xing, B. Song, M. Zhu, Z. Hu, M. Qi, K. Nomoto, and D. Jena. Unique opportunity to harness polarization in GaN to override the conventional power electronics figure-of-merits. In *2015 73rd Annual Device Research Conference (DRC)*, pages 51–52, June 2015. doi:10.1109/DRC.2015.7175549.

[41] J. Fabre and P. Ladoux. Parallel Connection of 1200-V/100-A SiC-MOSFET Half-Bridge Modules. *IEEE Transactions on Industry Applications*, 52(2):1669–1676, March 2016. doi:10.1109/TIA.2015.2496109.

[42] S. Madhusoodhanan, K. Mainali, A. Tripathi, A. Kadavelugu, K. Vechalapu, D. Patel, and S. Bhattacharya. Comparative evaluation of 15 kV SiC IGBT and 15 kV SiC MOSFET for 3-phase medium voltage high power grid connected

converter applications. In *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, pages 1–8, September 2016. doi:10.1109/ECCE.2016.7854933.

[43] A. Terano, T. Tsuchiya, and K. Mochizuki. Characteristics of GaN-Based Bipolar Transistors on Sapphire Substrates With the n-Type Emitter Region Formed Using Si-Ion Implantation. *IEEE Transactions on Electron Devices*, 61(10):3411–3416, October 2014. doi:10.1109/TED.2014.2346778.

[44] R. Gaska, M. A. Khan, X. Hu, G. Simin, J. Yang, J. Deng, S. Rumyantsev, and M. S. Shur. GaN-based MESFETs and DC-MOSFETs. In *58th DRC. Device Research Conference. Conference Digest (Cat. No.00TH8526)*, pages 43–44, June 2000. doi:10.1109/DRC.2000.877081.

[45] M. A. Khan, X. Hu, G. Sumin, A. Lunev, J. Yang, R. Gaska, and M. S. Shur. AlGaN/GaN metal oxide semiconductor heterostructure field effect transistor. *IEEE Electron Device Letters*, 21(2):63–65, February 2000. doi:10.1109/55.821668.

[46] Haruka Shimizu, Satoru Akiyama, Natsuki Yokoyama, Akio Shima, and Yasuhiro Shimamoto. Static and switching characteristics of 3.3 kV double channel-doped SiC vertical junction field effect transistor in cascode configuration. *Japanese Journal of Applied Physics*, 54(4S):04DP15, 2015. URL: http://stacks.iop.org/1347-4065/54/i=4S/a=04DP15.

[47] Ned Mohan and Tore M Undeland. *Power electronics: converters, applications, and design*. John Wiley & Sons, 2007.

[48] Hongrae Kim, T.M. Jahns, and G. Venkataramanan. Minimization of reverse recovery effects in hard-switched inverters using CoolMOS power switches. In *Industry Applications Conference, 2001. Thirty-Sixth IAS Annual Meeting. Conference Record of the 2001 IEEE*, volume 1, pages 641–647 vol.1, September 2001. doi:10.1109/IAS.2001.955487.

[49] Sungwoo Lee, Seungchul Jung, Jin Huh, Changbyung Park, Chun-Taek Rim, and Gyu-Hyeong Cho. Robust and efficient synchronous buck converter with near-optimal dead-time control. In *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2011 IEEE International*, pages 392–394, February 2011. doi:10.1109/ISSCC.2011.5746366.

[50] Cree Inc. *CAS120M12BM2 module datasheet*. 2014.

[51] ST Microelectronics. *ST13007 BJT datasheet*. 2009.

[52] ST Microelectronics. *STGW60V60DF IGBT datasheet*. 2013.

[53] A. Soldati, D. Barater, F. Brugnano, and C. Concari. Design of a control unit for advanced gate drivers featuring adaptive dead-time and diagnostics. In *IECON 2015 - 41st Annual Conference of the IEEE Industrial Electronics Society*, pages 002485–002490, November 2015. doi:10.1109/IECON.2015.7392476.

[54] N. Idir, R. Bausiere, and J. J. Franchaud. Active gate voltage control of turn-on di/dt and turn-off dv/dt in insulated gate transistors. *IEEE Transactions on Power Electronics*, 21(4):849–855, July 2006. doi:10.1109/TPEL.2007.876895.

[55] Shihong Park and T. M. Jahns. Flexible dv/dt and di/dt control method for insulated gate power switches. *IEEE Transactions on Industry Applications*, 39(3):657–664, 2003. doi:10.1109/TIA.2003.810654.

[56] Fairchild Semiconductor. *FDC6333C matched MOSFETs datasheet*. 2001.

[57] Y. Lobsiger, J.W. Kolar, and M. Laitinen. Active gate drive circuit, July 2013. URL: https://www.google.it/patents/EP2615737A1?cl=en.

[58] A. Kadavelugu, S. Bhattacharya, S. H. Ryu, D. Grider, S. Leslie, and K. Hatua. Understanding dv/dt of 15 kV SiC N-IGBT and its control using active gate driver. In *2014 IEEE Energy Conversion Congress and Exposition*

(ECCE), pages 2213–2220, September 2014. doi:10.1109/ECCE.2014.6953698.

[59] K. Onda, A. Konno, and J. Sakano. New concept high-voltage IGBT gate driver with self-adjusting active gate control function for SiC-SBD hybrid module. In *2013 25th International Symposium on Power Semiconductor Devices IC's (ISPSD)*, pages 343–346, 2013. doi:10.1109/ISPSD.2013.6694418.

[60] A. Soldati, D. Barater, C. Concari, and G. Franceschini. Comparing control topologies for wide-bandgap power-device drivers: A simulation study. In *IECON 2015 - 41st Annual Conference of the IEEE Industrial Electronics Society*, pages 002469–002474, November 2015. doi:10.1109/IECON.2015.7392473.

[61] Y. Lobsiger and J.W. Kolar. Closed-Loop di/dt and dv/dt control and dead time minimization of IGBTs in bridge leg configuration. In *Control and Modeling for Power Electronics (COMPEL), 2013 IEEE 14th Workshop on*, pages 1–7, June 2013. doi:10.1109/COMPEL.2013.6626392.

[62] Fairchild Semiconductor. *Active Miller Clamp Technology*. 2013.

[63] Y. Lobsiger and J.W. Kolar. Closed-Loop di/dt and dv/dt IGBT Gate Driver. *Power Electronics, IEEE Transactions on*, 30(6):3402–3417, June 2015. doi:10.1109/TPEL.2014.2332811.

[64] A. Ochoa. On stability in linear feedback circuits. In *Circuits and Systems, 1997. Proceedings of the 40th Midwest Symposium on*, volume 1, pages 51–55 vol.1, August 1997. doi:10.1109/MWSCAS.1997.666031.

[65] A.Jr. Ochoa. A systematic approach to the analysis of general and feedback circuits and systems using signal flow graphs and driving-point impedance. *Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on*, 45(2):187–195, February 1998. doi:10.1109/82.661648.

[66] A. Soldati, D. Barater, C. Concari, M. Galea, and C. Gerada. A voltage controlled power resistor circuit for active gate driving of wide-bandgap power devices. In *IECON 2015 - 41st Annual Conference of the IEEE Industrial Electronics Society*, pages 002445–002450, November 2015. doi:10.1109/IECON.2015.7392469.

[67] A. Soldati, G. Pietrini, D. Barater, and C. Concari. Stability and Performance Analysis of a Voltage Controlled Resistor Circuit for Wide Band-gap Device Gate Drivers. In *PCIM Europe 2016; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, pages 1–8, May 2016.

[68] D. Barater, F. Immovilli, A. Soldati, G. Buticchi, G. Franceschini, C. Gerada, and M. Galea. Multistress Characterization of Fault Mechanisms in Aerospace Electric Actuators. *IEEE Transactions on Industry Applications*, 53(2):1106–1115, March 2017. doi:10.1109/TIA.2016.2633948.

[69] D. Barater, G. Buticchi, A. Soldati, G. Franceschini, F. Immovilli, M. Galea, and C. Gerada. Multistress characterization of insulation aging mechanisms in aerospace electric actuators. In *2015 IEEE Energy Conversion Congress and Exposition (ECCE)*, pages 2215–2222, September 2015. doi:10.1109/ECCE.2015.7309972.

[70] D. Barater, A. Soldati, G. Pietrini, G. Franceschini, F. Immovilli, M. Galea, and C. Gerada. Test Setup for Multistress Characterization of Insulation Degradation Mechanisms in Electric Drives. In *PCIM Europe 2016; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, pages 1–8, May 2016.

[71] J. Millman and A. Grabel. *Microelectronics*. McGraw-Hill Series in Electrical Engineering. McGraw-Hill, 1987. URL: https://books.google.it/books?id=-yFTAAAAMAAJ.

[72] Hisham A H Al-Khazali and Mohamad R Askari. Geometrical and Graphical Representations Analysis of Lissajous Figures in Rotor Dynamic System. *IOSR Journal of Engineering*, 02, 2012.

[73] H. Shichman and D. A. Hodges. Modeling and simulation of insulated-gate field-effect transistor switching circuits. *IEEE Journal of Solid-State Circuits*, 3(3):285–289, September 1968. doi:10.1109/JSSC.1968.1049902.

[74] A. Soldati, F. Dossena, G. Pietrini, D. Barater, C. Concari, and F. Iannuzzo. Thermal stress mitigation by Active Thermal Control: Architectures, models and specific hardware. In *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, Cincinnati, OH, September 2017. (accepted).

[75] Krzysztof Ciesielski. On Stefan Banach and some of his results. *Banach J. Math. Anal*, 1:1–10, 2007.

[76] Mauro Ciappa. Selected failure mechanisms of modern power modules. *Microelectronics Reliability*, 42(4–5):653 – 667, 2002. doi:10.1016/S0026-2714(02)00042-2.

[77] M. Andresen, M. Liserre, and G. Buticchi. Review of active thermal and lifetime control techniques for power electronic modules. In *2014 16th European Conference on Power Electronics and Applications*, pages 1–10, August 2014. doi:10.1109/EPE.2014.6910822.

[78] C.M. Brown and D.J. Coombs. *Notes on Control with Delay*. Number No. 387 in Department of Computer Science: Technical report. University of Rochester, 1991. URL: https://books.google.it/books?id=hfWBtQAACAAJ.

[79] P. Hövel. *Control of Complex Nonlinear Systems with Delay*. Springer Theses. Springer Berlin Heidelberg, 2010. URL: https://books.google.it/books?id=2HqQY-5J5TIC.

[80] Otto Smith. A controller to overcome dead time. *ISA Journal*, 6:28–33, 1959. URL: http://ci.nii.ac.jp/naid/10003093722/en/.

[81] M.P. Polis, A. Dontchev, P. Kall, I. Lasiecka, and A.W. Olbrot. *Systems Modelling and Optimization Proceedings of the 18th IFIP TC7 Conference*. Chapman & Hall/CRC Research Notes in Mathematics Series. Taylor & Francis, 1999. URL: https://books.google.it/books?id=ds2eIQ6XZy0C.

[82] Johan Nilsson. Real-Time Control Systems with Delays. 1999.

[83] Leonid Mirkin and Zalman J. Palmor. Control Issues in Systems with Loop Delays. In Dimitrios Hristu-Varsakelis and William S. Levine, editors, *Handbook of Networked and Embedded Control Systems*, pages 627–648. Birkhäuser Boston, Boston, MA, 2005. DOI: 10.1007/0-8176-4404-0_27.

[84] P. K. Prasobhu, G. Buticchi, S. Brueske, and M. Liserre. Gate driver for the active thermal control of a DC/DC GaN-based converter. In *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, pages 1–8, September 2016. doi:10.1109/ECCE.2016.7855131.

[85] M. Andresen, G. Buticchi, J. Falck, M. Liserre, and O. Muehlfeld. Active thermal management for a single-phase H-Bridge inverter employing switching frequency control. In *PCIM Europe 2015; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management; Proceedings of*, pages 1–8, May 2015.

[86] H. Luo, F. Iannuzzo, K. Ma, F. Blaabjerg, W. Li, and X. He. Active gate driving method for reliability improvement of IGBTs via junction temperature swing reduction. In *2016 IEEE 7th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, pages 1–7, June 2016. doi:10.1109/PEDG.2016.7527079.

[87] D. A. Murdock, J. E. R. Torres, J. J. Connors, and R. D. Lorenz. Active thermal control of power electronic modules. *IEEE Transactions on Industry Applications*, 42(2):552–558, March 2006. doi:10.1109/TIA.2005.863905.

[88] J. Falck, G. Buticchi, and M. Liserre. Thermal Stress Based Model Predictive Control of Electric Drives. *IEEE Transactions on Industry Applications*, PP(99):1–1, 2017. doi:10.1109/TIA.2017.2772198.

[89] A. Soldati, F. Iannuzzo, C. Concari, D. Barater, and F. Blaabjerg. Active Thermal Control by Controlled Shoot-through of Power Devices. In *IECON 2017 - 43st Annual Conference of the IEEE Industrial Electronics Society*, Beijing, CN, October 2017. (accepted).

[90] J. Sun, H. Xu, X. Wu, S. Yang, Q. Guo, and K. Sheng. Short circuit capability and high temperature channel mobility of SiC MOSFETs. In *2017 29th International Symposium on Power Semiconductor Devices and IC's (ISPSD)*, pages 399–402, May 2017. doi:10.23919/ISPSD.2017.7988988.

[91] M. Trivedi and K. Shenai. Investigation of the short-circuit performance of an IGBT. *IEEE Transactions on Electron Devices*, 45(1):313–320, January 1998. doi:10.1109/16.658847.

[92] P. D. Reigosa, F. Iannuzzo, H. Luo, and F. Blaabjerg. A Short-Circuit Safe Operation Area Identification Criterion for SiC MOSFET Power Modules. *IEEE Transactions on Industry Applications*, 53(3):2880–2887, May 2017. doi:10.1109/TIA.2016.2628895.

[93] M. Held, P. Jacob, G. Nicoletti, P. Scacco, and M. H. Poech. Fast power cycling test of IGBT modules in traction application. In *Proceedings of Second International Conference on Power Electronics and Drive Systems*, volume 1, pages 425–430 vol.1, May 1997. doi:10.1109/PEDS.1997.618742.

[94] A. Soldati, F. Iannuzzo, C. Concari, F. Dossena, D. Barater, and F. Blaabjerg. Active Thermal Control for Reliability Improvement of MOS-gated Power Devices. In *IECON 2017 - 43st Annual Conference of the IEEE Industrial Electronics Society*, Beijing, CN, October 2017. (accepted).

[95] R. t Have, B. Vermulst, and J. v Duivenbode. An approach to lifetime estimation of SiC MOSFETs subjected to thermal stress. In *Proceedings of PCIM Europe*

2015; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, pages 1–9, May 2015.

[96] Arendt Wintrich, Ulrich Nicolai, Werner Tursky, and Tobias Reimann. *Application Manual Power Semiconductors*. ISLE, Ilmenau, 2nd, rev. ed edition, 2015.

[97] R. Bayerer, T. Herrmann, T. Licht, J. Lutz, and M. Feller. Model for Power Cycling lifetime of IGBT Modules - various factors influencing lifetime. In *5th International Conference on Integrated Power Electronics Systems*, pages 1–6, March 2008.

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