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Electrical Measurements and Numerical Simulations of Ion Implanted 4H-SiC PiN diodes

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To my family . . .

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Introduction

The fast growth of modern societies entails a quick development of electronic technologies with the aim to improve comfort, transportation and healthcare. These technological improvements require great advances in power distribution, power generation and power management technologies.

After the initial replacement of vacuum tubes by solid–state devices in the 1950s, the related electronic market grew up rapidly. Among all semiconductor, the preferred for industrial mass production of these devices was Silicon (Si). However, the steadily increasing request of devices with higher performances and with smaller dimensions have led the research efforts in studying new semiconductor materials suitable for the production of a new class of devices for high power electronic and high temperature applications. Thanks to the superior physical properties with respect to Silicon in terms of critical electric field and thermal conductivity values, Silicon Carbide (SiC) has attracted the attention of many researchers as a possible candidate for the fabrication of this new generation of devices with high performance and small dimensions.

Silicon Carbide is as old as Silicon, it was discovered more than likely by J. J. Berzelius in the far 1824. After the first synthesis of this compound material, which occured in the early 1890 by Ancheson, in 1907 its electronic properties were further investigated. The basic requirement for a mass industrial production is the growth of large wafers with electronic grade. Unfortunately, SiC have a complex structure, the Ancheson was a cumbersome process that required patience and often the purity of crystals was not controllable. For this reason, the interest in Silicon Carbide as an electronic material waned up to late 1970s when, thanks to the modified Lely pro-

cess, high quality 6H polytype large wafer were manufactured. After years of further developments CREE Research was the first company to sell a 2.5*cm* high quality 6H–SiC wafers and in the 1990s SiC devices entered the electronic market. Since the mid of 1990s the 4H became the favourite polytype for high power electronic device production for the higher mobility and higher band–gap with the respect to the 6H–SiC. As a result of the rapid progress in SiC wafers growth and device fabrication technologies in the last decade, SiC devices are commonly available in the electronic market to date.

In this thesis work 4H–SiC ion implanted PiN diodes are studied and characterised in detail. Electrical measurements (current–voltage curves and lifetime measurements) and Numerical simulations are performed with the aim to better understand physical phenomena which arises from the periphery of these diodes. This analysis is relevant as it is well known that perimeter currents affect performances of SiC devices. This thesis is structured as follows:

- Chapter 1 reports the material properties of the most used SiC polytype for electronic applications together with a brief historical background of growth processes of SiC wafers.

- Chapter 2 describes the ion implatation and post–implantation annealing processes for selective area doping of SiC material. Furthermore, the issue related to the ohmic contacts on SiC are also discussed. Finally, the processing steps of the studied devices are listed and their experimental forward and reverse curves are shown. In this chapter, the experimental set–up used for performing these latter measurements is described in detail.

- Chapter 3 describes the analysis methodologies for obtaining the experimental perimeter and area current density curves. The range of validity of the simple abrupt–junction model is also analysed before applying the method to experimental area and perimeter curves. From this detailed analysis, important information are extracted, in particular: defect activation energies responsible of current transport, the recombination lifetime within the Space Charge Region and information about the surface quality. Numerical simulations are per-

formed in order to study the origin of periphery currents. Simulations, which combines detailed experimental data analysis with appropriate literature results, are proposed and validated.

- Chapter 4 provides a brief explanation of generation and recombination lifetimes. The main lifetime measurement techniques used in the case of Silicon Carbide devices are reported with particular attention to the Open Circuit Voltage Decay (OCVD) which is the method used for this study. A detailed characterization of the experimental measurement set–up is shown and a schematic circuital model is provided. Comparison between experimental and theoretical calculations are performed in order to validate the proposed model. Finally, the experimental OCVD curves of diodes are shown and studied in detail and an explanation about the volume and surface lifetimes of these devices is provided.

Chapter 1

Single Crystal Silicon Carbide

1.1 Material Properties

Silicon Carbide (SiC) is a semiconductor which thanks to its physical properties is widely used for fabrication of devices for high temperature, high power and high frequency applications. The outstanding physical properties derive from its crystalline structure, the SiC is a IV–IV compound material with a tetrahedric structure in which Silicon atoms form almost covalent bondings with the near Carbon atoms (Fig. 1.1, [1]). The stacking sequence of this elementary cell gives origin to different SiC polytypes.

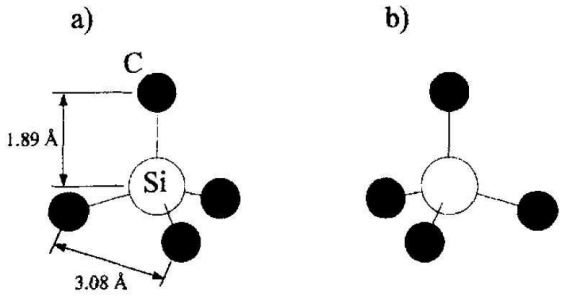


Figure 1.1: (a) Elementary structural unit of SiC material. (b) A second type rotated of 180° around the stacking direction, with respect to (a).

The strong chemical bondings together with a particular stacking sequence provide each polytype with unique electrical and optical properties. Even within a given polytype, some important electrical properties are non–isotropic, indeed they are a functions of crystallographic direction of current flow and applied electric field. Furthermore, SiC is able to form silicon dioxide (S_iO_2) as a native stable oxide, like Silicon, and this is an important advantage for device fabrication such as MOSFETs [2][3][4].

For use as an electronic semiconductor, among all SiC polytypes [5], the major efforts of research and development have been concentrated on 3C, 6H, and 4H polytypes [6]. 3C–SiC, also referred to as β–SiC, is the only form of SiC with a cubic crystal lattice structure. 4H–SiC and 6H–SiC are only two of many possible SiC polytypes with hexagonal crystal structure [7].

Fig. 1.2 reports the main physical properties of these three polytypes compared to those of the most employed material for electronic device fabrications, the Silicon.

Property	Silicon	GaAs	4H-SiC	6H-SiC	3C-SiC
Bandgap (eV)	1.1	1.42	3.2	3.0	2.3
Relative Dielectric Constant	11.9	13.1	9.7	9.7	9.7
Breakdown Field $N_D = 10^{17}$ cm^{-3} (MV/cm)	0.6	0.6	//c-axis: 3.0	// c-axis: 3.2 $\perp$c-axis: > 1	> 1.5
Thermal Conductivity (W/cm-K)	1.5	0.5	3 - 5	3 - 5	3 - 5
Intrinsic Carrier Concentration (cm^{-3})	10^{10}	1.8 x 10^{6}	~ 10^{-7}	~ 10^{-5}	~ 10
Electron Mobility @ $N_D = 10^{16}$ cm^{-3} (cm^2/V-s)	1200	6500	//c-axis: 800 $\perp$c-axis: 800	//c-axis: 60 $\perp$c-axis: 400	750
Hole Mobility @ $N_A = 10^{16}$ cm^{-3} (cm^2/V-s)	420	320	115	90	40
Saturated Electron Velocity (10^7 cm/s)	1.0	1.2	2	2	2.5
Donor Dopants & Shallowest Ionization Energy (meV)	P: 45 As: 54	Si: 5.8	N: 45 P: 80	N: 85 P: 80	N: 50
Acceptor Dopants & Shallowest Ionization Energy (meV)	B: 45	Be, Mg, C: 28	Al: 200 B: 300	Al: 200 B: 300	Al: 270
1998 Commercial Wafer Diameter (cm)	30	15	5	5	None

Figure 1.2: Table reporting the main physical properties of the most used SiC polytypes for electronic application.

More detailed electrical and optical properties can be found in [8][9].

SiC polytypes exhibit advantages and disadvantages if compared to Silicon. The most beneficial properties of SiC over Silicon are: higher breakdown electric field, wider band–gap energy, higher thermal conductivity and higher carrier saturation velocity (very important for high frequency applications). Compared to the others two politypes, 4H–SiC is nowadays the preferred for production of electronic devices, thanks to the superior band–gap and mobility values.

1.2 SiC Wafers

1.2.1 Early history

Most of Silicon Carbide's superior intrinsic electrical properties with respect to other semiconductor have been knowing for decades. Nevertheless, for commercial mass–production of semiconductor electronic devices, large high quality wafers are needed.

SiC sublimes instead of melting and therefore cannot be grown by conventional techniques such as Czochralski method employed in the manufacturing of almost all high–quality Silicon large wafers. This prevented the realization of SiC crystals suitable for electronic device mass–productions until the late 1980s.

Despite the absence of SiC substrates, the potential benefits of a SiC–based electronic, for realising devices working in harsh–environment, has led research efforts to obtain SiC manufacturable wafer.

In the late 1970s, Tairov and Tsvetkov invented a reproducible method for SiC ingots growth [10][11]. They introduced a 6H–SiC seed into a sublimation growth furnace and designed an appropriate temperature gradient to control mass transport from the SiC source onto the seed crystal, based on thermodynamic and kinetic considerations. This growth method is called modified Lely or seeded sublimation process (and also Physical Vapor Transport, PVT) and it was a breakthrough for SiC as it offered the first possibility of growing relatively high–quality large–area substrates of SiC that could be cut and polished into mass-produced SiC wafers.

After years of further development of the sublimation growth process [12], CREE Research became the first company to sell $2.5cm$–diameter semiconductor wafers of

6H-SiC in 1989 [13] (Fig. 1.3).

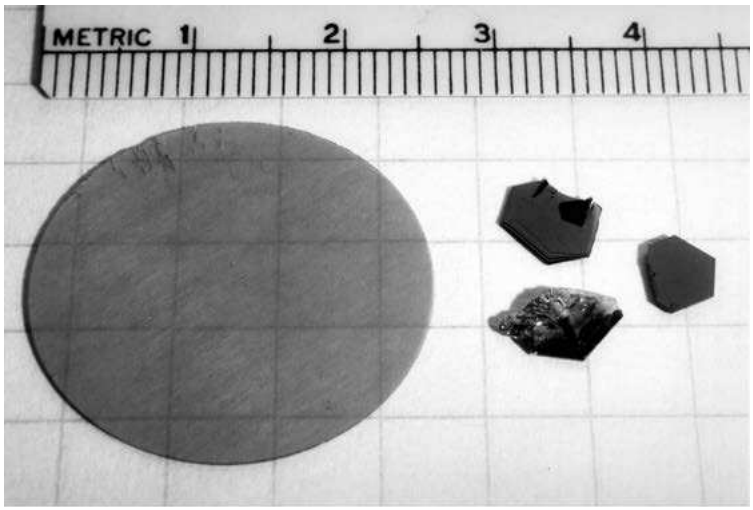
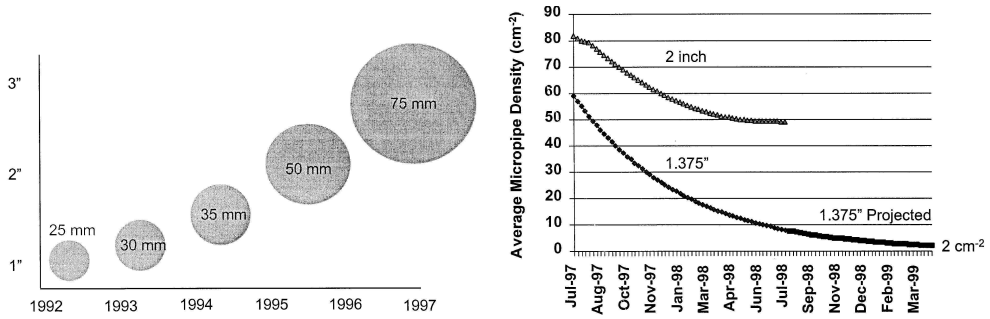


Figure 1.3: On the left 2.5*cm* 6H–SiC manufactured wafer by CREE by using seeded sublimation technique, on the right single–crystal SiC substrates available prior to 1989.

Thanks to the development of the modified Lely technique and its improvements in reducing micropipe densities (Fig. 1.4b) [14], larger single–crystal SiC wafers of electronic quality have became commercially available, as shown in Fig. 1.4a. As a consequence, the vast majority of silicon carbide semiconductor electronics development has taken place since the early 1990s.

PVT method has evolved from both commercial production environments and research laboratories up to date and it has became the current standard industrial process. High quality SiC wafers are routinely produced with the current PVT method (for the reason above it is called the standard PVT method). Currently 100*mm* 4H– and 6H–SiC wafers are commercially produced by standard PVT and 150*mm* wafers are expected in the near future [15].

Since the mid 1990s, other companies, besides CREE, have subsequently entered the SiC wafer market as reported in Fig. 1.5.



(a) (b)

Figure 1.4: (a) Increase of wafer size demonstrated by CREE company. (b) Reduction of micropipes densities in SiC Substrates of different dimension.

Vendor	Year	Product	Wafer Diameter	Micropipes (#/cm^2)	Price (US$)
Cree	1993	6H n-type, Si-face, R-Grade	3.0 cm	200 - 1000	1000
		6H n-type, Si-face, P-Grade	3.0 cm	200 - 1000	2900
		6H n-type, C-face, P-Grade	3.0 cm	200 - 1000	3000
		6H p-type, Si-face, P-Grade	3.0 cm	200 - 1000	3300
		4H n-type, Si-face, R-Grade	3.0 cm	200 - 1000	3800
Cree	1997	4H n-type, Si-face, R-Grade	3.5 cm	100 - 200	750
		4H n-type, Si-face, P-Grade	3.5 cm	100 - 200	1300
		4H n-type, Si-face, P-Grade	3.5 cm	< 30	2300
	1998	4H n-type, Si-face, R-Grade	5.1 cm	< 200	2100
		4H n-type, Si-face, P-Grade	5.1 cm	< 200	3100
	1997	4H p-type, Si-face, R-Grade	3.5 cm	< 200	1900
		4H Semi-Insulating, R-Grade	3.5 cm	< 200	4800
		6H n-type, Si-face, P-Grade	3.5 cm	< 200	1000
		6H p-type, Si-face, P-Grade	3.5 cm	< 200	2200
Nippon Steel	1997	4H n-type	2.5 cm	NA	NA
SiCrystal	1997	4H n-type, Quality I	3.5 cm	< 200	1200
		4H n-type, Quality III	3.5 cm	400 - 1000	900
		4H n-type, Quality I	2.5 cm	< 200	600
		6H n-type, Quality I	3.5 cm	< 200	1200
Sterling and ATMI/Epitronics	1998	6H n-type	3.5 cm	< 100	800
		4H n-type	3.5 cm	< 100	800

Figure 1.5: List of single–crystal SiC wafer providers since early 1990s.

1.2.2 SiC Epitaxial Growth

Although sublimation–growth techniques are relatively easy to implement, these processes are difficult to control, particularly over large substrate areas [1]. SiC is a material having more than 170 polytypes and each polytype shows different properties (as reported in Fig. 1.2 for the most common polytypes) such as different band–gap which can range from $2.4eV$ to $3.3eV$ [4]. Therefore, a key issue during the growth of SiC bulk material for electronic applications is the control of polytype. If special precautions are not taken, during SiC crystals grown by sublimation technique, the bulk material will contain inclusions of undesirable polytypes. Several technological parameters impact the final polytype structure of SiC crystals, in particular: supersaturation of the vapor above growing surface, growth temperature, growth pressure, seed surface orientation and polarity and presence of impurities. Another important technological improvement for the realization of SiC electronic devices with complex structures is the accurate control and type of doping impurities and the thickness of grown materials [15].

For these reasons, for improving the quality of bulk SiC material and realising complicated device structures, epitaxial growth methodologies such as liquid–phase epitaxy (LPE), molecular beam epitaxy (MBE), and chemical vapor deposition (CVD) have been also investigated.

In 1983 [16][17], the hetero–epitaxial growth of single–crystal SiC layers on top of large–area silicon substrates was firstly carried out. Unfortunately, hetero–epitaxy of SiC using Silicon as a substrate always results in growth of 3C-SiC with a very high density of defects, because of differences in lattice constant and thermal expansion coefficient between these two materials. For this reason, 3C–SiC has been commonly used for manufacturing Micro–Electro–Mechanical systems (MEMS)–based sensors (see as an example [18]), since the performance of electronic devices (Schottky barrier diodes (SBDs), pn diodes, MOSFETs) was far below that expected.

However, strong economic motivation still encourages to improve hetero–epitaxial growth of SiC on large–area Silicon substrates as this would provide cheap wafers for productions of SiC electronic devices that would be immediately compatible with silicon integrated circuit.

In 1987, Matsunami et al. [19] discovered that high–quality 6H–SiC can be homo–epitaxially grown by CVD at relatively low growth temperature, when a several degree off–angle, with respect to the c–axis substrates (obtained by Acheson [20] or modified Lely processes), is introduced into the 6H–SiC with (0001) orientation, this technique was called step–controlled epitaxy [21].

Step controlled epitaxy is based upon growing epilayers on a SiC wafer polished at an angle (called the tilt–angle or off–axis angle) of typically 3° to 8° off the (0001) basal plane, resulting in a surface with atomic steps and flat terraces between steps as schematically depicted in Fig.1.4. When growth conditions are properly controlled and there is a sufficiently short distance between steps, ordered lateral step flow growth takes place which enables the stacking sequence of the substrate to be exactly mirrored in the growing epilayer.

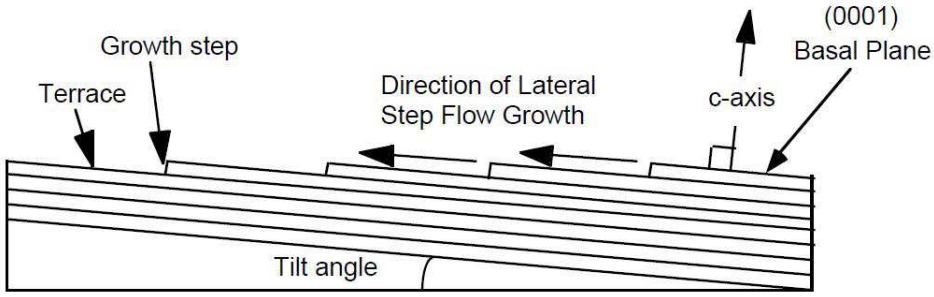


Figure 1.6: Schematic view of a step–controlled epitaxial growth.

Homo–epitaxial growth of 6H–SiC on off–axis 6H-SiC (0001) became a standard technique in the SiC community because it yielded high purity, good in–situ doping control [22] and uniformity.

In 1993, a high mobility of over $700 cm^2 V^1 s^1$ was first reported for 4H–SiC grown using this technique [23]. The combination of this result together with the superior physical properties of 4H-SiC, the commercial release of 4H polytype wafers, and demonstration of excellent devices realised with this material, made 4H–SiC the preferred choice for electronic device fabrication in the mid 1990s.

In 1995, a hot–wall CVD reactor was proposed by Kordina et al. [24]. This reactor

design is currently the standard, because it allows superior control of temperature distribution, has a much longer susceptor life and better growth efficiency.

1.3 Technological improvements in SiC Growth substrates

SiC devices realised since the 1990s, when the first high quality substrate was manifacured by CREE, began to show performances that in some cases exceeded those of GaAs or Si devices in high–power and high–temperature applications. As a consequence, physical properties and defects of SiC materials have been extensively investigated. At the same time, other grown techniques were considered in order to obtain wafers of higher quality, since substrates are the key elements in the development of electronic devices with high performances. Fig. 1.7 shows the current status about the knowledge of processing technologies for SiC substrates.

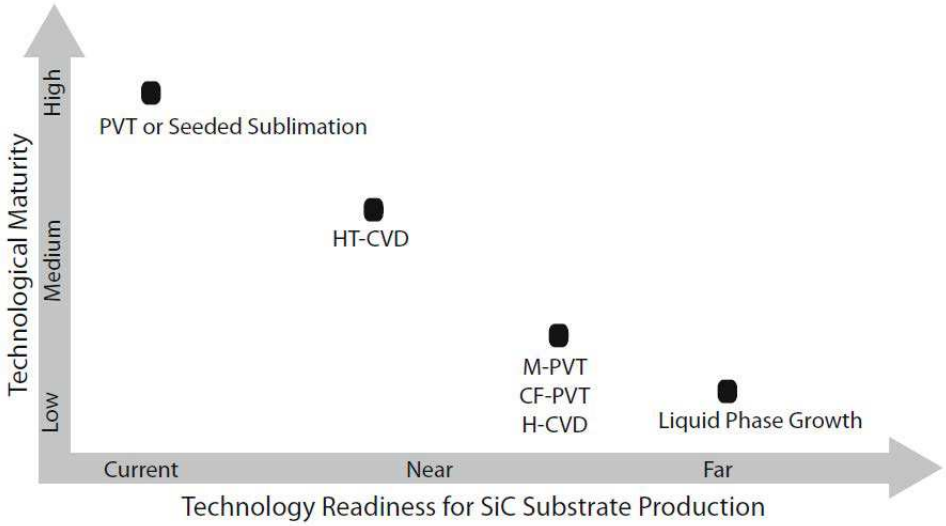


Figure 1.7: Current knowledge status of SiC process technologies for electronic grade substrates.

The above figure illustrates that the two most mature techniques, currently used in commercial environments, are the PVT process, discovered in the late 1970s and

the HT–CVD proposed more recently, as discussed in the previous section.

Other promising techniques are the Continuous Feed PVT (CF–PVT) [25], Halide CVD (H–CVD) [26], and Modified PVT (M–PVT) [27]. Although these latter growth techniques might have some technological edges over their predecessors, they are still at the research stage.

Solution phase growth has yet to prove its capability of producing large area substrates. Nonetheless, promising initial results and the advantages of this method will certainly draw more attention from the research and industrial community.

Chapter 2

Ion Implanted vertical 4H-SiC PiN diodes

2.1 Ion Implantation

Diffusion and Ion implantation are fundamental processes for introducing impurities in a semiconductor wafer through windows that are opened in selected regions of a mask film that is deposied, or grown, on the surface of the semiconductor wafer itself.

In the case of Silicon Carbide, because of its very strong chemical bonding, diffusion constants of impurities are extremely small. For this reason, a significant diffused dopant–depth profile requires both very high temperatures (larger than 2000°C) and relatively long times. Under these conditions, it is hard to find a good material for the fabrication of a sufficiently resistant diffusion mask, moreover, the decomposition of SiC at such high temperatures, as well as the formation of intrinsic and extended defects, are strongly favoured. The development of ion implantation processing for the selected area doping of SiC wafers is of major importance for obtaining: source or drain regions, junction termination, channel doping, p-body of FET devices, p^+ contact and p-n junction [2][28][29].

The most common dopants for SiC are Aluminum (Al) and Boron (B) for obtaining p-type doped regions, whereas Nitrogen (N) and Phosphorus (P) are used

for n-type doped regions. Implant profiles can be scheduled either by Monte Carlo simulations of the ion implantation process in software such as SRIM (Stopping and Range of Ions in Matter) [30], or, much better, by Pearson IV algorithms [31] which take into accounts experimental database for the different momenta of the ion depth distribution such as those in [32]. In both the cases, simulation outputs concern ion implantation processes along a random direction. The implantation geometry into a crystal is defined as random when the incidence ions experience as many energy losses and collisions as they would have in the same material but with amorphous structure [3].

The convention for identifying implantation geometries is linked to tilt and twist angles with respect to the wafer normal and the wafer flat, respectively. The tilt angle can be defined as the rotation angle in the direction of the wafer normal with respect to the ion beam incidence, whereas the twist angle is the rotation angle of the wafer around its normal, as shown in Fig. 2.1. The tilt and twist angle values depend on the relative position of the semiconductor lattice structure with respect to the wafer plane and on the ion species, ion energy, and ion beam direction.

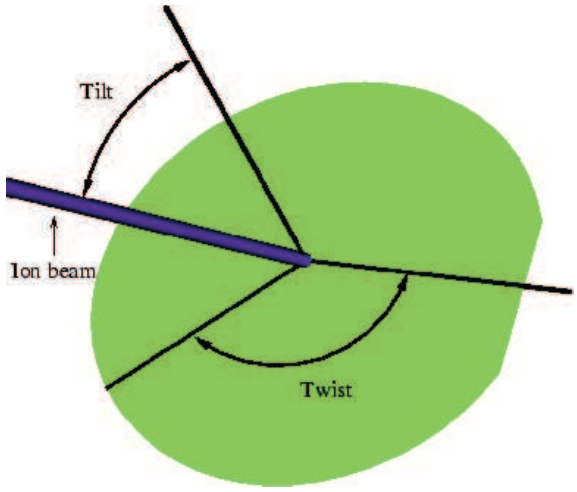


Figure 2.1: Illustration of tilt and twist angles for defining implantation geometry. See text for further details.

Fig. 2.2 depicts, as an example, a typical Nitrogen implantation profiles in SiC <0001> for different tilt angle θ. The symbols represent the SRIM simulation. In random implantation geometries, implanted ions follows an almost Gaussian–like distribution (this is the case of solid black line curve in Fig. 2.2). The choice of tilt and twist angles in order to obtain random implantation geometries does not guarantee that ions might be scattered along major crystallographic direction giving origin to undesired channeled trajectories [33][34][35] (dotted black line in Fig. 2.2).

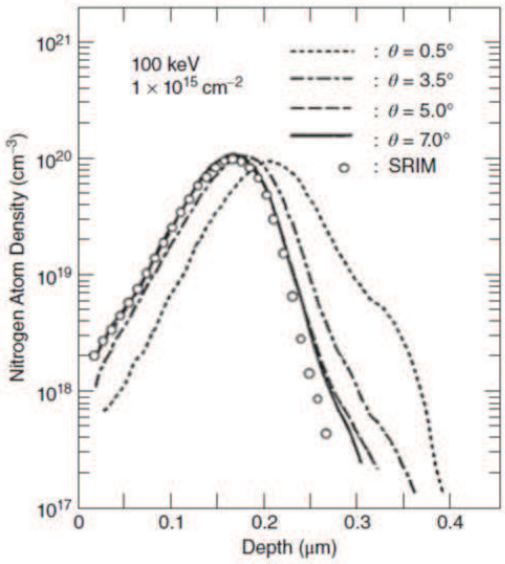


Figure 2.2: Depth profiles of Nitrogen implantation into SiC <0001> with various tilt angles.

In the case of SiC crystal the attempt to obtain random implantation is not trivial because of the poor knowledge about channelling phenomena in different SiC polytypes and because of the lack of a convention among material suppliers to provide the crystal orientation (e.g. [36], [37], [38]). For this reason, control and reproducibility of the implantation geometry in the case of SiC wafers is not a simple task.

For the realization of doping profiles which differ from the simple Gaussian distribution (shown in Fig. 2.2, symbols or solid black line), the technique of multiple

implantations is needed. In particular this procedure consists in a series of ion implants with different energies and doses. This technique is commonly used for obtaining flat profiles (like box) to form anodes region in p–n junction, an example is shown in Fig. 2.3. The sum of multiple energy ion implantation processes can be used for obtaining dopant depth profiles not obtainable by diffusion processes.

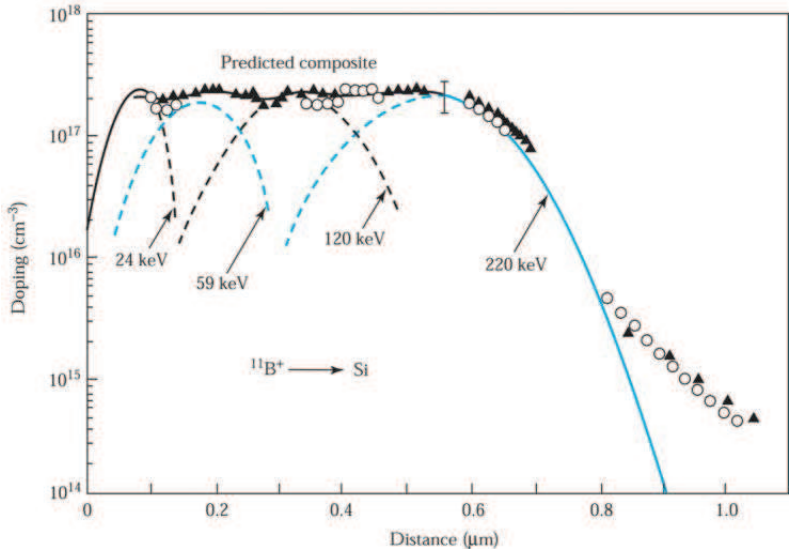


Figure 2.3: Example of multiple ion implantetion processes to obtain a flat box doping profile.

2.2 Post implantation annealing

The drawback of an implantation process is the damaging of the crystalline structure of materials due to the bombardment by ions. The generated damage can range from point defects to amorphization depending on the ion energies and implanted doses.

Recent studies have shown that the damage due to high implantation doses can be reduced by increasing the substrate temperature during implantation processes. This method, called dynamic annealing, allows the annihilation of defects and, for low

ion fluxes, defect densities can never reach the critical value for having the material amorphization. The schematic representation in Fig. 2.4 shows the effect of dynamic annealing: in particular by increasing the substrate temperature, higher implanted doses can be tolerated before material reaches the amorphization.

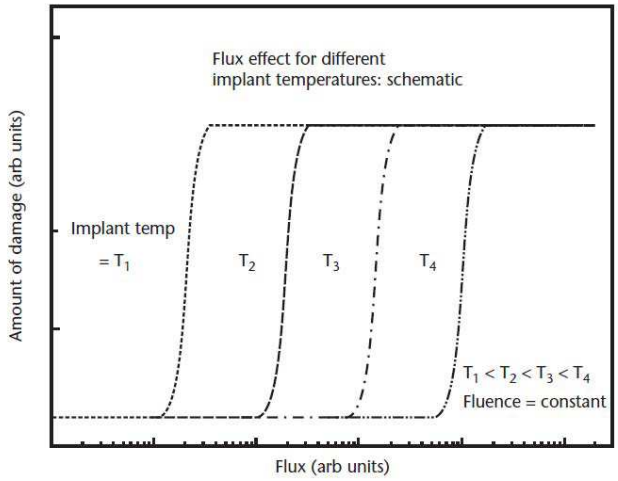


Figure 2.4: Schematic example of dynamic annealing. Increasing the substrate temperature a higher ion flux is tolerated during ion implantation processes.

However, for recovering the damaged lattice and for electrically activating the implanted dopants, post implantation annealing processes, at an appropriate combination of time and temperature, are mandatory after the ion implantation [39]. In the case of SiC, the understanding and accurate control of such a process is still a scientific challenge [3].

As an example, Fig. 2.5 depicts the resistivity as a function of *Al* concentration in a 4H–SiC sample [40] for different post implantation annealing temperatures. This figure illustrates that the higher the annealing temperature the lower the resistivity of the material. In particular, the resistivity of a material is the inverse of conductivity which, in turn, is directly proportional to the free carrier concentration. Therefore, the lower the resistivity the higher the free carrier concentration and, besides the dopant partial ionization, the higher the electrical activation. For this reason, in the case of

SiC, the post implantation annealing processes are usually performed at temperatures higher than 1600°C.

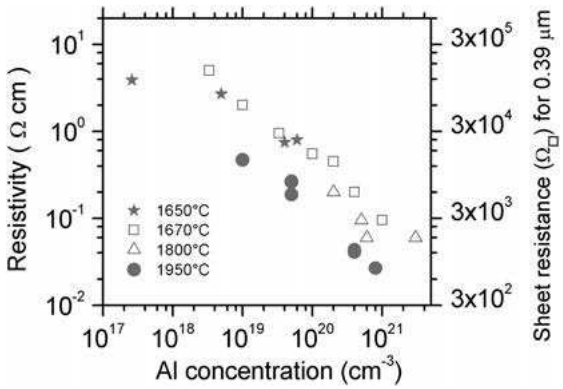


Figure 2.5: Resistivity versus Aluminum implanted concentration in a 4H-SiC sample for different annealing temperatures, see text for further details.

At such high annealing temperature surface degradation of SiC is observed with a subsequent lost of the typical mirror-like surface. This effect is shown in Fig. 2.6a where Atomic Force Microscope (AFM) image of a 4H-SiC sample is reported. Two are the mechanisms which contribute to surface degradation:

1. migration of Silicon atoms from SiC lattice to surface. This phenomena is enhanced if the sample is annealed in vacuum. Therefore, to overcome this migration, annealing in Silane overpressure can be performed [3];

2. migration or out–diffusion of dopant atoms to surface. This second mechanism cannot be avoided by using a simple Silane overpressure during annealing process, but a protective capping layer is needed. Among the capping materials the best results were given by a carbon cap which so far is commonly used in industrial device fabrications. Fig. 2.6b shows the surface morphology of the sample processes with a carbon cap layer.

During ion implantation processes, displacement of Si and C atoms occurs, generating point defects such as vacancies, interstitials and anti–sites. When post im-

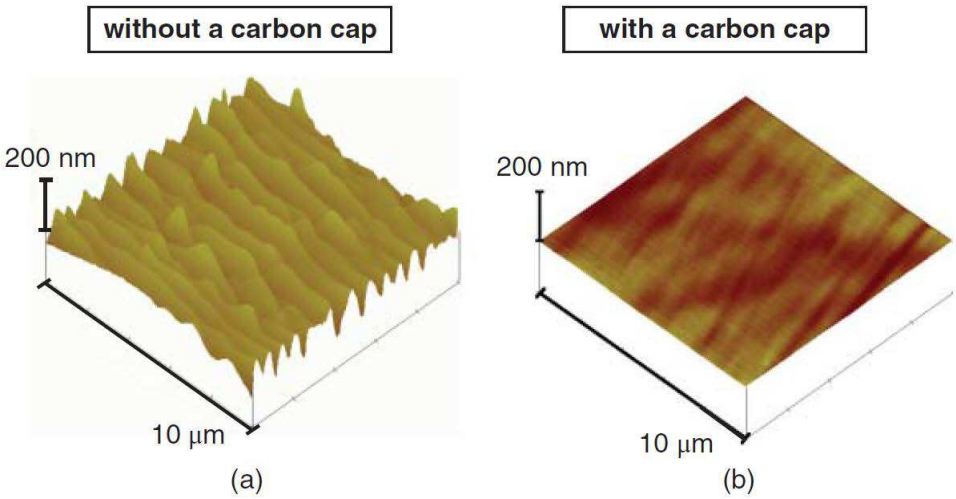


Figure 2.6: Surface morphology of SiC samples after annealing process (a) without protective carbon cap and (b) with protective carbon cap.

plantation annealing is performed, the generated points defect may also combine with implanted impurities giving rise to localized levels (shallow or deep) in the band–gap.

In literature (see as example [41][42][43]), the commonly observed deep levels in 4H-SiC are: Z1/2 with position of $(E_C - 0.63eV)$ and EH6/7 positioned at $(E_C - 1.55eV)$. These levels are observed in 4H-SiC after ion implantation regardless of dopant ions.

2.3 Ohmic Contacts

In general, an ohmic contact can be defined as a metal-semiconductor not rectifying junction which is able to supply the necessary device current and provides a very low voltage across its junction without injection of minority carriers [44], or, in other words, provides a very low resistance junction value compared to that of the semiconductor device [45]. In addition, in the case of Silicon Carbide, thermal stability is also required, since thanks to its properties SiC-based devices can operate at very

high-temperature.

Fig. 2.7 shows the 4H-SiC band diagram referring to the vacuum level. Ideally, for having an ohmic contact, a metal with work function $q\Phi_m$ lower than $q\chi_s$ for n–type material or higher than $q\chi_s + E_g$ for p–type material is required. In these cases, the carriers can flow in both directions without encountering any Schottky barrier.

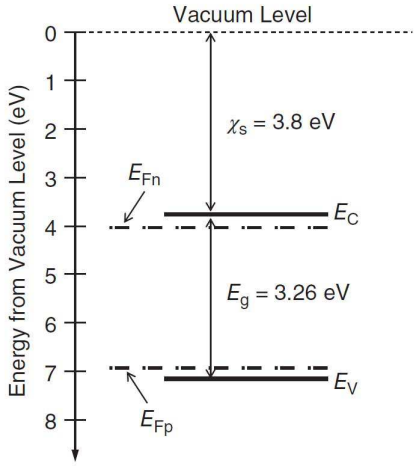
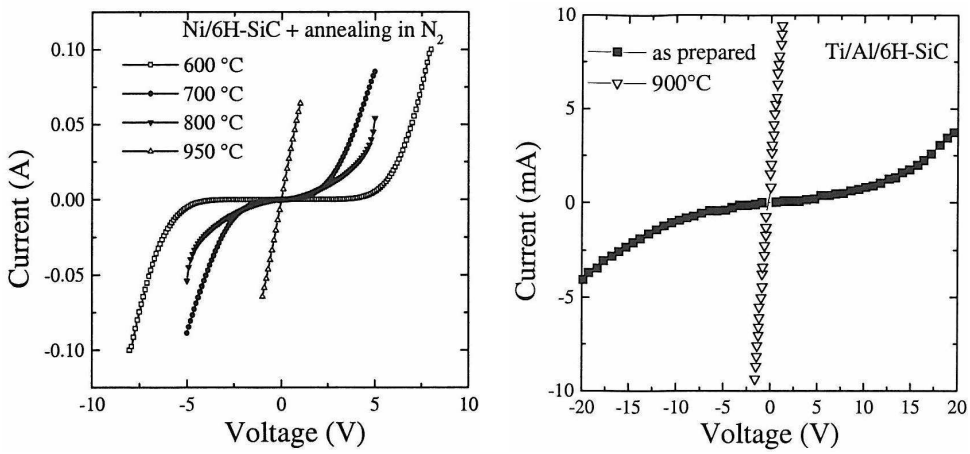


Figure 2.7: Band diagram of 4H-SiC.

However, almost all metals have a work function Φ_m between $5 \div 6eV$ and therefore, as shown in Fig. 2.7, in 4H-SiC ideal ohmic contacts cannot be realized especially on p–type material [46]. To overcome this problem in the case of wide band–gap materials, the common strategies to form low resistivity ohmic contacts is by using the tunnelling current phenomena [2].

In general, the as-deposited Metal–SiC contacts are non ohmic but with rectifying properties because of the high value of the Schottky barrier. Therefore, besides to the creation of highly doped layers for tunnelling phenomena and the accurate choice of a metal which may form a low barrier height, a post deposition annealing process at temperature in the range $900 \div 1000^{\circ}$C is required. As an example, Fig. 2.8 shows electrical Trasmission Line Model (TLM) measurements of as-deposited and after annealing process of Ni on n–type 6H-SiC (2.8a) and of Al/Ti on p–type 6H-SiC

(2.8b).



(a) (b)

Figure 2.8: (a) Ni deposition on n–type 6H-SiC (b) Al/Ti deposition on p–type 6H-SiC, before and after annealing process.

This figure clearly illustrates that rectifying properties of Metal–SiC junction occurs if annealing processe temperatures lower than 900°C are performed. For higher temperature reactions at the interface Metal-SiC with formation of Silicides, Carbides or ternary phase occurs with subsequent reduction of barrier height and formation of ohmic contacts.

Among the metals, the most suitable for creating ohmic contacts on n–type SiC is Nichel (Ni). Specific contact resistance values of $\rho_C \approx 10^{-6}\Omega cm^2$ were measured, furthermore Ni offers long term stability at high temperature [46].

For the reason discussed earlier, ohmic contacts on p–type SiC are not simple to realize. Nevertheless, thanks to the low Schottky barrier height and because it is commonly used for p–type doping, Al is the most suitable metal to form ohmic contacts on p–type SiC. Unfortunately, its low melting point (about 600°C) cannot allow to form a pure Al metal on SiC. To overcome this problem Al-based alloys are commonly used to realize ohmic contacts on p–type SiC, in particular, the most

employed are Al/Ti alloys and its modification (e.g. Al/Ti/Ni) [2].

The sintering process for obtaining good ohmic contacts on p–type SiC is still a scientific challenge, in particular the conservation of form factor and thickness of the chemically reacted layer at the interface Metal-SiC are still open issues (e.g. [47]).

2.4 Process steps

A <0001> 8° off–axis 4H–SiC n–type homo–epitaxial commercial wafers [13] was used to fabricate vertical p^+–i–n^- diodes.

The n^- epi–layer thickness and doping are $25\mu m$ and $3 \times 10^{15} cm^{-3}$, respectively. The n–type bulk wafer is $372\mu m$ thick and has a resistivity of $0.021\Omega cm$.

The p^+ anodes are circular with different diameters in the range $150 \div 1000\mu m$ and have been obtained by multiple-energies Al^+ ion implantation processes at 400°C on selected areas. The implantation schedule has been fixed on the base of SRIM2008 simulation outputs [30] for obtaining an almost flat $2.5 \times 10^{20} cm^{-3}$ *Al* depth box profile thick about $0.57\mu m$.

Post–implantation annealing process has been performed inside an inductively–heated graphite crucible in a high–purity Ar atmosphere at 1950°C for 5 min. The heating rate was 40°C/s and the cooling rate was exponential with a characteristic time of about 3 min.

A resist film pyrolyzed in a forming gas ambient (C-cap) [48] has protected the wafer surface during post–implantation annealing and was later removed by 850°C/15 min dry oxidation.

Ohmic contacts on the p^+–implanted anodes and on the n^+ bulk cathode have been formed with Ti/Al (80 nm/350 nm) and Ni (150 nm), respectively. Contacts were alloyed at 1000°C/2min in vacuum. After alloying, the anode contacts were covered by a sputtered 350 nm Al(2%Si) film. The contacts on p^+ are circular, concentric with the anodes and 40-50μm smaller in diameter than the anode. The Ni cathode contact extends all over the wafer back surface.

Previous studies on the electrical activation [49] and the surface roughness [50] of Al^+ implanted 4H-SiC specimens have shown a root mean square surface roughness

$\leq 2nm$ and an Al electrical activation of about 80% with a compensation of about 20% for 4H-SiC samples doped as the diode's emitters of this study.

2.5 Static electrical measurements

2.5.1 Device schematic cross–sections and selection criteria

The studied diodes were placed, together with other test structures such as TLM for specific contact resistance measurements and VdP (Van der Pauw) for electrical activation measurements, on chips with dimension of $5 \times 7mm$. The image representing the elementary cell which repeats over all the wafer is shown in the bottom of Fig. 2.9. Table 2.1 summarize anode (diameter) and metal dimensions of on–chip diodes. In this Table, the column labelled $(D-M)/2$ (where D is the Diameter, and M the Metal) reports the distance between metal edge and the end of diode anodes. For all diodes, besides D7, this distance is $25\mu m$, while for the $150\mu m$ diameter diode D7 is $20\mu m$.

Devices have been fabricated in the clean–room facility of National Research Council, Institute of Micro–electronics and Micro–systems, Bologna Unit (CNR–IMM UOS Bologna) [51], by using processes described in the previous section. A schematic cross–section of processed diodes is shown in the top of Fig. 2.9.

2.5.2 Experimental Setup description

Static forward and reverse current-voltage characteristics were measured by using a home assembled wafer–level parametric characterization system. Measurements were performed in air at different temperatures. The minimum temperature was 30°C whereas the maximum 290°C, the other measurement temperatures range between $50 \div 250$°C with a step of 50°C. All the measurement instruments were remote controlled by GPIB 488 protocol and a Keithley 707a switching matrix and configured by using the commercial software ICS (Integrated Controll System).

Forward current measurements were performed by using two Keithley SMUs (Source/Measure Units) model 238 in particular: the first connected to the thermo–

DIMENSION OF PROCESSED DIODES

Label –	Diameter $[\mu m]$	Metal $[\mu m]$	$(D-M)/2$ $[\mu m]$	number –
D7	150	110	20	4
D1	250	200	25	4
D2, D6	400	350	25	8
D3	600	550	25	4
D4	800	750	25	3
D5	1000	950	25	3

Table 2.1: Labels and dimensions of processed diodes.

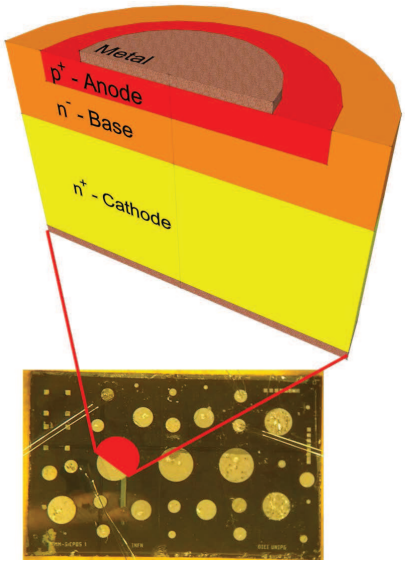


Figure 2.9: In the top a schematic cross section of the studied diodes and in the bottom a processed chip containing the studied devices are shown.

chuck for fixing the reference voltage at $0V$, the second to the probe tip placed on device anodes. The maximum applied voltage was $3.9V$ and the minimum step for performing the voltage sweep was $30mV$. This latter values ensured a stable output of the SMU. A study on delay time between the voltage application and the current reading was performed and an optimum delay of $4s$ was found. This time is sufficient to avoid apparent leakage currents due to transients of parasitic connection elements. By using the described measurement configuration a current floor of $5 \times 10^{-14}A$ was measured at Room Temperature (RT).

Since very low reverse currents are expected in the case of SiC devices, the Keithley Sub–femto–amperometer model 6430 was used for reverse measurements on the studied diodes. In this case for minimizing the influence of parasitic leakage currents, the instrument was directly connected to the thermo–chuck avoiding switching matrix connections. The maximum reverse bias voltage was $-190V$ and sweep step was $-10V$. A study on the delay time, similar to that of forward current measurements, was performed and a delay time of $300s$ was applied for this measurements with a current reading each $5s$ in order to observe the trend of experimental data as a function of time. In this case a current floor of $\approx 5 \times 10^{-15}A$ was measured at RT.

2.5.3 Diode selection criteria

Among all devices on wafer, only few diodes with precise properties were measured at different temperatures. In particular, the following criteria was adopted for selecting the good devices:

- forward characteristic study: only diodes with no shunt current at low voltages and with higher current in ohmic region at the minimum measurement temperature (i.e. 30°C) were selected;
- reverse characteristic study: only diodes with the lower reverse current at the maximum bias voltage ($190V$) and with no evidence of break–down trend at the maximum measurement temperature (i.e. 290°C) were selected.

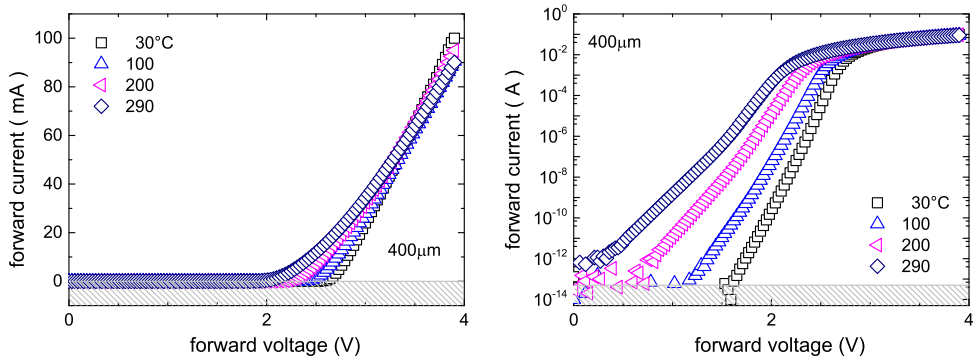
By adopting the above selection criteria, after a first screening, one diode for each

dimension among those listed in 2.1, were considered. In particular, diodes D7, D2, D3 and D5 were characterized at all temperatures for forward study, whereas diodes D7, D2 ad D3 for reverse study.

2.5.4 Experimental measurements

Fig. 2.10 shows a typical current–voltage curves of diodes selected by using the criteria described earlier, in particular: Fig. 2.10a shows the forward current–voltage curves in the case of linear scale, whereas Fig. 2.10b in logarithmic scale, for $400\mu m$ diameter diode for some measurement temperatures. In these figure the instrumental current floor of $5 \times 10^{-14} A$ at RT is represented by the grey dashed region.

In the case of linear scale, it is worthwhile pointing out that the diode enters the high–injection regime. In particular, after switching on, a typical exponential–like trend of the current–voltage curve for each temperature can be observed. This trend indicates that the resistance of the diode base is lowering because of typical modulation of the PiN diode base [52][53].



(a) (b)

Figure 2.10: (a) Linear scale and (b) log scale current–voltage characteristic of a $400\mu m$ diameter diode of this study, for varying temperatures.

In the case of logarithmic scale, the curves have no evidence of shunt currents at low voltages and, after switching on, clearly show two different exponential trend

before entering the ohmic region. Under the assumption that the forward current can be modelled by using the following equation:

$$I(V,T) = I_0 \cdot \left[exp\left(\frac{qV}{nkT}\right) - 1 \right] \tag{2.1}$$

where I_0 is the saturation current (or zero voltage current), q is the electron charge, V the applied voltage, k the Boltzmann constant, T the absolute temperature and n the ideality factor. The estimation of n as a function of voltage and temperature is straightforward, in particular, considering Eq. (2.1), n can be expressed as:

$$n(V,T) = \frac{1}{\frac{kT}{q}\frac{d[\ln I(V,T)]}{dV}} \tag{2.2}$$

By using Eq. 2.2, the trend of the ideality factor, of forward current–voltage curves showed in Fig. 2.9, is obtained as a function of the applied voltage and for each measurement temperature. This plot illustrates that the current curves show a trait with ideality factor n equal 2 for almost all temperatures at low voltages, never passing through 1 before entering the ohmic region. This trend has been observed for all the studied diodes.

As an example, Fig. 2.12 illustrates the data analysis method for the reverse current in the case of $400\mu m$ diameter diode for two fixed voltages: $20V$ Fig. 2.12a and $180V$ Fig. 2.12b at the fixed temperature of 150°C (the same analysis was performed for all diodes at all temperatures and for all bias voltages).

In particular, static current values have been obtained by studying the current as a function of time. It has been observed that the thermo–dynamic equilibrium of devices in the case of low bias voltage (for all temperatures) is reached after $300s$ (Fig. 2.12a), whereas for higher bias voltages and high temperature the the thermo–dynamic equilibrium is reached almost immediately (Fig. 2.12b). This means that for low voltages and low temperatures the current measurements are mainly influenced by the parasitic transients due to connections. The influence of transients become less important when the measured current signal increases (Fig. 2.12b), therefore devices reach the equilibrium faster with the increasing currents.

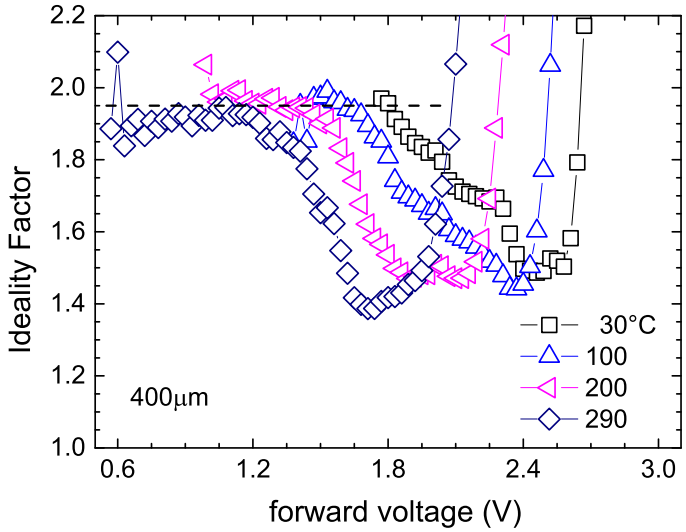
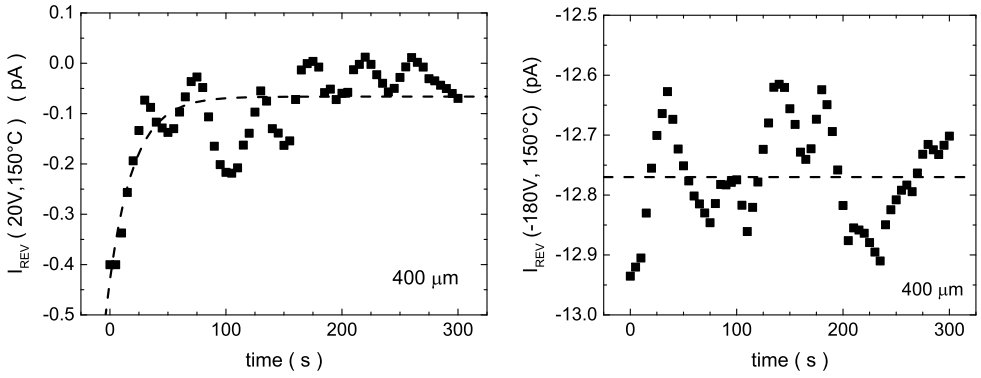


Figure 2.11: Trend of ideality factor of curves showed in Fig. 2.10.



(a) (b)

Figure 2.12: Example of data analysis for two different reverse bias voltage (a) $20V$ and (b) $180V$ for the fixed temperature of 150°C for a $400\mu m$ diameter diode.

For a more accurate estimation of the reverse current, especially at low voltages, the value of the current measured at $0V$ bias voltage, which takes into account for the noise current due to the instrumental offset voltage, has been subtracted from all currents obtained at other bias voltages at all temperatures, in particular:

$$I_{rev}(V,T) = I_{rev\_meas}(V,T) - I_{rev\_meas}(0,T) \tag{2.3}$$

where in Eq. (2.3) $I_{rev\_meas}(V,T)$ is the measured reverse current at the bias voltage V and at the temperature T.

Fig. 2.13 depicts a typical reverse current characteristic of a $400\mu m$ diameter diode at different temperatures. The characteristics of all diodes have similar trend and have been obtained by using the method described above. The grey dashed box points out the region above which the measured current has a reliable values (i.e. above the instrumental current floor). Data within the box or at its boundary have been obtained as a consequence of the operation by using Eq. (2.3), for this reason these experimental data were excluded for data analysis.

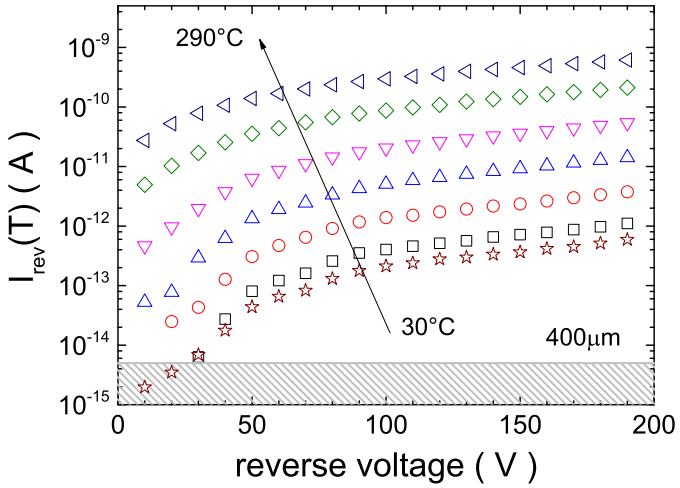


Figure 2.13: Typical reverse characteristic of a diode of this study for all the measurement temperatures.

Chapter 3

Analysis of Static current–voltage curves

3.1 Motivations

The common way for obtaining the area current density from forward or reverse current–voltage characteristics of devices is to divide the measured current by the active area of device itself:

$$J(V,T) = I_{meas}(V,T)/A \tag{3.1}$$

Nevertheless, the above relationship has validity only if the measured current originates from the device volume, in other words only if periphery effects are insignificant.

It is well–known that, in the case of Silicon Carbide devices, the periphery contribution to the total measured current is not negligible and indeed its importance has been claimed several times (see as an example [54][55][56]). However, few are the studies which shows the separation and the accurate analysis of periphery and volume current components in forward and reverse bias in the case of SiC devices.

The aim of this thesis work is to provide a methodology for deeply studying the current–voltage characteristics of SiC devices in order to obtain a better comprehen-

sion of such a device performances and reliable estimates of the physical parameters which can help to improve the device fabrication processing.

In the following sections area and volume currents have the same meaning, as the device volume is the volume which lies below the device active area, in particular: for the diodes of this study is the volume which lies under the diode anodes. Therefore, the area or volume current is the current which flows through the area which defines the volume or which flows in the volume with a section equal to the active area.

3.2 Extraction of Area and Periphery current densities

3.2.1 Theoretical background I

The measured current of a planar diode, $I_{meas}(V,T)$, which is voltage (V) and temperature (T) dependent, can be written as a sum of several contributions, in particular [57]:

$$I_{meas}(V,T) = AJ_{area}(V,T) + PJ_{per}(V,T) + CI_{cor}(V,T) + I_{par}(V,T) \tag{3.2}$$

where:

- A and P are Area and Perimeter of the planar junction interface, i.e. Area and Perimeter of the anode, respectively;
- C is the number of corners at P;
- $J_{area}(V,T)$ and $J_{per}(V,T)$ are the current densities per unit area A and per unit length of the perimeter P, respectively. More precisely: $J_{area}(V,T)$ is the current which flows in the volume defined by the junction area of devices and $J_{per}(V,T)$ is the current which flows in the periphery of devices;
- $I_{cor}(V,T)$ is the current value per corner;
- $I_{par}(V,T)$ is a contribution that takes into account parasitic currents of the measurement system.

$I_{cor}(V,T)$ depends on the device geometry and $I_{par}(V,T)$ depends on the used instrumental set–up.

In this study, vertical planar 4H-SiC p-i-n diodes with circular emitters of different diameters (see Chapter 2, Table 2.1) were characterized. This geometry allows to neglect the $CI_{cor}(V,T)$ term in Eq. (3.2). Moreover, forward and reverse current-voltage measurements were performed with two instrumental set–up with current floors of $5\times10^{-14}A$ and $5\times10^{-15}A$, respectively, in the whole voltage and temperature ranges of measurements (see Chapter 2, section 2.5.2). Therefore, in the case of forward bias, $I_{par}(V,T)$ term in Eq. (3.2) was neglected as its value is very small compared to that of the measured current (see Fig. 2.10b).

In conclusion, considering that $A=\pi r^2$ and $P=2\pi r$, where r is the anode radius, Eq. (3.2) can be written as:

$$I_{meas}(V,T)\approx \pi r^2 J_{area}(V,T)+2\pi r J_{per}(V,T) \tag{3.3}$$

When all terms of Eq. (3.3) are divided by the junction area $A=\pi r^2$, the following equation is obtained:

$$\frac{I_{meas}(V,T)}{\pi r^2}=J_{area}(V,T)+J_{per}(V,T)\frac{2}{r} \tag{3.4}$$

Making a plot of the measured current divided by the emitter Area (πr^2) versus the Perimeter–Area ratio ($2/r$) for each voltage and at a fixed temperature, the separation of Area and Perimeter current densities is obtained. In particular, by using a linear fitting on the so obtained curves, the intercept of the straight line gives the Area current density and its slope the Perimeter current density. From Eq. (3.4) it is evident that:

$$\forall V>3k/T,\quad \frac{I_{meas}(V,T)}{\pi r^2}\equiv J_{area}(V,T)\quad\Longleftrightarrow\quad J_{per}(V,T)\cong 0\vee A>>P$$

In other words, the measured current divided by the diode emitter area (Eq. 3.1) well approximates the area current density only in case of:

- straight line with negligible slope (i.e. $J_{per}\approx 0$);

- large area diodes, this latter condition (i.e. $A >> P$) is not fulfilled by the SiC diodes of this study.

For the identification of the current type, the model proposed by Sah et al. [58][59] for planar diodes with cylindrical symmetry (this suits the case of ion implanted diodes, Fig. 2.9) is considered. In this model, the diode total current is the sum of four contributions:

i) a bulk recombination-generation current in the space charge region (SCR) of the p-n junction that extends at the interface between emitter and base regions (Fig. 3.1, SCR II, segment e–f–g). This interface is the sum of the emitter area plus the emitter lateral surface (Fig. 3.1, SCR II, polygon h–c–d–e–f–g);

ii) a bulk diffusion current in the quasi neutral regions of the emitter volume and surrounding diode base (Fig. 3.1, region V);

iii) a surface recombination-generation current in the region where the p-n junction intercepts the wafer surface (Fig. 3.1, region III, region g–h);

iv) a bulk recombination-generation current in a channel that may form at the sample surface next to the Space Charge Region (SCR II, Fig. 3.1) because of the native oxide/SiC interface charges (Fig. 3.1, SCR IV, delimited by the polygon a–b–h).

The first two currents depend on the volume of devices, therefore from the area current density $J_{area}(V,T)$ in Eq. (3.3). The other two depend on the periphery of devices and may be linked to the perimeter current density $J_{per}(V,T)$ in Eq. (3.3). All these current components have an exponential dependence on V, so that for V greater than few kT/q can be written as:

$$I(V,T) = I_0 \cdot \left(exp \frac{qV}{nkT} \right) \tag{3.5}$$

where I_0 is the saturation or zero-voltage current that is dependent on the current type, q is the electron elementary charge, V the applied voltage, k the Boltzmann constant, T the absolute temperature and n the ideality factor.

The value of n determines the type and the nature of the current, more precisely: for current type *i)* $n = 2$, for current type *ii)* $n = 1$, for current type *iii)* $1 < n < 2$ and for current *iv)* $1 < n < 4$.

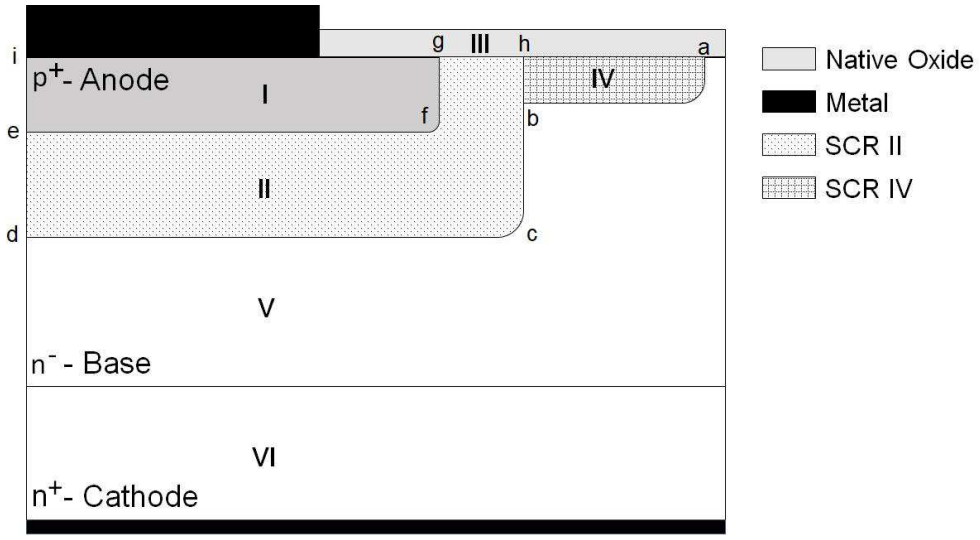


Figure 3.1: Two–dimensional schematic representation of the Sha model for diodes of this study (see Chapter 2, Fig. 2.9).

3.2.2 Experimental Area and Perimeter current density curves

Fig. 3.2a shows the set of current–voltage curves at RT in logarithmic scale of the diodes selected for this study. Fig. 3.2b plots the current density versus the applied voltage obtained dividing the current–voltage curves of Fig. Fig. 3.2a to the area of diodes. The plotted current density curves differs each other, periphery effects might affect the diode characteristics. Starting from the forward characteristics showed in Fig. 3.2a, the algorithm described in the previous section was applied in order to obtain the Area and Perimeter current densities. Figure 3.3 shows, as an example, a typical plot in linear (a) and logarithmic (b) scale constructed by Eq. (3.4) at a fixed temperature of 30°C and for different values of forward bias voltage (the same plot was constructed in the case of reverse bias).

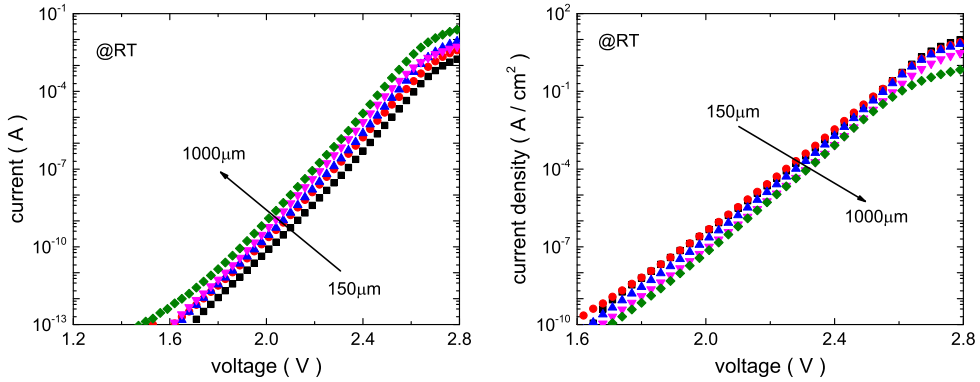


Figure 3.2: (a) Current–voltage characteristics at RT for all diodes of this study. (b) The curves showed in (a) are divided by the anode area for obtaining the corresponding current densities.

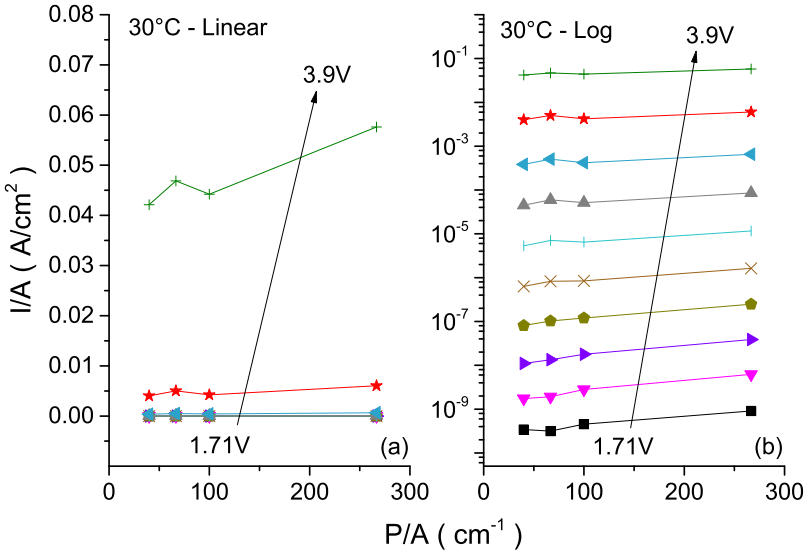


Figure 3.3: Experimental current data divided by the emitter area of the studied diodes and plotted versus the ratio $2/r$ by using Eq. (3.4) at 30°C in linear (a) and logarithmic scale (b).

For each studied temperature, the starting voltage for the data analysis (1.71V at 30°C, in Fig.3.3) is determined from the lowest common voltage among the whole set of diodes which ensures a conduction current higher than the instrumental current floor.

As clearly shown in Fig. 3.3(b) the slope of the curves decreases with increasing voltages, meaning that the perimeter current is higher at low voltages and decreases for increasing voltages.

Figure 3.4 features the core data of this study in the case of forward bias. In particular, (a) the perimeter ($J_{F,Per}$) and (b) the area ($J_{F,Vol}$) current density, obtained from the intercept and the slope of curves in Fig. 3.3, respectively, are plotted as a function of the applied voltage for different temperatures of measurement in logarithmic scale.

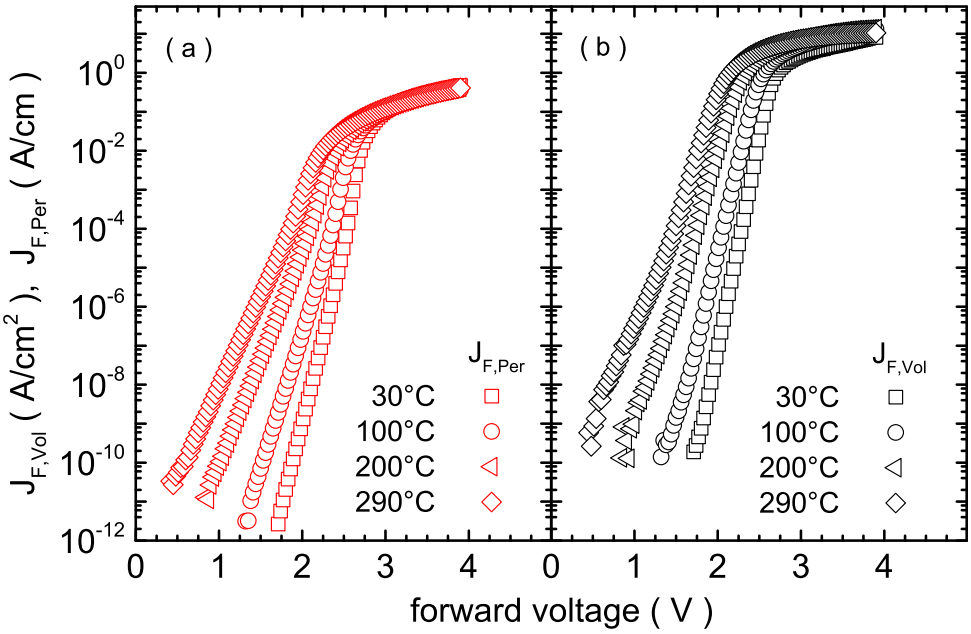


Figure 3.4: Experimental perimeter (a) and area (b) current densities plotted versus the applied voltage for several temperatures.

In Figure 3.5 the trend of the ideality factor, computed by using Eq. (2.2), of the perimeter (a) and area (b) current densities is illustrated as a function of forward bias.

These figures show that at low voltages and at all temperatures both the area and perimeter current densities have an exponential trend with a value of *n* around 2 and that for increasing voltages 1<*n*<2 never passing through 1 before entering the ohmic region.

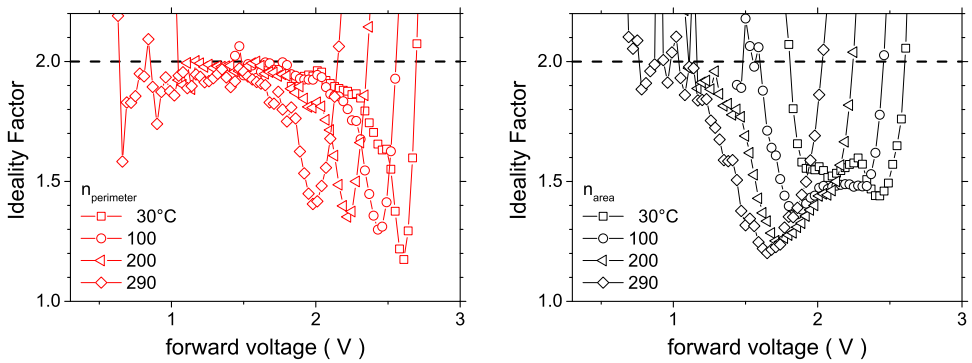
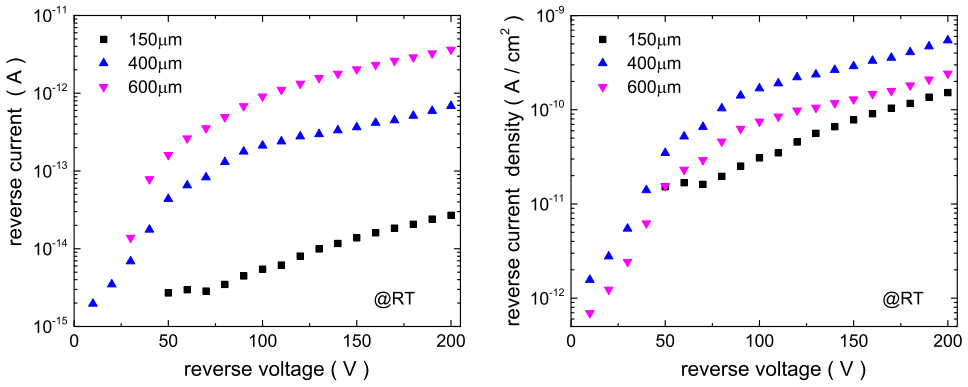


Figure 3.5: Trend of the ideality factor *n* for the perimeter (a) and the area (b) current density.

A check like that for forward characteristics (Fig. 3.2), was performed for the reverse curves of the selected diodes. In particular, Fig. 3.6a shows the reverse current curves at RT in logarithmic scale of the diodes and Fig. 3.6b show the corresponding reverse current densities. This might mean that periphery effect might affect the measured reverse diode characteristics.

In Figure 3.7 are displayed (a) the Perimeter ($J_{R,Per}$) and (b) Area ($J_{R,Vol}$) current densities, in the case of reverse bias: they are extracted by using the same algorithm used for forward bias (see, as an example Fig. 3.3) and described in the previous section.

For small diameter diodes and for lower bias voltages, the measured reverse current was comparable with the instrumental detection limit (as detailed in Chapter 2, Section 2.5.2, Fig. 2.13). Therefore, in the temperature range from 24°C up to 150°C, the obtained Area and Perimeter current density curves in Fig. 3.4 start at the reverse

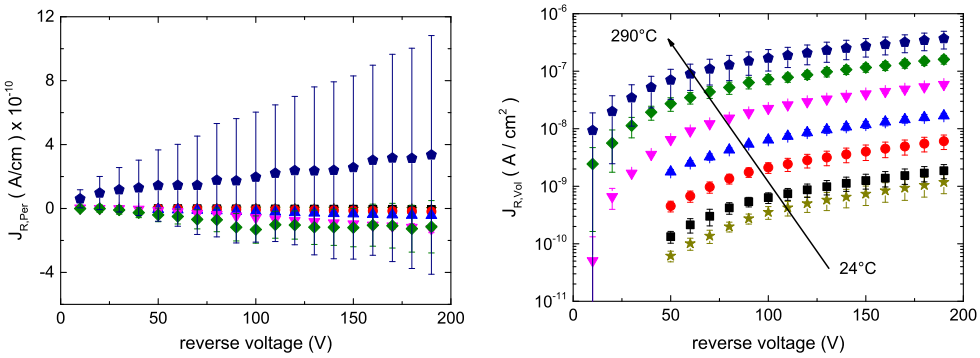


(a) (b)

Figure 3.6: (a) Reverse current–voltage curves at RT for all diodes of this study. (b) The curves showed in (a) were divided to the anode area for obtaining reverse current densities.

voltage of $50V$. For higher temperatures, over 150°C, the value of reverse current was sufficiently high to be detected even at low voltages.

The reverse perimeter current density is scattered and has not a well defined trend dependence on the temperature and voltage and its value is always lower than the area current density. Therefore, it was assumed that the reverse current of these devices can mainly linked to their volume. For this reason the fitting of curves like those showed in Fig. 3.3 was performed by assuming null slope: the obtained results are shown in Fig. 3.8. The Affinity between absolute current values in the latter figure and those showed in Fig. 3.7b, confirm that the contribution of perimeter reverse current density can be neglected and therefore the reverse current density of these devices can be linked to their volume.



(a) (b)

Figure 3.7: (a) Perimeter (in linear scale) and (b) Area (in logarithmic scale) reverse current densities

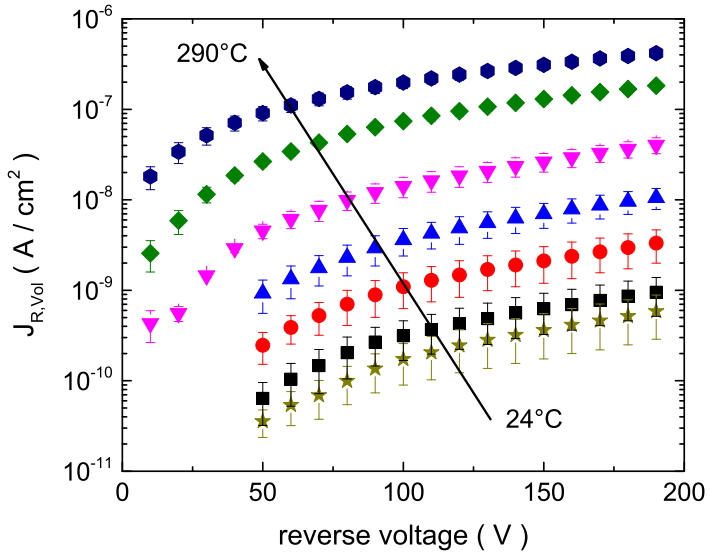


Figure 3.8: Reverse area current density ($J_{R,Vol}$) for increasing voltage and temperature is shown. This current was obtained by using algorithm described in the previous section, assuming negligible perimeter current (null slope).

3.3 Current temperature dependences and Arrhenius plot

3.3.1 Theoretical background II

Area current density

The forward area current density $J_{F,Area}$ (J_{area} in Eq. 3.3), in the ideal case of a semi–infinite bipolar junction, is the sum of a recombination ($J_{F,Area\_rec}$) and diffusion ($J_{F,Area\_diff}$) currents, as described in the Sah model, in particular:

$$J_{F,Area}(V,T) = J_{F,Area\_rec}(V,T) + J_{F,Area\_diff}(V,T) \tag{3.6}$$

The two terms of Eq. (3.6) can be expressed as [45]:

$$J_{F,Area\_rec}(V,T) = \frac{qW(V,T)n_i(T)}{2\tau_r(T)} \cdot exp\left(\frac{qV}{2kT}\right) \tag{3.7}$$

$$J_{F,Area\_diff}(V,T) = q\sqrt{\frac{D_p(T)}{\tau_p(T)}} \cdot \frac{n_i^2(T)}{N_D} \cdot exp\left(\frac{qV}{kT}\right) \tag{3.8}$$

where q is the electron charge, W is the depletion region width, n_i is the intrinsic carrier concentration, τ_r is the effective carrier recombination lifetime in the Space–Charge Region (SCR), k is the Boltzmann constant, D_p and τ_p are the minority carrier diffusion coefficient and lifetime, respectively, and N_D is the ionized donor concentration in the diffusion region. Dependences on the absolute temperature T and on the applied voltage V of all variables in Eqs. (3.7) and (3.8) are specified inside the round brackets.

An accurate study of pre–exponential factors, or saturation zero-voltage currents, in Eqs. (3.7) and (3.8) is remarkable since these currents are linked to the material parameters, in particular: τ_r and the ratio D_p/τ_p.

The temperature dependences of the pre–exponential factors of the above equations can be studied by extrapolating to zero–voltage the relative current component, therefore:

$$J_{F0,Area\_rec}(0,T) = \frac{qW(0,T)n_i(T)}{2\tau_r(T)} \tag{3.9}$$

$$J_{F0,Area\_diff}(0,T) = q\sqrt{\frac{D_p(T)}{\tau_p(T)}}\cdot\frac{n_i^2(T)}{N_D} \tag{3.10}$$

where in above equations the intrinsic carrier density can be expressed as [45]:

$$n_i(T) = \sqrt{N_C(T)\cdot N_V(T)}\cdot exp\left(-\frac{E_g(T)}{2kT}\right) \tag{3.11}$$

In Eq. (3.11) $N_C(T)$ and $N_V(T)$ are the temperauture–dependent effective density of state in the conduction and valence band, respectively and $E_g(T)$ is the temperature dependent band–gap. These quantities can be expressed as [45]:

$$N_C(T) = 2\cdot\left(\frac{2\pi m_{de}kT}{h^2}\right)^{3/2}\cdot M_c \tag{3.12}$$

$$N_V(T) = 2\cdot\left(\frac{2\pi m_{dh}kT}{h^2}\right)^{3/2} \tag{3.13}$$

$$E_g(T) = E_g(4K) - \frac{\alpha T^2}{(\beta+T)} \tag{3.14}$$

where in Eqs. (3.12) and (3.13) m_{de} and m_{dh} are the density of state effective mass for electrons and holes, respectively, h is the Planck constant, in Eq. (3.12) M_c is the number of equivalent minima in the conduction band. In Eq. (3.14) $E_g(4K)$ is the value of the energy gap at 4K, α and β are two fitting parameters.

Under the hypothesis of abrupt junction, assuming $N_A >> N_D$ (with N_A and N_D are the net acceptors and donors densities, respectively), the depletion layer width $W(V,T)$ in Eq. (3.7) can be expressed as [45]:

$$W(V,T) = \sqrt{\frac{2\varepsilon_0\varepsilon_r}{qN_D}\cdot(V_{bi}(T)-V)} \tag{3.15}$$

where ε_0 is the vacuum dielectric constant, ε_r is the relative material dielectric constant, V the applied voltage and V_{bi} is the temperature dependent built–in potential given by [45]:

$$V_{bi} = \frac{kT}{q}\ln\left(\frac{N_A(T)N_D}{n_i^2}\right) \tag{3.16}$$

where q, k, T, N_D and n_i were defined earlier, and N_A is the temperature dependent acceptors density in the anode equal to the activated implanted *Al* density.

Assuming a weak temperature dependence of the ratio $W(0,T)/\tau_r(T)$ it follows that the main temperature dependence of $J_{F0,Area\_rec}$ of Eq. (3.9) is:

$$\begin{aligned} J_{F0,Area\_rec}(0,T) &\propto n_i(T) \\ &\propto \sqrt{T^{3/2}\cdot T^{3/2}}\cdot exp\left(-\frac{E_g(T)}{2kT}\right) \\ &\propto T^{3/2} exp\left(-\frac{E_g(T)}{2kT}\right) \end{aligned}$$

hence:

$$\begin{aligned} J_{F0,Area\_rec}(0,T)\ /\ T^{3/2} &\propto exp\left(-\frac{E_g(T)}{2kT}\right) \\ \ln\left(J_{F0,Area\_rec}(0,T)\ /\ T^{3/2}\right) &\propto -\frac{1}{2kT}\cdot E_g(T) \end{aligned} \tag{3.17}$$

Therefore in the frame of this ideal abrupt junction model for the recombination current, making a plot of the natural logarithm of the ratio $(J_{F0,Area\_rec}(0,T)\ /\ T^{3/2})$ versus $1/2kT$ and fitting the curve with a straight line, its slope gives the material energy gap. It means that to apply this model and to extract a reliable value of the recombination lifetime τ_r within the Space Charge Region (SCR), the slope obtained by linear fitting the plot of experimental data constructed by Eq. (3.17), must verify the above described condition, that is, must give the material energy gap.

The same reasoning applies to $J_{F0,Area\_diff}(0,T)$. In particular, starting from Eq. (3.10), assuming that $\sqrt{\frac{D_p}{\tau_p}}$ is proportional to $T^{\gamma/2}$ where γ is constant [45], the temperature dependence of $J_{F0,Area\_diff}(0,T)$ can be written as:

$$\begin{aligned} J_{F0,Area\_diff}(0,T) &\propto T^{\gamma/2}\cdot\left[T^{3/2}\cdot exp\left(-\frac{E_g(T)}{2kT}\right)\right]^2 \\ &\propto T^{\gamma/2}\cdot T^3\cdot exp\left(-\frac{E_g(T)}{kT}\right) \\ J_{F0,Area\_diff}(0,T)\ /\ T^3 &\propto T^{\gamma/2}\cdot exp\left(-\frac{E_g(T)}{kT}\right) \end{aligned} \tag{3.18}$$

Since the term $T^{\gamma/2}$ is weak compared to the exponential one, Eq. (3.18) can be rewritten as:

$$J_{F0,Area\_diff}(0,T) \,/\, T^3 \propto exp\left(-\frac{E_g(T)}{kT}\right)$$

and hence:

$$\ln\left(J_{F0,Area\_diff}(0,T) \,/\, T^3\right) \propto -\frac{1}{kT}\cdot E_g(T) \tag{3.19}$$

As discussed earlier for $J_{F0,Area\_rec}$, before applying this model to the diffusion current, the Arrhenius plot of experimental data must return the material energy gap.

Perimeter current density

As the diode emitters of this study have been doped by a selective area ion implantation process (see Chapter 2 for further details), a lateral bipolar junction surrounding the emitter over its thickness is present. This junction may contribute to the perimeter current component with a recombination and a diffusion current governed by Eqs. (3.7) and (3.8).

At the same time, this p–n junction crosses orthogonally the wafer surface (as shown in Fig. 3.1, region g–h), therefore perimeter current, governed by surface current, may be expected. This latter have an exponential-like dependence which can be modelled as [54][60]:

$$J_{F,Per}(V,T) = qs_p(T)L_s(T)n_i(T)\cdot exp\left(-\frac{qV}{2kT}\right) \tag{3.20}$$

where $s_p(T)$ is the surface recombination velocity and $L_s(T)$ is the surface diffusion length, both of these variables are dependent on the temperature (T). Extrapolating to zero-voltage the previous equation it follows:

$$J_{F0,Per}(0,T) = qs_p(T)L_s(T)n_i(T) \tag{3.21}$$

A weak temperature dependence of the product $s_p(T)L_s(T)$ is expected, therefore the temperature dependence of the perimeter saturation current is determined by that of

the intrinsic carrier density:

$$\begin{aligned} J_{F0,Per}(0,T) &\propto n_i(T) \\ &\propto T^{3/2} \cdot exp\left(-\frac{E_g(T)}{2kT}\right) \end{aligned}$$

and hence:

$$\begin{aligned} J_{F0,Per}(0,T) \,/\, T^{3/2} &\propto exp\left(-\frac{E_g(T)}{2kT}\right) \\ \ln\left(J_{F0,Per}(0,T) \,/\, T^{3/2}\right) &\propto -\frac{1}{2kT} \cdot E_g(T) \end{aligned} \tag{3.22}$$

As discussed earlier for the area current density, making an Arrhenius plot of experimental data by using Eq. (3.22) if the resulting curve is a straight line with a slope equal to the material energy gap, reliable values of the product $s_p L_s$, which is considered as a quality factor of surface passivation, can be obtained from Eq. (3.21).

Reverse area current

The reverse area current density $J_{R,Area}(V,T)$, as in the forward case, can be expressed as a sum of generation and diffusion currents [45]:

$$J_{R,Area}(V,T) = J_{R,Area\_gen} + J_{R,Area\_diff} \tag{3.23}$$

where in Eq. (3.23):

$$J_{R,Area\_gen}(V,T) = \frac{qW(V,T)n_i(T)}{\tau_g(T)} \tag{3.24}$$

$$J_{R,Area\_diff}(V,T) = q\sqrt{\frac{D_p(T)}{\tau_p(T)}} \cdot \frac{n_i^2(T)}{N_D} \tag{3.25}$$

in Eq. (3.24) $\tau_g(T)$ is the generation lifetime of carriers within the SCR, the other variables in Eqs. (3.24) and (3.25) were previously defined.

In the case of semiconductor with small values of intrinsic carrier density $n_i(T)$ (such as Silicon Carbide) the diffusion current component will be necessarily negligible compared to the generation one, therefore:

$$J_{R,Area}(V,T) \approx J_{R,Area\_gen}(V,T) \approx \frac{qW(V,T)n_i(T)}{\tau_g(T)} \tag{3.26}$$

Under the hypothesis of abrupt junction (as supposed so far), the depletion layer width $W(V,T)$ can be expressed by using Eq. (3.15) obtaining:

$$J_{R,Area\_gen}(V,T) \approx \frac{qn_i(T)}{\tau_g(T)} \cdot \sqrt{\frac{2\varepsilon_0\varepsilon_r}{qN_D} \cdot (V_{bi}(T) - V)} \tag{3.27}$$

This equation shows that this ideal model can be used for representing the experimental data only if:

$$J_{R,Area\_gen}(V,T) \propto V^{1/2} \tag{3.28}$$

3.3.2 Calculated constant values

The constant values, used for the calculation of described variables in the previous section, are reported in Table 3.1.

In this study N_D is equal to the N^- donor density of the epitaxial layer, as this concentration is low ($3 \times 10^{15} cm^{-3}$) even at Room Temperature all donors are fully ionized, as shown, as an example, in Fig. 3.9 for 6H–SiC.

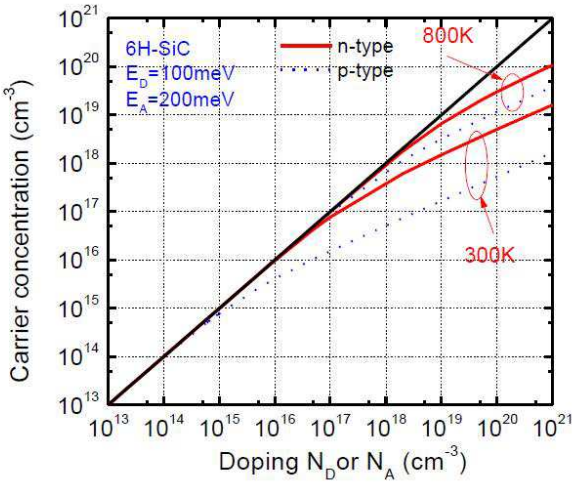


Figure 3.9: Example of dopants partial ionization at different temperatures in the case of 6H–SiC material.

The hole density $N_A(T)$ in the anode is a function of temperature and is plotted in Fig. 3.10. This latter figure was obtained from literature data of Hall-effect measurements for the same implantation process and electrical activation thermal treatment of the studied diodes [49].

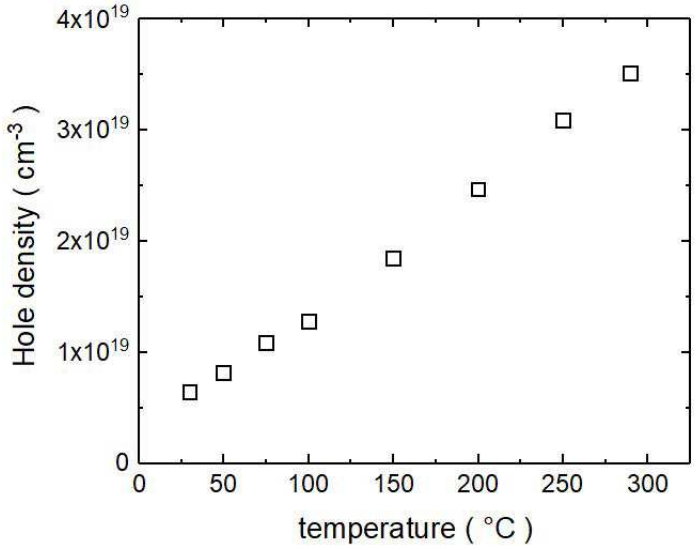


Figure 3.10: Experimental hole density as a function of temperature.

3.3.3 Data analysis and experimental results

Figure 3.11 depicts, as an example, the area (black square) and perimeter (red circle) current densities at a fixed temperature of 250°C. The black and red dashed lines represent the extrapolation to zero–voltage of the area and perimeter current density curves, respectively, with ideality factor $n = 2$.

This extrapolation procedure was applied to all curves at all temperatures. The so obtained set of recombination saturation currents ($J_{F0,Area\_rec}(0,T)$ and $J_{F0,Per}(0,T)$) were studied following the methodology discussed in Section 3.3.1 for the area and perimeter currents. In particular, for applying the abrupt junction model, the Arrhenius plot of the saturation currents of the curve trait with $n = 2$ must give the energy

PHYSICAL CONSTANTS

Parameter	Symbol	Value		Ref.
Electron charge	q	1.602×10^{-19}	[C]	[45]
Electron rest mass	m_0	9.1095×10^{-31}	[kg]	
Boltzmann constant	k	1.381×10^{-23}	[J/K]	
		8.617×10^{-5}	[eV/K]	
Permittivity in vacuum	ε_0	8.854×10^{-14}	[F/cm]	
Plank constant	h	6.626×10^{-34}	[J s]	
		4.136×10^{-15}	[eV s]	
PROPERTIES OF 4H-SIC				
Conduction Band Minima	M_c	3	–	[61]
Energy Gap (4K)	$E_g(4K)$	3.265	[K]	
α	α	6.5×10^{-4}	[eV/K]	
β	β	1.3×10^{3}	[K]	
Dielectric constant	$\varepsilon_r/\varepsilon_0$	9.66	–	
e_{DOS} Mass	m_{de}/m_0	0.42	–	[62]
h_{DOS} Mass	m_{dh}/m_0	2.6	–	

Table 3.1: Physical constant and 4H-SiC material properties used in calculations.

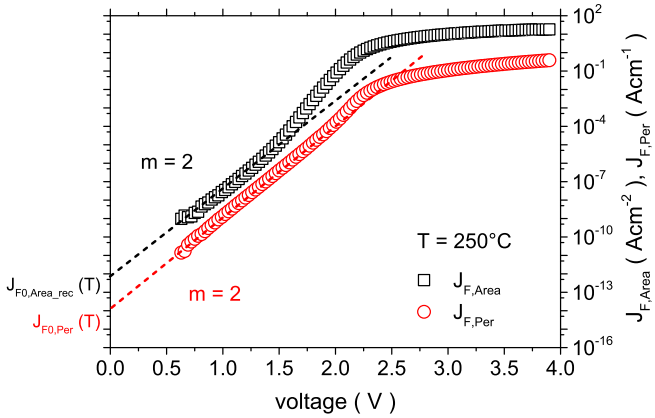


Figure 3.11: Area (black square) and perimeter (red circle) current densities at 250°C. The dashed curves shows the extraction procedure for obtaining the saturation currents.

gap of the 4H-SiC.

Fig. 3.12 depicts the Arrhenius plot of Area and Perimeter saturation currents. The obtained activation energy ($1.65 \pm 0.03eV$), for both perimeter and area currents, is very close to the half energy band–gap of 4H-SiC. In the case of the Area current density this result allows to use the ideal abrupt junction model for representing the experimental data with $n = 2$.

This latter result is relevant because an ion implanted p–n interface, such as that of the studied diodes, is never abrupt overall in SiC devices [63]. In the case of perimeter current this result may have two different interpretations. In particular, $J_{F,Per}(V,T)$ might be treated either as an area or as a surface current, as discussed earlier.

Area current density

For studying the recombination area current density, the ideal abrupt junction model of Eq. (3.9) was used. Fig. 3.13a shows the Arrhenius plot of the ratio $W(0,T)/\tau_r(T)$. As expected, this latter ratio has a weak temperature dependence. This result together with that showed in Fig. 3.12 support the hypothesis that $J_{F,Area\_rec}(V,T)$ can be

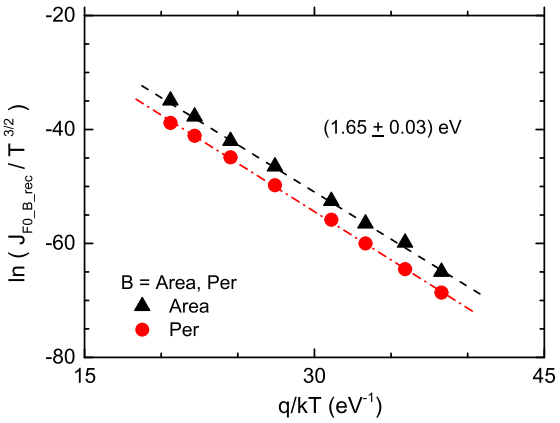
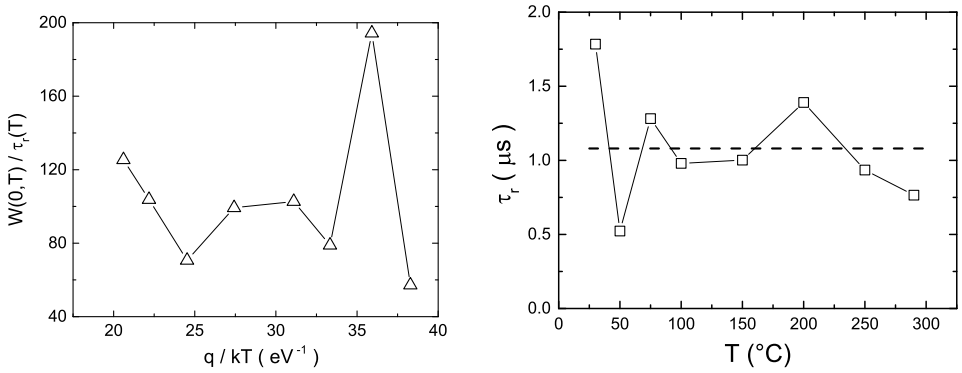


Figure 3.12: Arrhenius plot of Area (black triangles) and Perimeter (red circle) saturation current densities.



(a) (b)

Figure 3.13: (a) Temperature dependence of the ratio between the space charge region at zero saturation voltage ($W(0,T)$)and the recombination lifetime ($\tau_r(T)$). (b) Recombination lifetime vs temperature.

modelled as a recombination current.

Fig. 3.13b shows the estimated recombination lifetime τ_r within the SCR versus the temperature. The computed values are of the order of about $1.1\mu s$.

A curve trait with $n = 1$ may be found before ohmic regime, if the bulk diffusion current becomes dominant on the recombination one. When this condition in not fulfilled the ideality factor n has a value between 1 and 2 [45]. In this latter case,

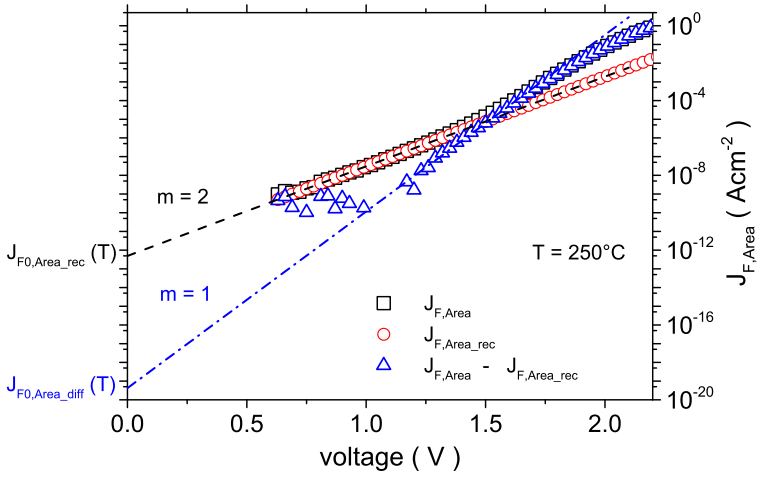


Figure 3.14: Graphical procedure for obtaining the diffusion current. The area recombination current desnity (red circle) is subtracted from the total area current density (black square) and the diffusion current density (blue triangle) is obtained.

diffusion and recombination currents might be comparable and the trait of curve with $n = 1$ might be recognized by using a graphical approach. Fig. 3.14, as an example, shows the graphical procedure for isolating the diffusion current component. In particular, by extrapolating the recombination current to higher voltages (red open circles in Fig. 3.14), by using Eq. (3.7), and subtracting it from the total Area current density (black open squares in Fig. 3.14), the diffusion component $J_{F,Area\_diff}(V,T)$ was obtained (blue open triangles in Fig. 3.14). As shown in the figure, at low voltages the current with $n = 2$ due to the recombination within the SCR controls the curve. At higher voltages the diffusion current is significant for a limited voltage

ranges before the ohmic conduction starts dominating the last part of the curve. By this procedure a set of diffusion saturation current $J_{F0,Area\_diff}(0,T)$ was obtained for each temperature.

In figure 3.15, the Arrhenius plot of the so obtained diffusion saturation currents, is depicted. The extracted activation energy of $2.77 \pm 0.04eV$ is too far from the en-

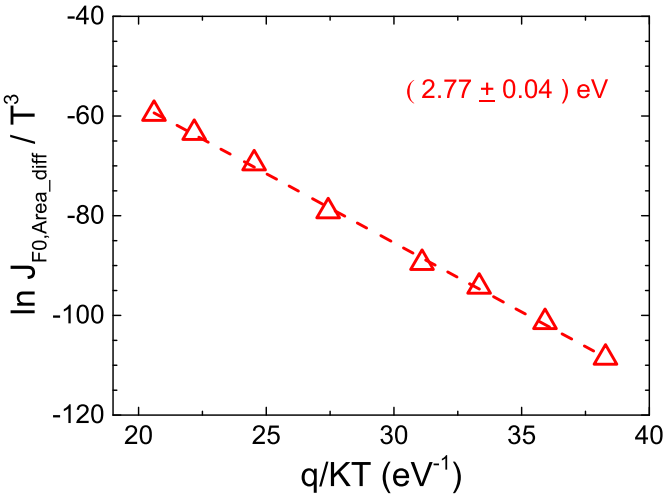


Figure 3.15: Arrhenius plot of the diffusion current component.

ergy band–gap of 4H-SiC to conclude that the exponential dependence in Eq. (3.17) is dominant. This rules out the possibility to use Eq. (3.10) for an estimation of the minority carrier lifetime τ_p in the drift layer. Even if the ideal abrupt junction model cannot be applied to all current components, the separation of perimeter and area current densities has allowed to observe that traits of the forward current of 4H-SiC $p^+ - i - n^-$ diodes can be described as the sum of two exponential current contributions with ideality factor $n = 2$ and $n = 1$, plus the ohmic region contribution.

Perimeter current density

As observed earlier, the result shown in Fig. 3.12 may have two interpretations. In particular the perimeter component may be treated as:

- an area current and studied by using the equations Eqs. (3.7) and (3.8);
- a perimeter current and studied by using Eq. (3.20).

In the first case the evaluation of $\tau_r(T)$ requires the knowledge of the lateral extension width of the SCR region adjacent to the emitter perimeter (i.e. the length of the segment a–h relative to SCR IV in Fig. 3.1). Since it was not possible to estimate it, the hypothesis of modelling the perimeter current by using Eq. (3.7) was not considered. Moreover, applying the graphical procedure showed in Fig. 3.14, the trait with ideality factor $n = 1$ was not observed. For this two reasons, $J_{F,Per}(V,T)$ in this study was treated as a surface current and the surface quality factor (i.e. the product $s_p(T)L_s(T)$) was calculated.

Fig. 3.16 represents the product $s_p(T)L_s(T)$ as a function of temperature. It can be

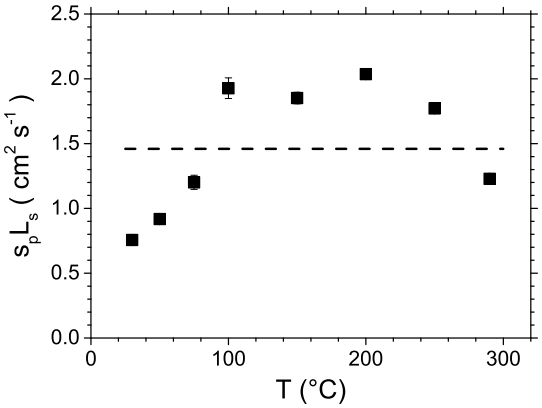


Figure 3.16: $s_p(T)L_s(T)$ quality factor vs temperature. The dashed line represents the average value.

state that, as expected, the temperature dependence is weak. The value of the product $s_p(T)L_s(T)$ is often used for qualifying the surface passivation, more precisely lower values of this product imply better surface passivations. Since the diodes of this study have no intentional surface passivation, the curve of Fig. 3.16 qualifies the passivation due to the native oxide, or oxy-carbide, that spontaneously forms on the 4H-SiC wafer surface when it is exposed to air. These values are two order of magnitude lower than

those published for mesa 4H-SiC p–i–n diodes [54]. This is promising for the use of selected area ion implantation technology for the fabrication of SiC bipolar junctions.

Reverse current density

Unfortunately, the reverse area current densities showed in Fig. 3.8 have a V–dependence steeper than the $V^{1/2}$ expected in case of a pure generation current and therefore the simple model of abrupt junction cannot be used for representing the experimental data. Nevertheless, under the hypothesis that this current might be dominated by carrier emission from traps within the depleted region, the temperature dependence might be determined by the trap emission rate [64]:

$$J_{R,Area}(V,T) \propto T^2 exp\left(\frac{-E_{na}}{kT}\right) \tag{3.29}$$

where E_{na} is a trap signature. Passing through the natural logarithm it follows that:

$$\ln\left(J_{R,Area}(V,T)/T^2\right) \propto \frac{-E_{na}}{kT} \tag{3.30}$$

Fig. 3.17 shows the Arrhenius plot of $J_{R,Area}(V,T)/T^2$ for $V = -100,\ -190V$. Within errors, the two curves can be fitted by activation energies of $0.20 + 0.02eV$ at low T and of $0.49 + 0.06eV$ at high T.

As the two reverse bias values show identical trap signatures, the hypothesis that trap distribution over the depleted depth is uniform may hold. The trap signature of Eq. 3.29 is connected with but does not exactly corresponds to the trap energy position in the band gap. In order to validate this extraction procedure E_{na} has been compared with the trap signature obtained by other electrical characterization techniques, such as deep level transient spectroscopy (DLTS).

The electrically active defects in diodes of this study have been identified by DLTS and the results are reported in [43]. Three electron traps were found, in particular: $EH6/7$ at $(Ec-1.5)eV$, $Z1/2$ at $(Ec-0.67)eV$, and $X1$ at $(Ec-0.16)eV$, plus a hole trap $X2$ at $(Ev-0.35)eV$.

$Z1/2$ and $EH6/7$ are traps associated with the presence of carbon vacancies V_C while $X1$ is systematically present in n–type 4H-SiC and may be due to metal impuri-

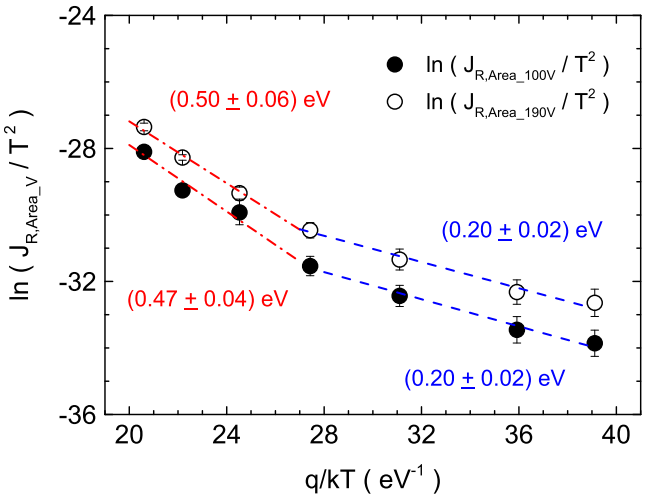


Figure 3.17: Arrhenius plot of the reverse area current density at two different bias voltage: $-100V$ (black full circle) and $-190V$ (black open circle).

ties [65]. The high density of V_C defects in the drift layer of diodes of this study is due to the very high temperature of the post–implantation annealing process [43][66][67].

The trap signatures showed in Fig. 3.17 and those of $Z1/2$ and $X1$ defects identified by DLTS are in good agreement, while the very deep trap responsible of the recombination current is likely to be the $EH6/7$ trap [68][69], and it was observed in forward study (Fig. 3.12).

3.4 Numerical simulations

3.4.1 Motivations

Numerical simulation of forward characteristics of the studied diodes has been performed by using Synopsys Sentaurus TCAD [70] with the aim to explain the origin of perimeter current.

The experimental activation energies, obtained from forward and reverse curve analysis (see Section 3.3), were used and their effect on the area and perimeter current

components was also studied.

Since, the previous performed analysis of experimental current–voltage curves gives only the distance of defects within the band–gap from one of the edge band, for classifying defects in terms of capture cross section, defect densities and type, the support of other measurement techniques is needed. Therefore, Deep Level Transient Spectroscopy (DLTS) measurements [43] were also performed on the studied diodes as already reported at the end of the previous Section. These results are in agreement with those present in literature for other ion implanted 4H–SiC devices. Therefore, the available capture cross sections and defect densities of DLTS study were used as input parameters within Sentaurus TCAD. The missing information can be considered as an original results used for fitting the area and perimeter forward curves of the studied 4H–SiC devices.

This procedure, which involves detailed electrical measurements and data analysis, combined with appropriate literature results (for obtaining the missing information from the electrical curves analysis), allows, in first approximation, the creation of models which may be used to explain not considered effects speeding up and improving design and fabrication of new devices.

3.4.2 Used models and simulation parameters

Simulations are based on the solution of well–known stationary drift–diffusion equations including models for incomplete ionization of dopants [71] and band–gap narrowing [72]. Physically based models for Shockley-Read-Hall (SRH) and Auger [73] recombination are used as well, even if, under the operating conditions of interest, SRH recombination is dominant and Auger recombination negligible.

Electron and holes mobilities are modelled by the empirical relation of Caughey–Thomas with the fitting parameters for SiC taken from [74]. All simulations have been performed at Room Temperature (RT). The fundamental 4H–SiC parameters used in all simulations are listed in Table 3.2.

The cylindrical symmetry of the diodes (see Fig. 3.18) allows limiting the simulated area to half of the cross–section on a symmetry plane and calculating the 3D current in a post–processing step thanks to the cylindrical option available in Syn-

opsys tool [70]. The modelled structure is the section inside the black frame in Fig. 3.18.

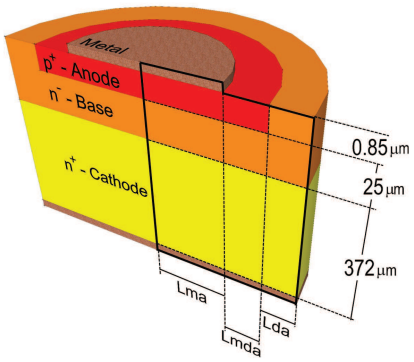


Figure 3.18: 3D cross–section of simulated diodes.

While the n^- and n^+ regions have a constant doping of $3 \times 10^{15} cm^{-3}$ (see Chapters 2 and 3 for details) and $7 \times 10^{18} cm^{-3}$ (corresponding to $0.021 \Omega cm$ resistivity) respectively, the anode acceptor doping is variable with depth. Fig. 3.19 shows the Al^+ acceptor depth profile with the corresponding hole distribution at RT; the former has been computed taking into account the implanted Al depth profile simulated by SRIM2008 [30] and an electrical activation of 80%, the latter by Synopsys-Sentaurus TCAD, which accounts for the temperature dependence of the partial ionization of the Al acceptors in 4H–SiC. In the light of the net donor density in the n–epilayer, the metallurgic p–n junction of diodes of this study falls at a depth of about 0.85 μm.

3.4.3 Simulation results

Area current density

In order to obtain the area current density, the ideal device with $L_{ma} + L_{mda}$ section (Fig. 3.18) was simulated and the effect of single traps on the electrical characteristics were studied. As explained in the introduction, type and density of defects used in the SRH model are based on DLTS study, while the used trap activation energies E_{A1},

4H-SIC SIMULATION PARAMETERS AT $T_0 = 300K$

Parameter	Symbol	Value		Ref.
Energy gap	E_g	3.2	[eV]	[45]
Electron affinity	χ	4.1	[eV]	
Dielectric constant	$\varepsilon_r/\varepsilon_0$	9.66	–	
e_{DOS} Mass	m_{de}/m_0	0.42	–	[62]
h_{DOS} Mass	m_{dh}/m_0	2.6	–	
DOPANT INCOMPLETE IONIZATION: MAXIMUM IONIZATION ENETRGY				
Aluminum	Al	0.265	[eV]	[71]
Nitrogen	N	0.05	[eV]	[75]
CAUGHEY–THOMAS MODEL FOR MOBILITY DOPING DEPENDENCE				
	electron	hole		
μ_{max}	954	120	[cm^2/Vs]	[74]
μ_{min}	0	15.9	[cm^2/Vs]	
$N_{ref} \times 10^{17}$	1.28	18	[cm^{-3}]	
a	0.61	0.65	–	

Table 3.2: Simulation parameters used for modelling 4H-SiC material.

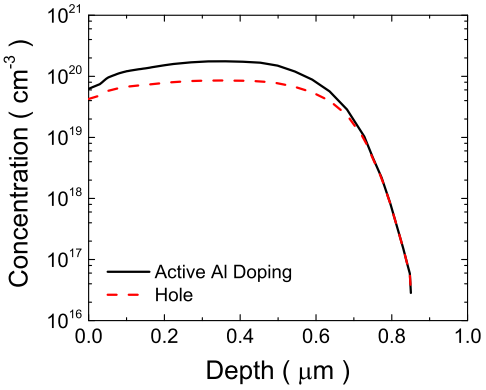


Figure 3.19: Active implanted Aluminum density versus depth obtained as the 80% of SRIM2008 simulated profile (dark solid line), emitter hole concentration versus depth simulated by Synopsys-Sentaurus TCAD (dashed red line).

E_{A2} and E_{A3} were those extracted from the experimental data analysis showed in the previous chapter. Table 3.3 summarize trap properties used in simulations.

DEFECT PROPERTIES

Defect	Position [eV]	type	τ_e [ns]	τ_h [ns]
L1	$E_C - 1.65$	donor	12	20
L2	$E_C - 0.2$	acceptor	420	10
L3	$E_C - 0.5$	acceptor	8	100
thermal velocity, v_{th} - electrons: $1.9 \times 10^7 cm/s$, *holes:* $1.2 \times 10^7 cm/s$				

Table 3.3: Defect properties used in simulations.

Fig. 3.20 shows simulation results, in particular: the solid line is the simulation which takes into account all traps, the dotted line is the simulation without traps and the other dashed lines are simulations with single traps. The experimental area current density (see section 3.2) is represented with open symbols. This graph shows

the effect on the total current of each single trap.

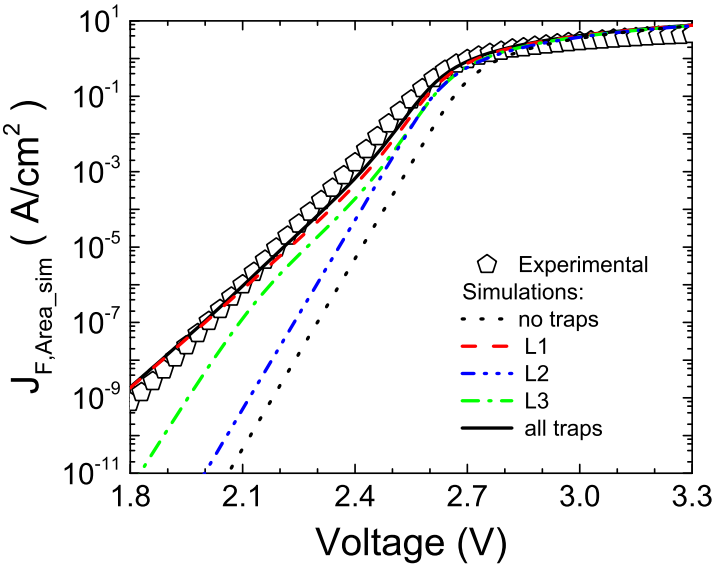


Figure 3.20: Open black squares represent the experimental data, black solid line show the simulated area current density taking into account all traps, while the black dot line show the ideal area current density (no traps). The other curves represent the contribution to the total simulated area current density of the single traps listed in table 3.3.

The level L1 can be identified with $EH6/7$ defect that originates from a carbon vacancy [76][77]. In the proposed model this defect is a donor, uniformly distributed in the diode's volume and positioned at $E_{A1} = 1.65eV$ under the conduction band edge [68][43]. Its concentration, taken from DLTS measurements [43], is $N_{T1} = 2.4 \times 10^{14} cm^{-3}$. The $EH6/7$ level controls the carrier lifetime in p–type 4H–SiC [78] and therefore doping–concentration–dependent SRH carrier lifetime for this defect is considered, which is calculated as:

$$\tau_{L1} = \frac{\tau_0}{1 + \left(\frac{N_{Al}}{N_{Ref}}\right)^{\gamma}} \tag{3.31}$$

where $N_{Ref} = 5 \times 10^{18} cm^{-3}$, $\gamma = 1.2$ and N_{Al} is the implanted Aluminum concentra-

tion. As in [78] and [43], $\tau_0 = 20ns$ is assumed for holes, while for electrons $\tau_0 = 12ns$ is based on DLTS data [43].

Level L2 has been tentatively attributed to a residual impurity of a transition metal like Ti or Cr, commonly observed in 4H-SiC [65]. Traps located at $E_C - 0.16eV$ and $E_C - 0.18eV$ are assigned to Ti [65][69], while a trap located at $E_C - 0.17eV$ is attributed to Ti or Cr [79]. However, this trap has an acceptor–like behaviour. The trap concentration and electron capture cross section lie in the ranges $10^{13} - 10^{14}cm^{-3}$ and $8 \times 10^{-16} - 2 \times 10^{-14}cm^2$ [69][80][81], respectively. Referring to the DLTS data [43], concentration $N_{T2} = 4.2 \times 10^{13}cm^{-3}$ and electron capture cross section $\sigma_e = 3 \times 10^{-15}cm^2$ were fixed, while hole capture cross–section $\sigma_h = 2 \times 10^{-13}cm^2$ values gave the best match between measurements and simulations.

The Level L3 located around at $0.50eV$ above the valence band maximum has been observed by several groups and usually is identified as the Boron–related D–center [82][83][84][85]. However, considering that the Boron–related D–center has been mainly detected in p–type–grown or Boron–implanted devices, in this study it has been attributed to the $Z1/2$ centre as commonly observed by DLTS measurement on ion implanted diodes [2][3][43]. Therefore, the energy position of L3 is $0.5eV$ below the conduction band. Its concentration and electron capture cross section are: $N_{T3} = 4.2 \times 10^{14}cm^{-3}$ and $\sigma_e = 1.8 \times 10^{-14}cm^2$, respectively [43]. The corresponding hole capture cross–section was fixed at $2 \times 10^{-15}cm^2$.

Perimeter current density

Taking into account all defects used in the previous section (listed in Table 3.3) for reproducing the area current density, simulations on diodes with different diameter (as listed in Table 3.4) were performed in order to explain the origin of the experimental perimeter current density.

For taking into account the periphery of diodes, With respect to the previous ideal simulation, the $L_{ma} + L_{mda} + L_{da}$ section (Fig. 3.18) was considered.

Fig. 3.21 shows the simulated current of the Diode labelled as B ($400\mu m$ diameter, see Table 2.1), in particular, as already seen for the area current density, the solid line is the simulation of the total current taking into account all traps, the dotted line

is the simulation without traps and the other dashed lines are simulations with single traps, while the experimental data are represented by open symbols.

SIMULATED DIODE CHARACTERISTICS

Diode	L_{ma} $[\mu m]$	L_{mda} $[\mu m]$	L_{da} $[\mu m]$	R_{D_anode} $[\Omega]$	$R_{D\_cathode}$ $[\Omega]$
A	55	20	50	1.9×10^{-3}	10^{-4}
B	175	25	50	7×10^{-3}	10^{-4}
C	475	25	50	4.5×10^{-2}	10^{-4}

Table 3.4: Geometrical characteristics of the simulated diodes and distributed resistance $R_{D\_anode/cathode}$ used for each diode.

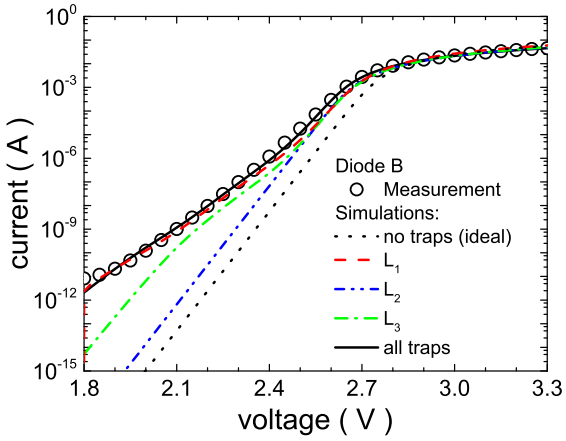


Figure 3.21: Simulation of the total current (black solid line) of the $400\mu m$ diameter diode (Diode B). The black open symbols are the experimental data.

In the case of diode B (Fig. 3.21) the simulation match the experimental data. Figs. 3.22 show the simulated total current for diodes A, B and C. No adjustment of simulation parameters was made from sample to sample: only the geometry was changed (see Tabele 3.4). The black dashed lines represent the simulated area current

considering the section $L_{ma} + L_{mda}$, the red dot–dashed lines are the total current without hypothesis on the surface next to the diode anode and considering the diode periphery (section $L_{ma} + L_{mda} + L_{da}$, Fig. 3.18). Finally, the blue solid lines represents the total simulated current obtained by using a model which accounts for periphery effects. This model will be detailed later on.

In Figs. 3.22 two different regions, divided by the dashed line, can be recognized: the region I at low voltages and the region II at high voltages.

In the case of larger diode C, the region II is completely controlled by the area current. In particular, as shown in Fig. 3.22c, the area (black dashed line) and total (red dot–dashed line) simulated currents overlap and both of them match the experimental data (open black triangles). Always considering Region II, in the case of diodes A and B, the only simulated area current (black dashed line) do not match the experimental data, as shown in Fig. 3.22a and Fig. 3.22b. The presence of diode periphery is necessary to reproduce the experimental data, indeed the total current, represented by the red dot–dashed line, match the experimental data (open black squares and circles). Furthermore, it is worth to highlight that the difference between the area simulated current (black dashed line) and the total simulated current (red dot–dashed line) decreases with the increasing of diode dimensions.

Observing region I, the simulated area current (black dashed line) fits the total simulated current (red dot–dashed line) for all diodes. Moreover, in diodes B and C the simulated area current also reproduces the measured current (symbols) quite well, whereas in diode A there are some discrepancies.

The fact that the simulated current at low voltages (region I) does not scale with the diode dimension suggests that some effects on the periphery of diodes are not accounted for in the simulation model. These effects are negligible in larger diameter devices and are more relevant for smaller diodes, indeed the low–voltage recombination current in the simulation for diode A is underestimated. This underestimation may be due to some inaccuracy of the surface modelling. The studied diodes have no intentional surface passivation but the presence of native oxide may be expected, as supposed in the previous Section 3.3.

The presence of a native oxide was taken into account by placing a negative fixed

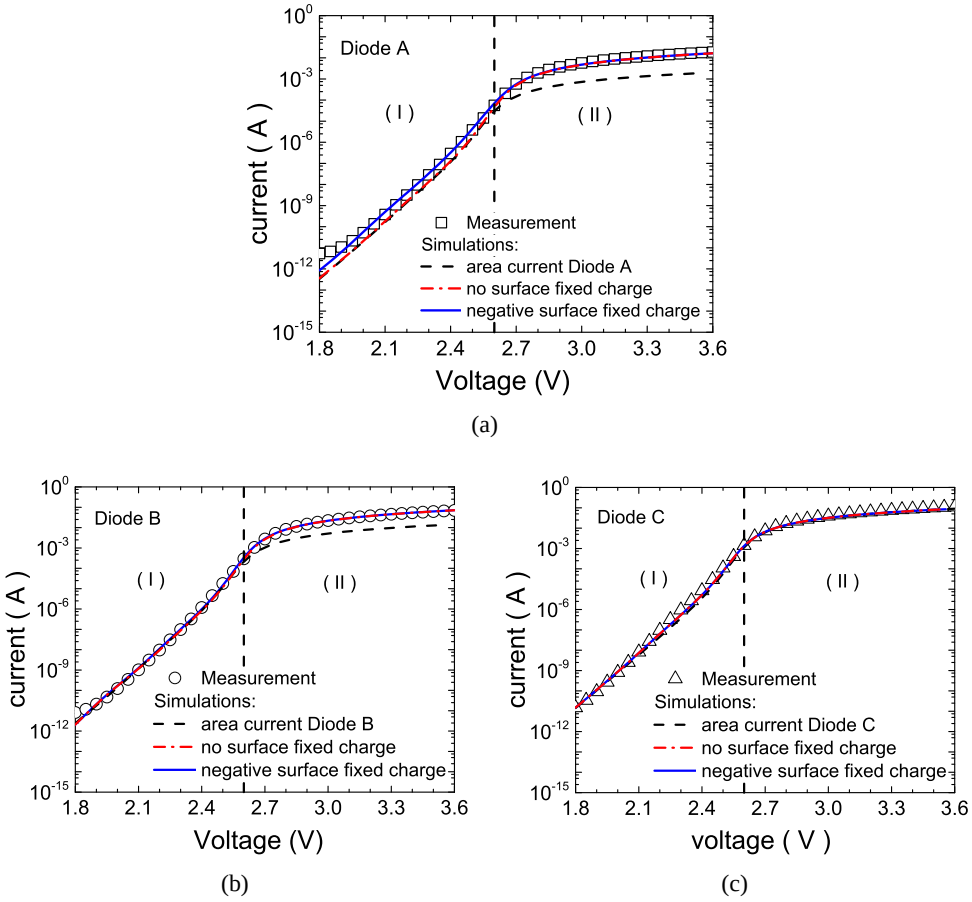
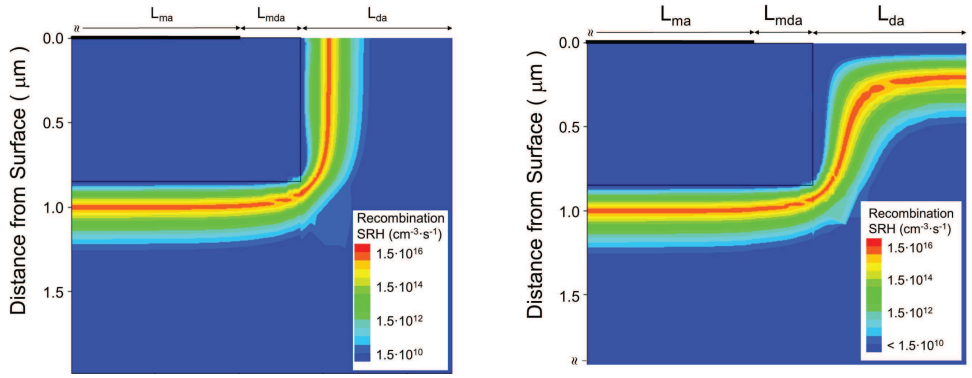


Figure 3.22: Simulation results for different diameter diodes, in particular: (a) small diameter diode A, (b) medium diameter diode B, (c) large diameter diode C. This figure shows that for smaller dimension diode the periphery is necessary to reproduce the experimental data (blue solid line).

charge of density Q_{fix} on the diode surface [86][87] that extends over the distance $L_{mda} + L_{da}$ (Fig. 3.18 and Fig. 3.1 for comparison with the model of Sha). The insertion of $Q_{fix}/q = -5 \times 10^{12} cm^{-2}$ increases the recombination current of diode A at low voltages and the simulation match the experimental curve (as shown in Fig. 3.22a, solid blue line). On the other hand, the insertion of this charge has negligible effects on the I–V characteristics of diodes B and C.

Figs. 3.23 shows the effect of negative fixed charge on the diode surface. In particular: the presence of Q_{fix} modifies the potential under the surface, attracting minority carriers (holes) towards the n–region and enlarging the space charge region over the L_{da} distance close to diode surface as shown in Fig. 3.23b (consistently with the Sha model explained in the previous section). The extension of SCR increases the recombination current at low voltages with respect to the case without surface fixed charge (Fig. 3.23a) where SCR surrounds the diode anode. As reported in Table 3.4, the region delimited by the distance L_da where the SCR extends, is comparable in size to the junction area only for the small diode A, while for the larger B and C diodes its contribution to recombination current is negligible. This explains why the effect of Q_{fix} vanishes when the diode diameter increases.



(a) (b)

Figure 3.23: SRH recombination rate within the Space Charge Region (SCR), (a) without any surface fixed charge and (b) with presence of surface fixed charge.

Finally, Fig. 3.24 shows the simulated perimeter current density component, obtained by subtracting the area current (black dashed line, Fig. 3.22) from the total current of smaller diode and divided for its area, both with (dot–dashed red line, Fig. 3.22) and without negative surface charge (blue solid line, Fig. 3.22): the simulated perimeter current is far from matching the experimental data (red open symbols) if the fixed negative charge is not considered (red dashed line).

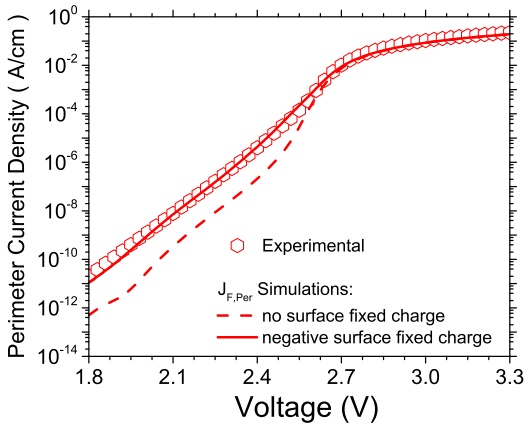


Figure 3.24: Simulation of the perimeter current density with (solid red line) and without (red dashed line) surface fixed charge (see text for details).

Chapter 4

Lifetime measurements in SiC devices

4.1 Motivations

Carrier lifetimes appear in all equations which model the current transport in bipolar semiconductor devices (see as an example Eqs. (3.7),(3.8),(3.24)) and heavily affect their performances. They are strictly connected to the presence of defects in the material and can give information about their densities [44]. Therefore, an accurate estimation of this parameter can help designers to improve manufacturing processes of devices and bulk materials.

4.2 Lifetime definition

Let consider a semiconductor in thermal equilibrium [88]; under this hypothesis the action mass law holds:

$$np = n_i^2 \tag{4.1}$$

where n and p are the free electron and hole concentrations, respectively, and n_i^2 is the intrinsic carrier concentration. When either injection or extraction of carriers occurs within semiconductor, the thermal equilibrium state is violated and the product

in Eq. (4.1) deviates its value from n_i^2. In particular: $np > n_i^2$ in case of injection and $np < n_i^2$ in case of extraction of carriers. The time period needed to restore the thermal equilibrium state of the semiconductor can be define as lifetime. This temporal parameter falls in two different categories: recombination and generation lifetimes. The former takes place when electron–hole pair annihilates to restore the thermal equilibrium after an injection of excess carriers ($np > n_i^2$). The latter takes place in the opposite case, that is, when electron–hole pair generates due to a paucity of carriers ($np < n_i^2$). When the recombination and generation mechanisms take place in the bulk of semiconductor the parameter $\tau_{r,g}$ indicates either recombination or generation lifetimes, whereas if these processes take place at the surface the quantity $s_{r,g}$ is used to indicate either surface recombination velocity or generation velocity.

4.2.1 Recombination lifetime

The recombination lifetime τ_r is a temporal parameter which is used to measure the amount of time necessary to restore the thermal equilibrium state when excess carriers are introduced by light or by forward biasing in a semiconductor or a p–n junction. Its estimation passes through the recombination rate R which has a non–linear dependence on the carrier concentrations, in particular:

$$R = A\Delta p(t) + B\Delta p(t)^2 + C\Delta p(t)^3 \tag{4.2}$$

where A, B and C are three proportionality constants and $\Delta p(t)$ is the excess carrier density which can be define as $\Delta p(t) = p(t) - p_0$ where p_0 is the carrier concentration density at equilibrium. Dividing Eq. (4.2) by $\Delta p(t)$ it follows:

$$\begin{aligned} \frac{R}{\Delta p(t)} &= A + B\Delta p(t) + C\Delta p(t)^2 \\ &= \frac{1}{\tau_{SRH}} + \frac{1}{\tau_{rad}} + \frac{1}{\tau_{Auger}} \\ &\equiv \frac{1}{\tau_r} \end{aligned} \tag{4.3}$$

Hence, the lifetime τ_r in Eq. (4.3) depends on three different mechanisms [89], schematically illustrated in Fig. 4.1 and described below:

1. the well–known Shockely-Read-Hall (SRH) recombination (Fig. 4.1a) [90][91] defined by τ_{SRH} which is independent from the carrier concentration and is dominant in indirect band–gap semiconductor;

2. the radiative or band–to–band recombination (Fig. 4.1b) defined by τ_{rad} which is inversely dependent on the carrier concentration and is dominant in direct band–gap semiconductors;

3. the Auger or three–carrier recombination (Fig. 4.1c) defined by τ_{Auger} which is inversely dependent on the square of carrier concentration and therefore is dominant in case of high doping or high injection condition.

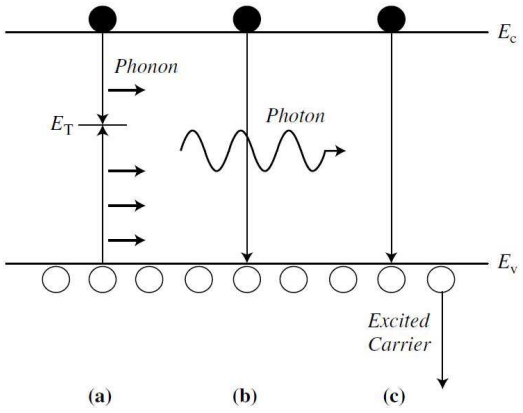


Figure 4.1: (a) SRH, (b) radiative, (c) Auger recombination mechanisms.

4.2.2 Generation lifetime

The generation lifetime τ_g is the counterpart of recombination one. In particular is a temporal parameter which is used to measure the amount of time necessary to generate an electron–hole pair (ehp) in case of paucity of carriers, for example within the SCR in a reverse biased junction. Its estimation passes through the generation rate G which is the opposite of recombination rate:

$$G = -R$$

In particular, the inverse process of:

1. SRH recombination is the thermal generation. This mechanism depends on the sample temperature and is due to the breaking of chemical bonds which liberate electrons generating an ehp.

2. Auger recombination is the impact ionization generation or avalanche multiplication. This process occurs if the electric field in a reverse biased junction is high enough for accelerating carriers such that they can lift an electron by impact from valence into the conduction band.

3. Radiative recombination is the optical generation. In this process a photon with an energy $E = hf$, where h is the Plank constant and f is the frequency, can be absorbed within the SCR generating an ehp.

4.2.3 Continuity equation for Generation/Recombination processes

In a semiconductor at thermal equilibrium, electron–hole pairs continuously generate and recombine with the same rate. It means that in a time interval dt the net recombination rate given by the difference between thermal generation G_{th} and recombination R is null. In the macroscopic case it means that the variation of excess carriers is null, more precisely that the carrier concentrations is constant as a function of time:

$$\frac{d\Delta p(t)}{dt} = G_{th} - R = 0 \tag{4.4}$$

Eq. (4.4) define the steady-state condition of semiconductors, in particular when generation and recombination processes are balanced the material is in the steady-state condition. By rearranging and substituting Eq. (4.3) in Eq. Eq. (4.4), it yields:

$$\frac{d\Delta p(t)}{dt} = G_{th} - \frac{\Delta p(t)}{\tau_r} = 0 \tag{4.5}$$

The general equations described above are valid for electrons ($n(t)$) and holes ($p(t)$). Let consider an n-type semiconductor at thermal equilibrium without external stimuli, Eqs. (4.1) and (4.5) hold. If excess concentrations of minority carriers $p_n << n_0$

(low level injection) is produced by lighting the semiconductor, the new steady-state condition is given by:

$$\frac{d\Delta p(t)}{dt} = G - \frac{\Delta p(t)}{\tau_r} = 0 \tag{4.6}$$

where in this case $G = G_{th} + G_{light}$ and $\Delta p_n(t) = p_n(t) - p_{n0} = G_{light} \cdot \tau_r + p_{n0}$. If the light is suddenly turned-off at $t = 0$ Eq. (4.6) is modified as:

$$\frac{d\Delta p_n(t)}{dt} = -\frac{\Delta p_n(t)}{\tau_r} \tag{4.7}$$

Considering the boundary condition $p(t \to \infty) = p_{n0}$ and $\Delta p_n(0) = p_n(t) - p_{n0} = G_{light} \cdot \tau_r + p_{n0}$ the solution which gives the decay of excess carrier concentration as a function of time is:

$$p_n(t) = \Delta p_n(0) \cdot \exp^{-\frac{t}{\tau_r}} \tag{4.8}$$

4.2.4 Surface recombination velocity and surface recombination lifetime

Recombinations can occur at the surface of semiconductor, for example because of the presence of dangling bonds [88]. For this reason, the measured lifetime depends on both the bulk recombination lifetime τ_r and the surface recombination lifetime τ_s and its expression is given by:

$$\frac{1}{\tau_{r,eff}} = \frac{1}{\tau_{r,bulk}} + \frac{1}{\tau_s} \tag{4.9}$$

where $\tau_{r,eff}$ is the effective (as–measured) carrier lifetime, $\tau_{r,bulk}$ is the bulk recombination lifetime given by Eq. (4.3) and τ_s is the surface recombination lifetime.

4.3 Lifetime measurements

Several optical and electrical techniques can by used for measuring the carrier lifetimes in semiconductor devices [44]. However, because of the vertical structure of the studied devices, shown in Fig. 2.9, the optical techniques were excluded as the excess of carriers cannot be directly generated by lighting the base of diodes, where the

main recombination mechanisms take place. Among the electrical methods, the two most used are the Current Recovery Time (CRT or Reverse Recovery) and the Open Circuit Voltage Decay. Since, the reverse current of the measured diodes at RT is very low (see fig. 2.13) and even at high reverse voltage for smaller diodes might be lower than the detection limit of the measurement instrumentations (see as an example Fig. 3.6a), the OCVD technique was adopted for performing lifetime measurements on the PiN diodes of this study. Furthermore, in the case of SiC devices, this technique in more suitable and allows to extract reliable values of the carrier lifetime in the base of PiN diodes [92]. Compared to the well-known CRT or Reverse Recovery technique:

- all the generated excess carriers recombine spontaneously within the base; none are swept out by the applied reverse voltage;
- the experimental set–up is of easy implementation and reverse bias is not required.

4.3.1 Open Circuit Voltage Decay

The Open Circuit Voltage Decay working principle is very simple: carrier lifetimes can be evaluated by observing the open circuit voltage decay after suddenly switching off the forward diode current [44][93].

Fig. 4.2a depicts a schematic circuit for implementing the OCVD technique and Fig. 4.2b illustrates the possible voltage decays after opening the circuit.

This electrical method was firstly proposed for measuring the minority carrier lifetime in p–n junction [94]. In particular in [94] the effective minority carrier lifetime was linked to the voltage decay by the following equation:

$$\tau_{p,eff} = -\frac{kT}{q} \times \frac{1}{\frac{dV(t)}{dt}} \tag{4.10}$$

where in Eq. (4.10) k is the Blotzmann constant, T is the absolute temperature, q is the electron elementary charge and $dV(t)/dt$ is the slope of the linear part of voltage decay (Fig. 4.2b, ideal decay).

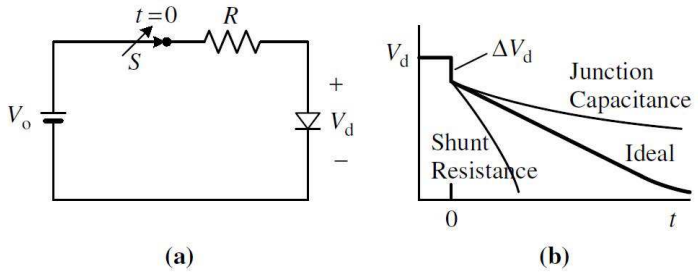


Figure 4.2: (a) Ideal schematic circuit for implementing the OCVD measurement technique, in this case the diode is forward biased with a voltage source. (b) Different voltage decays after switching off the diode.

The theory initially developed for measuring the minority carrier lifetime in a p-n junction, was later extended to the case of p–i–n devices for high injection level condition [95][96][97][98] for obtaining the effective ambipolar carrier lifetime. In this case Eq. (4.10) is modified as:

$$\tau_{amb,eff} = -\frac{2kT}{q} \times \frac{1}{\frac{dV(t)}{dt}} \tag{4.11}$$

In both Eqs. (4.10) and (4.11) the extracted value of τ is an effective recombination lifetime which follows the expression shown in Eq. (4.9).

Besides being used to estimate carrier lifetimes, this technique can also be used to approximatively evaluate the series resistance of junction devices. Indeed, the initial voltage drop (ΔV_d in Fig. 4.2b) is proportional to the series resistance of the measure junction devices [44][99].

4.3.2 Experimental setup

Fig. 4.3 depicts the block diagram of the experimental setup used in this work for performing OCVD measurements.

The Source Monitor Unit (SMU) Keithley 2400 was used to provide the bias current to the DUT (Device Under Test).

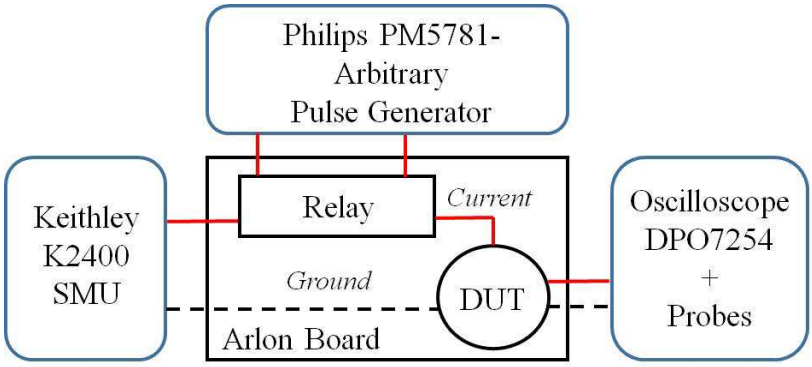


Figure 4.3: Schematic block diagram of the experimental set–up used for OCVD measurements. The central square block represents the PCB.

To separate the biasing unit from the DUT, the PCB (Printed Circuit Board) was equipped with a mercury wetted relay, as suggested firstly in [96][100] and later in [101], in particular with the model 200–1–A–5/6 of Pickering [102]. This kind of relay provides very low on-state resistance $R_{on} \approx 0.075\Omega$, an open circuit resistance greater than $10^{12}\Omega$ and a parasitic capacitance of about $5pF$ (as reported in the data–sheet).

For opening the contact within the relay the arbitrary pulse generator Philips PM5781 was used. The characteristics of the pulsed square signal were: amplitude 4 V, rise and fall time 2 ns (leading and trailing edges, respectively), duty cycle 50% and period 50 ms (20 Hz).

For reading the open circuit voltage decay, Tektronix passive (P6139A) and active (TAP2500) probes connected to the Tektronix Phosphorus Oscilloscope DPO7254 were used [103]. For minimizing parasitic contributions due to connections, the PCB is made on an Arlon board [104] and devices are placed very close each other on the board. Furthermore, SMA (SubMiniature version A) connectors are used to carry electrical signals from generator to the PCB.

4.3.3 Experimental set–up characterization

The first measurements were carried out with the aim to evaluate the parasitic elements of the circuit which might affect the OCVD measures. For this reason, a schematic model of the experimental set–up was developed and a comparison between theoretical calculation of the time constant τ_{RC} and its experimental evaluation was performed.

Fig. 4.4 shows the schematic circuit used for modelling the experimental set–up. The right hand side of this figure shows the subsystem formed by probes plus oscilloscope, in particular these two elements, used for reading the open circuit signal, were modelled by an input resistance (R_{in}) in parallel with an input capacitor (C_{in}). The values of these two parts depend on the properties of the used probes. The left hand side of Fig. 4.4 shows the subsystem formed by the switching element (labelled as relay), the DUT (Device Under Test) and the current source unit (I_{pol}). The relay's resistance is neglected because so high that, in first approximation, it cannot affect the circuit time constant, whereas its capacitance (C_{relay}) was taken into account because the value is comparable with that of C_{in}.

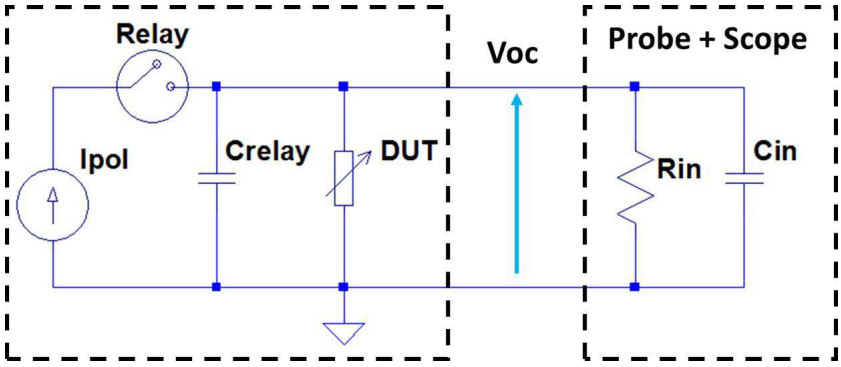


Figure 4.4: Schematic model of the experimental set–up used for evaluating the parasitic elements of the circuit.

The time constant τ_{RC} of the circuit, shown in Fig. 4.4, can be easily obtained as:

$$\tau_{RC} = (R_{in} \parallel R_{DUT}) \cdot (C_{in} \parallel C_{relay}) = R_{eq} \cdot C_{eq} \tag{4.12}$$

As described in the previous Subsection, two different kind of probes were used to read the voltage signal on the R_{DUT}, in particular:

- Tektronix passive (P6139A): characterized by an input resistance $R_{in} \approx 10M\Omega$ and by an input capacitor $C_{in} \approx 8pF$. Since this probe is made by passive elements is called passive probe.

- Tektronix active (TAP2500): characterized by an input resistance $R_{in} \approx 33k\Omega$ and by an input capacitor $C_{in} \approx 0.8pF$. Since this probe is made by active elements (i.e. semiconductors devices) is called active probe.

In this experiment in order to evaluate the τ_{RC} of the circuit, resistances of known values in the range $47 \div 10k\Omega$ were placed as a Device Under Test (R_{DUT}). Bias currents were chosen for keeping a voltage drop of almost $5V$ on the R_{DUT}. The time constant τ_{RC} was estimated as the time needed to pass from 90% to 10% of the voltage signal amplitude. Fig. 4.5 illustrates the measured voltage transient in the case of passive (Fig. 4.5a) and active probes (Fig. 4.5b). The limits mentioned above for estimating the 90% and 10% of the voltage amplitude are also shown by black arrows. In the case of active probes (Fig. 4.5b), the voltage scale was normalized to $5V$, while the different time scale with the respect to the case of passive probes (Fig. 4.5a) is due to the different characteristic between the two probes as discussed earlier.

In Figs. 4.5a and 4.5b, for high current, a typical under–damped response of an RLC circuit is observed in the voltage transient. Oscillations are due to parasitic inductances of connections. However this undesired effect, which is always present in real circuit, does not compromise the estimation of τ_{RC}. Table 4.1 reports the extracted value of τ_{RC} for the different values of R_{DUT} in both cases of active and passive probes. The used bias current values are also reported as I_{pol}.

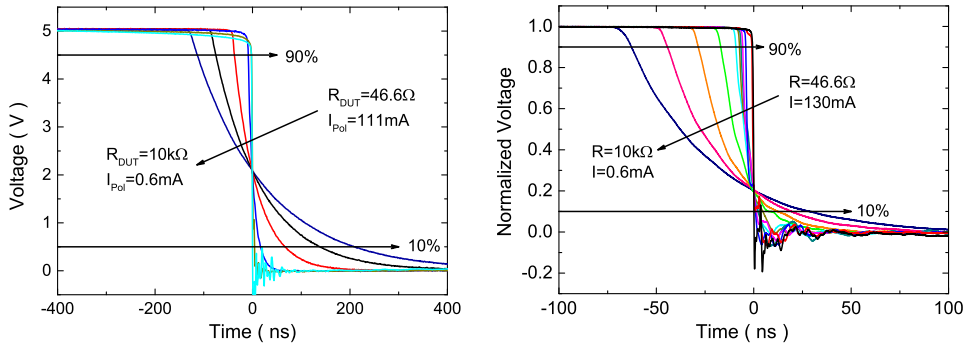
Taking into account that $C_{relay} = 5pF$, in the frame of the hypothesized model of Fig. 4.4, the expected value of C_{eq} should be about $13pF$ and about $6pF$, for passive and active probes, respectively.

Fig. 4.6a plots the experimental values of τ_{RC} versus the parallel between R_{DUT} and R_{in} (i.e. R_{eq}), in the case of active (red full circle) and passive probes (black

EXPERIMENTAL τ_{RC} VALUES

PASSIVE PROBE			
$R_{DUT}[\Omega]$	$R_{DUT} \parallel R_{in}[\Omega]$	I_{pol} [mA]	τ_{RC} [ns]
10000	9990	0.5	146.8
6740	6735	0.742	96.6
3260	3258	1.534	47.0
805	804.94	6.211	11.6
217	216.99	23.742	2.9
46.6	46.6	111	1.0
ACTIVE PROBE			
$R_{DUT}[\Omega]$	$R_{DUT} \parallel R_{in}[\Omega]$	I_{pol} [mA]	τ_{RC} [ns]
10000	8000	0.6	41.3
6740	5768	0.9	28.6
3260	3014	1.84	18.5
2174	2062	3	10.6
1184	1150	6.07	5.44
996	972	6.03	5.44
805	789	7.5	3.90
671	660	9	2.47
333	330	18.02	2.24
217	215	30	0.62
46.6	46.55	130	0.36

Table 4.1: Time constant values for different R_{DUT} in the case of passive and active probes. The bias current is also reported.



(a) (b)

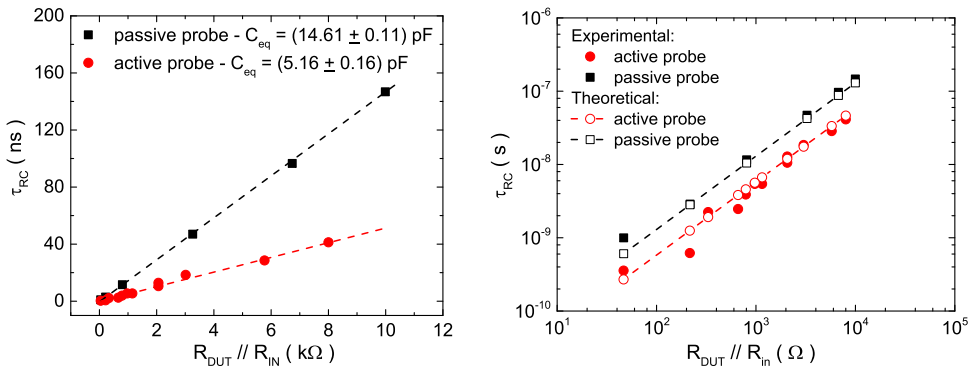
Figure 4.5: Voltage transient measured (a) with passive probe (b) with active probe by using different R_{DUT}.

full squares). The slope of the straight line with null intercept which fits the experimental data, returns the value of equivalent capacitance $C_{relay} \parallel C_{in} = C_{eq}$ of the circuit. In particular, $C_{eq} \approx 14.6pF$ and $C_{eq} \approx 5.2pF$ was extracted for passive and active probes, respectively. These values are very close to those expected following the model of Fig. 4.4.

Fig. 4.6b shows a cross–check between experimental data and theoretical calculations. With respect to the previous experiment, the experimental data (black solid square of passive probes and red solid circle for active probes) were fitted by using the expected values of C_{eq} ($13pF$ and $6pF$ for passive and active probes, respectively) in Eq. (4.12). In this plot the theoretical curves match the experimental data validating the hypothesized model.

The extracted values of τ_{RC}, reported in Table 4.1 and showed in Fig. 4.6, confirm that active probes may be suitable for detecting very quick transient.

However, with respect to passive probes, in addition to the lower input capacitance, the active probes feature a lower input resistance. Fig. 4.7 plots the computed R_{eq} versus the DUT resistance in the range $46 \div 10^7\Omega$, by using the R_{in} of either passive (black full squares) or active (red full circles) probes. The DUT resistance ranges from a minimum value that allowed to use each probe at its higher sensitiv-



(a) (b)

Figure 4.6: Experimental time constant τ_{RC} versus $R_{eq} = R_{DUT} \parallel R_{in}$, (a) experimental data are fitted for extracting the value of C_{eq}, (b) the experimental data are fitted by using Eq. (4.12) with expected values of C_{eq}.

ity and a maximum value that emulates the high increasing resistance of a p-n diode approaching the off-state.

In the case of passive probes R_{eq} is equal to the DUT resistance for a wider range of R_{DUT} values. In the case of active probes for R_{DUT} values higher than $10^4\Omega$, R_{eq} is lower than the corresponding DUT resistance and for $R_{DUT} = 10^6\Omega$ $R_{eq} = R_{in}$. Figure 4.7 shows that, depending on the used probes, there is always a limit DUT resistance value so that R_{eq} is almost equal to the DUT resistance which ensures to perform reliable measurements.

The characterization of the measurement circuit which implements the OCVD method pointed out that:

1. the parasitic capacitance of the relay C_{relay} is always present and cannot be avoided;

2. the large resistance of the relay does not affect the measurement;

3. parasitic inductances due to connections are present and their effect can be observed at very high current. However, these elements, always present in real

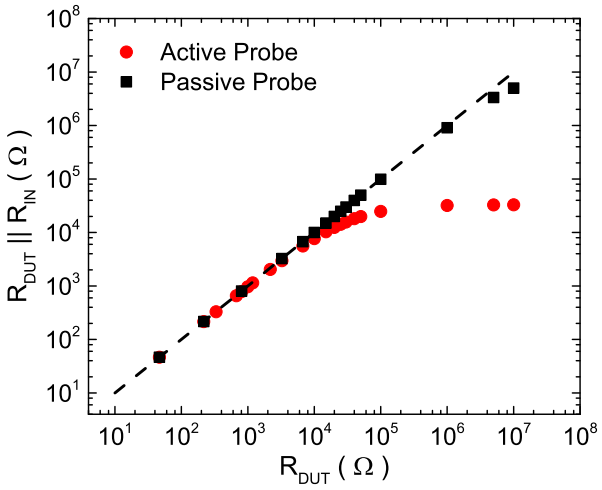


Figure 4.7: $R_{eq} = R_{DUT} \parallel R_{in}$ versus R_{DUT} by using R_{in} of either passive (black full squares) or active (red full circles) probes.

circuits, does not affect the measurement even if they can generate fluctuation of the voltage signal;

4. the choice of the probe for reading the voltage signal depends on the features of DUT and on the speed of transients.

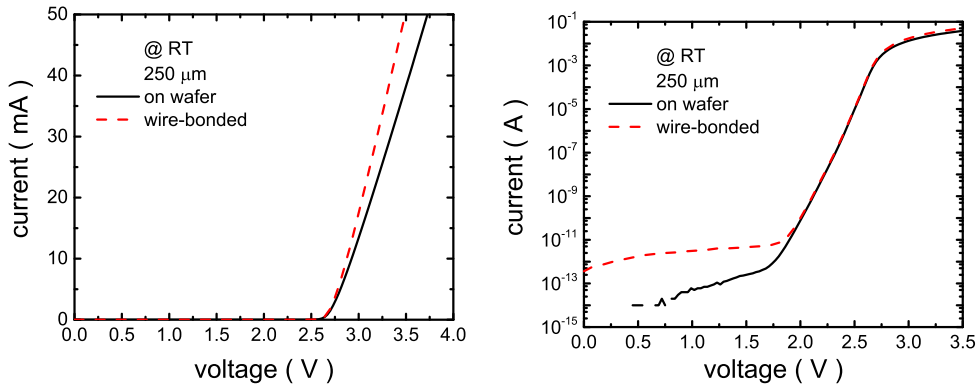
4.3.4 Measured devices

Devices measured by using OCVD technique are vertical 4H-SiC PiN implanted diodes manufactured at CNR-IMM of Bologna on n-type 4H-SiC epitaxial wafers targeted for 3000 V blocking voltage. In particular, devices belonging to the chip labelled L5 from diodes family SIC0303b were used. The precessing steps of these devices were described earlier in Chapter 2. The selection criteria of diodes used for OCVD measurements were the same adopted for the choice of devices for studying forward and reverse characteristics (Chapter 2).

Since these diodes were on a chip, like that showed in the bottom of Fig. 2.9, for connecting the sample on the PCB used in the OCVD measures (Fig. 4.3), Transistor

Outline packages model TO8–12 were used [105]. More precisely, the back of chip L5 was mounted on a TO package by using a conductive paste and the diode anodes were wire–bonded to its headers by using the digital wire–bonder model K&S 4523a [106].

Diodes with different anode dimensions were used for lifetime measurements, in particular, referring to Table 2.1, devices D1,D3,D6,D7 were mounted on TO package and wire–bonded. As an example, Fig. 4.8 illustrates a comparison between forward current–voltage curves before (black solid line) and after (red dashed line) wire–bonding process on a 250μm diameter diode (D1) in linear scale (Fig. 4.8a) and logarithmic scale (Fig. 4.8b).



(a) (b)

Figure 4.8: Experimental forward current–voltage curves of a 250μm diameter diode before (red solid line) and after (red dashed line) the wire bonding process.

These figures show that in the region of interest, where the trend is exponential, the electric characteristics, before and after the wire bonding process, overlap each other. In the very low voltage region the gap is due to the different experimental setup and therefore the instrumental current floor plays a major role. While in the linear part of the characteristic (ohmic region) the bonded diode offer a slightly lower series resistance. This check is necessary since wrong settings of ultrasonic bonding processes might damage the crystalline structure of materials generating undesidered

defects.

For checking whether the presence of the package might increase the parasitic capacitance of the measurement circuit, diodes capacitance–voltage (C–V) and capacitance–frequency (C–f) measurements under reverse voltage ($f = 100kHz$ and maximum $V_{rev} = -10V$) and at $0V$ at RT, respectively, were performed before and after mounting the sample by using an HP4284A LCR meter with a test signal amplitude of 15mV. No relevant differences of capacitance values were observed.

Referring to the schematic model of Fig. 4.4, when the DUT is substituted with a p–n junction, its resistance and capacitance vary, as a function of the voltage, during the transient subsequent to the opening of the circuit. Fig. 4.9 shows a new schematic representation of the experimental set–up which takes into account these capacitance and resistance variations by using a simple circuital model of the diode represented by the parallel between the differential resistance R_d and diffusion capacitance C_{diff}.

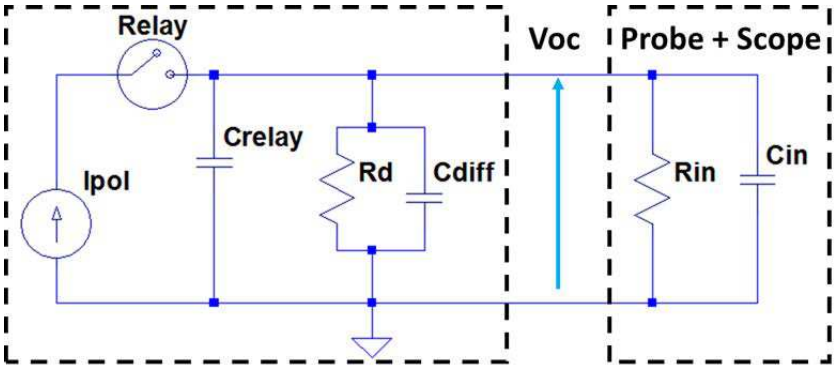


Figure 4.9: Schematic model of the experimental set–up considering a p–n junction as a DUT.

For SiC diodes of this study, R_d is of the order of few Ω before the opening of the circuit and increases during the voltage transient up to values larger than $10^{12}\Omega$. At the same time, C_{diff} is larger than any other capacitance in the system when diodes are in the on–state and decreases to values of few pF when the diodes are in the off-state. In the following section, the OCVD curves taken by using either passive or active probes for the above described SiC diodes will be shown and discussed. All

these measurements were performed at RT.

4.3.5 OCVD measurements and ambipolar lifetime extraction

Fig. 4.10a represents OCVD measurements on a $400\mu m$ diameter diode forward biased with a current of $50mA$. The measures were performed in two different conditions, in particular: by using passive probes (red solid line) and active probes (black solid line). In this figure (as also showed in Fig. 4.2b), two different trends can be recognized: i) the junction capacitance trend and ii) the shunt resistance trend. By using the configuration with passive probes for reading the voltage transient, the junction capacitance trend is evident and the decay is never linear, while in the case of active probes the shunt resistance trend is dominant meaning that the shunt resistor of the active probes is over–compensating the diode junction capacitance [107]. However, in this latter case, even if the voltage transient decays rapidly, a linear traits of the curve (which might approximate the ideal decay for few time constants) is present, as shown in the enlargement in Fig. 4.10b, and can be used for extracting the slope which can be used for computing the carrier lifetime by using Eq. (4.11).

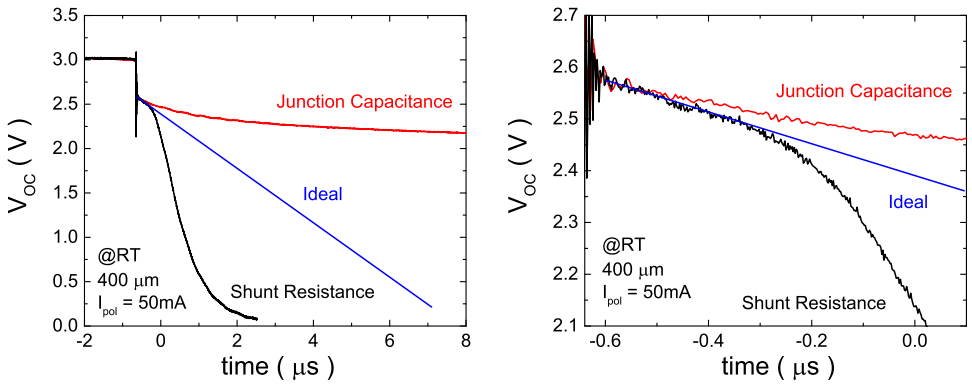


Figure 4.10: Experimental OCVD curves of a $400\mu m$ diameter diode measured by using either passive (red solid line) and active (black solid line) probes, the blues slid line represents the ideal trend by using a manual fitting.

For this reason, all OCVD measurements of this study were performed by using the configuration with active probes.

Fig. 4.11a depicts the OCVD measurements of a 250μm diameter diode performed by using active probes for different bias currents. The enlargement of Fig. 4.11b points out that:

- the higher the bias currents, the larger and less steep the initial linear traits before the shunt–resistance trend starts dominating. These variations indicate that the slope (and therefore lifetime for Eq. (4.11)) of the linear trait changes as a function of the injection level;
- the voltage after the switch opening (i.e. the voltage value after the voltage drop) saturates as explained in [108];
- as expected for increasing currents, the voltage drop ΔV increases being proportional to the series resistance of diode [99][44].

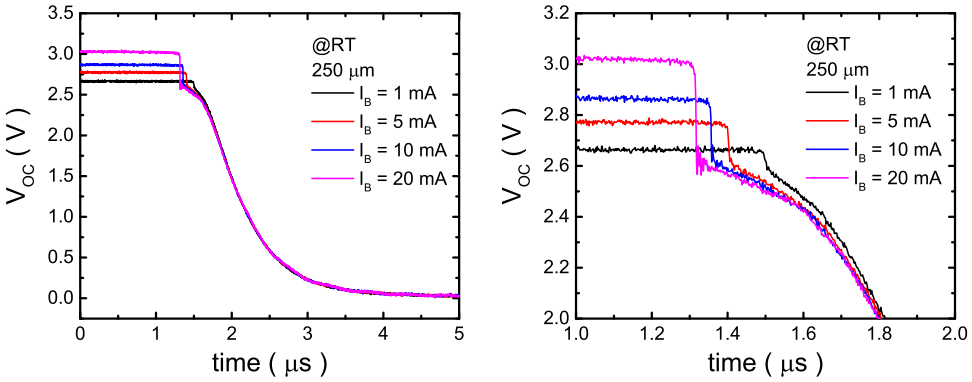


Figure 4.11: Experimental OCVD curves of a 250μm diameter diodes measured by using active probes for different bias currents.

The voltage limit after which the shunt–resistance trend dominates the transient decay may be evaluated starting from the model shown in Fig. 4.9. In particular,

considering that $R_{eq} = R_d \parallel R_{in}$ and $C_{eq} = C_{diff} \parallel C_{in} = C_{diff} + C_{in}$, it can be stated that $\tau_{circuit}$ may be modelled by the following simple equation:

$$\tau_{circuit} = (R_d(V) \parallel R_{in}) \cdot \left(C_{diff}(V) + C_{in}\right) \tag{4.13}$$

At the beginning of the transient $R_d(V) << R_{in}$ and the time constant of the decay, showed in Eq. (4.13), becomes:

$$\tau_{circuit} = R_d(V) \cdot \left(C_{diff}(V) + C_{in}\right) \tag{4.14}$$

During the voltage transient the value of $R_d(V)$ increases and becomes higher than $R_{in} = R_{shunt}$. Therefore, R_{in} dominates the parallel between $R_d(V)$ and R_{in}, originating the shunt–resistance trend and the time constant of Eq. (4.14) will be:

$$\tau_{circuit} = R_{in} \cdot \left(C_{diff}(V) + C_{in}\right) \tag{4.15}$$

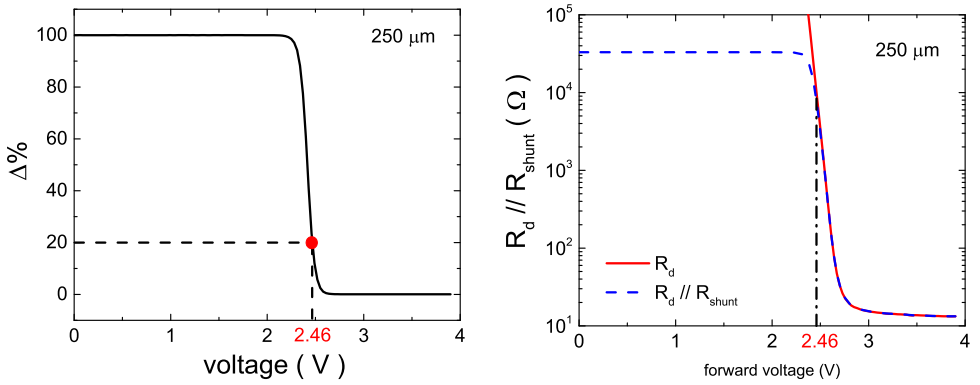
Fig. 4.12a shows the percentage variation of the parallel connection between R_{in} and $R_d(V)$ with the respect to $R_d(V)$ as a function of the applied voltage considering a $250\mu m$ diameter diode. For plotting this figure, $R_d(V)$ was easily obtained differentiating the forward curve of Fig. 4.8a by using [44]:

$$R_d(V) = \left(\frac{dV}{dI}\right)^{-1} \tag{4.16}$$

and $\Delta\% = [(R_d(V) - R_{eq})/R_d(V)] \cdot 100$.

Referring to Fig. 4.12a, if a maximum deviation of 20% from R_d is tolerated, Eq. (4.14) is valid as long as the voltage decay approaches $2.46V$ and this value may be set as a voltage limit after which the shunt–trend dominates. Fig. 4.12b shows that after the voltage limit of $2.46V$, the parallel between $R_d(V)$ and R_{in} saturates to R_{in}, therefore Eq. (4.15) will model the voltage transient.

Fig. 4.13 shows, as an example, the procedure adopted for extracting the ambipolar carrier lifetime τ_A: the dashed black line represents the linear fitting of the voltage decay after the voltage–drop and before the inflection point. The lifetime is extracted from the linear trait slope by using Eq. (4.11) for high injection level. The voltage limit of $2.46V$ is also plotted (red dashed–dot line) and it points out that the linear



(a) (b)

Figure 4.12: (a) Percentage variation of the parallel connection between R_{in} and $R_d(V)$ with the respect to $R_d(V)$ as a function of the applied voltage in the case of a 250μm diameter diode. (b) The parallel connection between the differential diode resistance R_d and the input resistance R_{in} (blue dashed line) and the diode differential resistance R_d (red solid line) are compared, as a function of the applied voltage.

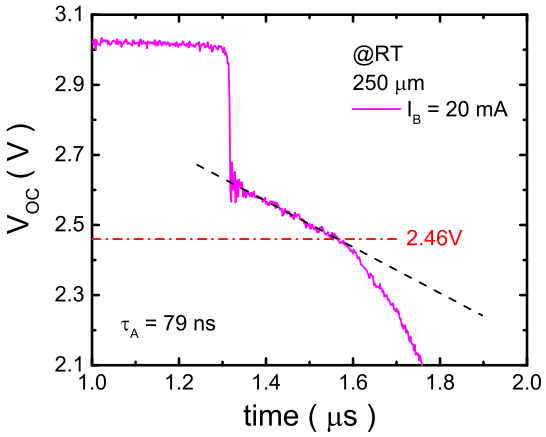


Figure 4.13: As an example, the procedure for extracting the carrier lifetime in the case of a 250μm diameter diode is shown. The magenta solid line represents the voltage decay of the diode, the black dashed line the linear fitting of the voltage decay, the red dashed–dot line represents the voltage limit. See text for further detail.

part of V_{OC} belongs to the diode. After this voltage limit the inflection point is due to the shunt resistor R_{in} which clearly dominates the remaining part of the transient.

Following the procedure described above, the ambipolar carrier lifetimes were extracted and plotted as a function of the bias current, as shown in Fig. 4.14. This figure highlights a dependence of τ_A from the current injection level as observed in the trends of Fig. 4.11. In particular, τ_A increases up to reach a saturation value $\tau_{A,Sat}$.

Since Eq. (4.11) is only valid for the high injection regime, the trend of τ_A in Fig. 4.14 might suggest that the diode works in high injection level only when τ_A saturates to $\tau_{A,Sat}$. For this reason, the hypothesis of high injection regime [52][53] must be verified.

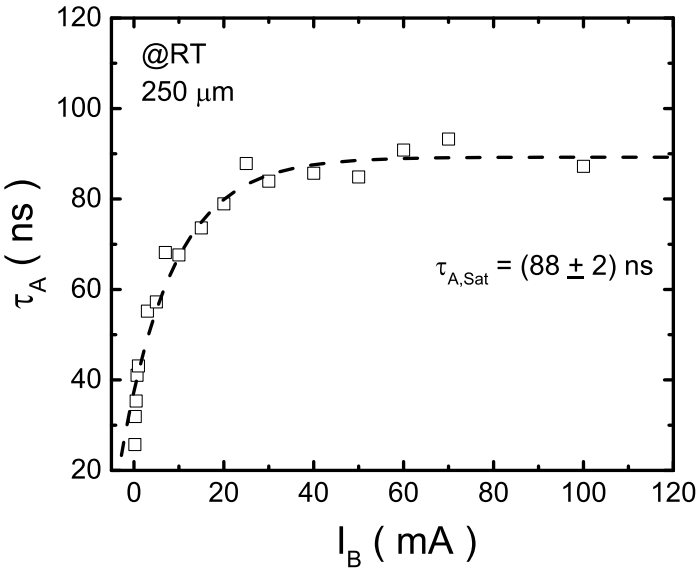


Figure 4.14: Typical trend of the extracted τ_A as a function of the applied bias current I_B for a diode of this study.

If the forward characteristic of the diode is studied, for verifying the high injection regime the following condition must be satisfied:

$$R_d(V) << R_s \tag{4.17}$$

where $R_d(V)$ represents the differential resistance computed by Eq. (4.16) and R_s is a sum of total resistance contributions of the diode given by:

$$R_s = 2R_C + R_{p^+} + R_{n^-} + R_{n^+} \tag{4.18}$$

where $2R_C$ represents the anode plus cathode contact resistances, R_{p^+} is the anode resistance, R_{n^+} is the bulk resistance and R_{n^-} is the intrinsic layer resistance. It is evident that for satisfying the relationship of Eq. (4.17), the only term of Eq. (4.18) which may change its value is R_{n^-} thanks to the effect of the modulation of the base in a PiN diode [52]. For the $250\mu m$ diameter diode, considering the geometry showed in Fig. 2.9:

$$\begin{aligned} R_s &= 2R_C + R_{p^+} + R_{n^-} + R_{n^+} \\ &= \left(2\rho_{c,sp} + R_{p^+,sheet} \cdot L_{p^+}^2 + \rho_{n^-} \cdot L_{n^-} + \rho_{n^+} \cdot L_{n+}\right)/A \end{aligned} \tag{4.19}$$

in Eq. (4.19), $\rho_{c,sp}$ is the specific contact resistance equal to $2 \cdot 10^{-5}\Omega cm^2$, $R_{p^+,sheet}$ is the anode sheet resistance equal to $2200\Omega/\square$, ρ_{n^+} is the bulk resistance per unit length defined in the process steps, while ρ_{n^-} can be estimated by the following equation [45]:

$$\rho_{n^-} = \frac{1}{q\mu_n N_D} \tag{4.20}$$

where q is the elementary electron charge, μ_n is the electron mobility and N_D is the intrinsic region doping.

The anode length $L_{p^+} \approx 600nm$, $L_{n^-} = 25\mu m$ and $L_{n^+} = 372\mu m$ (intrinsic and bulk length respectively). Finally, considering an electron mobility $\mu_n = 800cm^2V^{-1}s^{-1}$ [61][92], the value of R_s for a $250\mu m$ diameter diode of this study is: $R_s \approx 15\Omega$ and the higher resistance contribute in Eq. (4.19) is given by $R_{n^-} \approx 13\Omega$ which is the un–modulated base resistance. In this calculation the assumption of an electron mobility valid for low electric field and low doping was taken into account.

Fig. 4.15 shows on the left axis the forward current as a function of the applied voltage for a $250\mu m$ diameter diode (black solid line) and on the right axis the corresponding differential resistance values (red solid line). In addition, the red dashed line represents the R_s value calculated earlier by Eq. (4.19).

Observing the above described figure, it can be state that the diode enters the high injection regime when the bias current is greater than $24mA$ as the differential resistance satisfied the condition expressed by Eq. (4.17). This value is highlighted in the figure by the black dashed line.

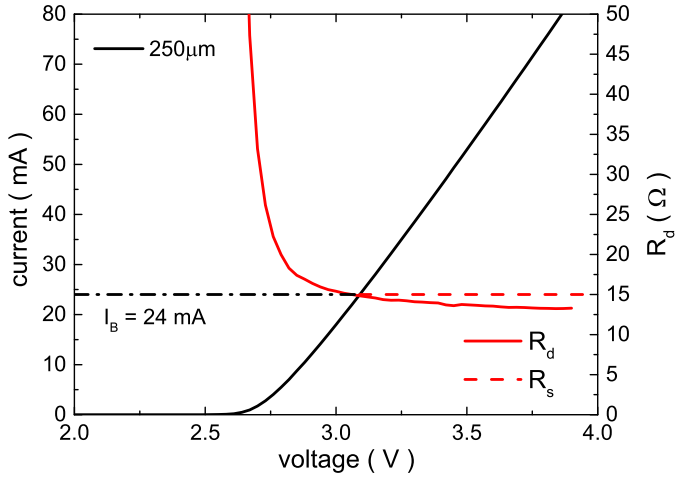


Figure 4.15: On the left axis the forward current (black solid line) and on the right axis the differential resistance (red solid line) of a $250\mu m$ diameter diode are reported. The R_s value plotted (red dashed lines) and the current level after which the diode enters high injection level (black dashed–dot line) are also plotted.

A cross-check was performed for verifying the high injection level condition by computing the minority carrier injected in the diode base by using the following simplified model [53]:

$$p_{avg} \approx n_{avg} = \frac{J_B \tau(J_B)}{2qd} \tag{4.21}$$

where J_B is the bias current density, $\tau(J_B)$ is the current–dependent carrier lifetime, q is the elementary electron charge and d is the half base width.

In Fig. 4.16, the plot of p_{avg}, obtained by Eq. (4.21), is overlapped to that of Fig. 4.14 on the right axis (red open circle). The blue dashed–dot line represent the intrinsic base doping $N_D = 3 \cdot 10^{15} cm^{-3}$.

This figure points out that:

1. the diode starts entering in the high injection level for a bias current of $10mA$ for which the condition of high injection regime ($p_{avg} \approx N_D$) is satisfied.

2. For current values lower than $10mA$, the model expressed by Eq. (4.11) is not valid: this is the case of extracted τ_A values which fall within the shaded grey region in the graph.

3. For current values larger than $25mA$, the average minority carrier density is about one order greater than the base doping and τ_A saturates to $\tau_{A,Sat}$. The saturation value of the carrier lifetime can be assumed as τ_{HL} and in the case of a $250\mu m$ diameter diode is $88ns$.

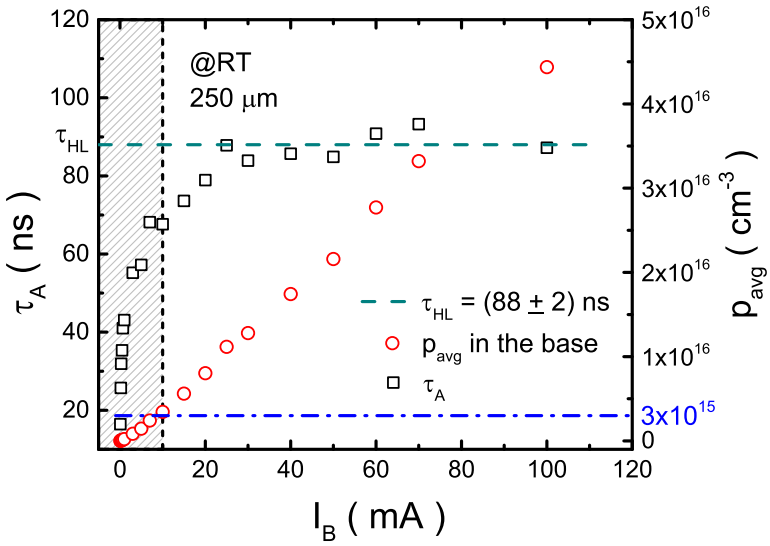


Figure 4.16: On the left axis the trend of τ_A is reported as a function of the applied bias current. On the right axis the average injected carried density is plotted by using Eq. (4.21). The data within the shaded region are not valid (see text for further details). The base doping $N_D = 3 \times 10^{15} cm^{-3}$ is highlighted with the blue dashed–dot line.

4.3.6 Volume and Surface lifetime

Fig. 4.17 shows the OCVD measurement results on diodes with different diameter, in particular, referring to Table 2.1, on diodes D1,D2,D3 and D7. Measure configuration was discussed in the previous section.

Fig. 4.17a depicts the trend of τ_A for all diodes as a function of the applied bias current density. As explained in the previous section, the shaded area represents the region for which Eq. (4.11) is not valid, while the saturation value of τ_A is labelled as τ_{HL}. Table 4.2 summarizes the obtained results.

Fig. 4.17b illustrates, for all diodes, the trend of p_{avg}, computed by using Eq. (4.21), as a function of the applied injection current density. The green dashed–dot line represents, for all diodes, the average concentration for which τ_{HL} is reached.

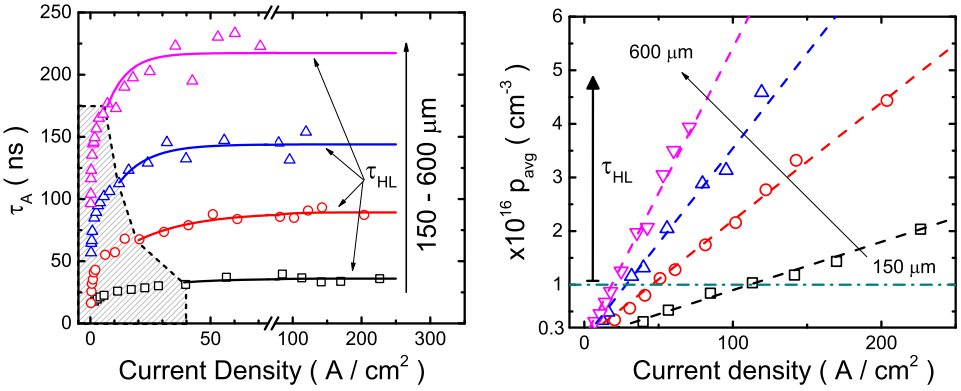


Figure 4.17: (a) Trend of τ_A for all diodes versus the applied bias current density. (b) Computed p_{avg} versus the bias current density, the dashed–dot line represents the average carrier concentration for having τ_{HL}.

For all diodes of this study, a dependence of τ_A from the bias current (i.e. injection level) is evident. This trend, depicted in Fig. 4.17, may be explained considering Eq. (4.3), where all its terms depend on the injected minority carrier concentration Δp. Analysing this equation in the frame of SiC material, the term τ_{rad} can be neglected

τ_{HL} MEASUREMENT RESULTS

Diode	Area [cm^2]	$J_{B,HL}$ [A/cm^2]	τ_{HL} [ns]
D7	0.2×10^{-4}	113	36
D1	0.5×10^{-4}	51	88
D2	1.3×10^{-3}	32	142
D3	2.8×10^{-3}	25	218

Table 4.2: τ_{HL} measurement results.

as SiC is an indirect band–gap material (like Silicon), therefore radiative recombination are highly improbable. In the case of Auger recombination and carrier–carrier scattering phenomena, which take place for very high injection levels, carrier lifetimes are expected to reduce [96][88]. Observing the trend of τ_A in Fig. 4.17a, after the saturation value of τ_{HL} the lifetimes never decreases, meaning that very high injection condition is never reached as shown in Fig. 4.17b and both Auger recombination and carrier–carrier scattering phenomena are of minor importance. Therefore the only term which might dominate the recombination rate in Eq. (4.3) is due to Shockley–Read–Hall generation–recombination mechanism. This suggests that a dominant recombination center might be present in these devices. Such a hypothesis is congruent with the study carried out in the previous chapter and with the literature results for ion implanted SiC diodes (see Chapter 2). In particular it is well–known in the literature that the positions occupied by the lifetime killer defects are those of $Z1/2$ and $EH6/7$ in the SiC bandgap [67][68][76] and with the fact that the density of such defects significantly increases with the increasing temperature for treatments above 1500°C [109][110].

The extracted τ_{HL} exhibits a dependence on diode dimensions, in particular ambipolar carrier lifetimes increase with increasing diode dimensions as clearly shown in Fig. 4.17. This behaviour suggests that recombinations might also occur at the diode periphery and the measured τ_{HL} might be an effective lifetime. More precisely, as shown in Eq. 4.9, τ_{HL} might be a sum of volume and surface lifetime. This hy-

pothesis is reasonable since in the previous chapter was demonstrated that the studied diodes have a non–negligible periphery current component. Moreover, other authors have observed the above described dependence by using different measurement techniques (e.g. [111]).

The excess carriers generated, either optically or electrically, in a semiconductor region tend to reach the equilibrium value through recombination either in the bulk or at the surface, following the continuity equation (Eq. (4.6)) that can be solved under appropriate boundary conditions; in the case of surface recombination its solution, which yields to τ_s, is usually described in term of a surface recombination velocity s_r [112]. Relating τ_s to the diode geometry and surface recombination velocity s_r, is not trivial: simple expressions of $1/\tau_s$ can be found in two limiting cases, for cylindrical geometry, of small and large s_r, respectively, corresponding to a surface– or diffusion–limited τ_s.

In the case of low s_r [112][113]:

$$\frac{1}{\tau_{HL}} = \frac{1}{\tau_{HL,vol}} + s_r \left(\frac{2}{r} + \frac{1}{h} \right) \tag{4.22}$$

where r is the anode radius, and $2h$ is the cylinder thickness that equals the drift layer thickness $2d = 25\mu m$.

In the opposite case of high s_r [114]:

$$\frac{1}{\tau_{HL}} = \frac{1}{\tau_{HL,vol}} + \frac{\pi^2 D}{4} \left(\frac{9}{4r^2} + \frac{1}{h^2} \right) \tag{4.23}$$

where D is the carrier diffusion coefficient within the bulk, the other quantities were previously defined.

Figs. 4.18 illustrate the fitting of the experimental data by using either Eq. (4.22) (Fig. 4.18a) or Eq. (4.23) (Fig. 4.18b). By interpolating the experimental data by using these expression, it can be concluded that:

- in the case of surface limited lifetime (Eq. (4.22)), the extracted volume lifetime is negative and the surface recombination velocity is too high. In contradiction to the hypothesis of low s_r (Fig. 4.18a).

- in the case of diffusion limited lifetime (Eq. (4.23)), an optimum correlation between data is verified and a value of $\tau_{HL} = 320ns$ was extracted (Fig. 4.18b). Unfortunately, the obtained value of the diffusion coefficient D is higher than that expected $\approx 5cm^2/s$ for $\mu_n(\mu_p) = 800(120)cm^2V^{-1}s^{-1}$.

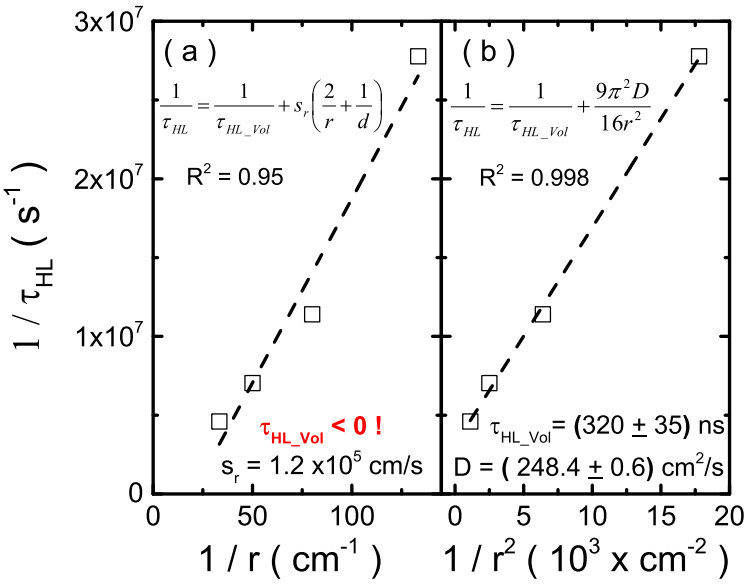


Figure 4.18: Separation of volume and surface lifetime in the case of (a) surface limited lifetime and (b) diffusion limited lifetime.

The excess carrier decay is mathematically described as the infinite summation of exponential terms called modes, each having different lifetimes τ_i [113][114][115]. The higher order modes have shorter τ_i, therefore after a sufficient long time the excitation stops and the decay is dominated by the fundamental mode τ_0.

The assumption of a decay dominated by the fundamental mode τ_0 is often not fulfilled in OCVD measurements. However, as proved by analytical simulations, the complete model of decay shows that the measured lifetimes allows estimating the volume lifetime, with an uncertainty lower than 10% also for measurements with $t < \tau_0$, provided that different diode diameters are used. Therefore can be conclude that the observed variation of lifetime with diode dimension is mainly due to recombination

on the lateral cylindrical surface of the recombination volume formed by the anode and the underneath SiC material.

Summary

since the 1990s, thanks to the quick advances in manufacturing processes, 4H polytype Silicon Carbide devices have became the preferred choice for applications in the field of high power systems. In the last decade research efforts have led to additional improvements regarding the wafer qualities and device performances.

In this thesis work 4H–SiC PiN ion–implanted vertical diodes for high power applications, manufactured at the Microsystem and Microelectronic Institute of Research National Council (CNR–IMM) of Bologna, were deeply characterised.

The studied diodes have a circular anodes with different diameter dimensions ranging from $150\mu m$ to $1000\mu m$. The p^+ type anodes have a $2.5 \times 10^{20} cm^{-3}$ doping and are obtained by ion implantation processes on an epitaxial intrinsic n^- region (the PiN base region) with a doping of $3 \times 10^{15} cm^{-3}$. This n^- region lies on a bulk material n^+ with resistivity of $0.021\Omega cm$. The cathode contact extends all over the back of wafer, while the front contacts are circulars, concentric with anodes and have dimensions smaller than $20 \div 25\mu m$ with the respect to anodes.

Forward electrical current–voltage curves were measured in a voltage range $0 \div 3.9V$ with $30mV$ voltage step and a $4s$ delay time in a temperature range of $30° \div 290°$C. Reverse curves were measured in the same temperature range, between $0V$ and $-190V$ with a delay of $300s$. The measured curves were used for extracting the area and perimeter current current densities. These latter curves were analysed by using the Sha model, valid for planar diodes with cylindrical symmetry. For the forward recombination area current density was demonstrated that the simple model of the abrupt junction can be used to model the experimental data. Therefore, the

position of the recombination centre within the material band–gap was obtained with a value of $E_A \approx 1.65eV$. Furthermore, the recombination lifetime in the Space Charge Region was extracted, in particular: $\tau_r \approx 1\mu s$. The perimeter current density was analysed as due to surface recombination and the surface quality factor was obtained: $s_p \cdot L_s \approx 1.5cm^2s^{-1}$. This value qualifies the native oxide which spontaneously forms on the sample surface when it is exposed to air. For comparison with the literature data this value is two order of magnitude smaller than that obtained for Mesa PiN diodes. This result is promising for the use of ion implantation technology for the fabrication of SiC bipolar devices.

Unfortunately, reverse current–voltage curves cannot be analysed in the frame of the simple abrupt junction model as th voltage dependence of the reverse area current density was steeper than the expected $V^{1/2}$. However, the value of E_{na}, which can be considered a trap signature, were extracted. Two different values were obtained: $E_{na1} \approx 0.2eV$ and $E_{na2} \approx 0.5eV$. The set of trap activation energies deriving from reverse and forward currents were compared with those obtained from a DLTS study performed on the same diodes finding a good agreement between them. In particular the trap positioned at $1.65eV$ was associated to the $EH6/7$ defect, the trap positioned at $\approx 0.5eV$ was associated to the $Z1/2$ defect. In the literature, it is demonstrated that these two traps are associated to the presence of carbon vacancies in 4H–SiC samples. The $0.2eV$ traps, instead, may be due to metal impurities.

Numerical simulations by using the commercial softward Synopsys Sentaurus TCAD were performed in order to understand the origin of periphery current which affects the forward characteristics of these diodes. This simulation study also demonstrates that a detailed (but simple) electrical characterization, like that performed on these diodes, combined with appropriate literature results can be used, in first approximation, for explaining unexpected physical phenomena without using other more complicated measurement techniques, like DLTS. Firstly, a deep literature study pointed out that the energy level of traps and capture cross–section obtained by the area and perimeter current components and by DLTS measurements on the diodes were in agreement. Therefore, the hypotheses made on traps extracted by electrical measurements were kept and their values were used as input parameter within the

simulator. Capture cross–sections available from DLTS (which were in agreement with literature results) were also used. The missing data were fitting parameters and can be considered as original result of this simulation study. The first simulations were performed on an ideal structure for fitting the experimental area current density component the following value of lifetime were used: $\tau_{e/h} = 12/20ns$ for $1.65eV$, $\tau_{e/h} = 420/10ns$ for $0.2eV$ and $\tau_{e/h} = 8/100ns$ for $0.5eV$. For the three traps: electron lifetimes were obtained by DLTS study whereas the hole lifetimes are the fitting parameters. Once fitted the area current density, the other simulations were performed on a real structure, that is, considering the periphery of diodes made by the intrinsic material next to the anode having a fixed length of $50\mu m$. In this real case for fitting the total curves of the whole set of diodes with different diameter dimensions by using the trap levels and lifetimes used for the ideal case, a negative fixed charge on the surface of diodes were taken into account. This negative charge extends the space charge region in the base region of diodes next to the surface increasing the recombination current. For a fixed periphery length, this effect is more visible in small–diameter diodes.

Finally, lifetime measurements were performed on the same diodes by using the electrical technique of Open Circuit Voltage decay (OCVD). After a detailed characterization of the experimental set–up for evaluating the parasitic quantities which could affect lifetime measurements, the ambipolar lifetime of diodes was extracted. Since increasing lifetimes with increasing diode dimensions were obtained, the analysis of bulk and surface lifetimes were performed. It was found that high recombination occurs on the side of the intrinsic material which surrounds the volume defined by the diode anodes. The extracted recombination ambipolar lifetime related to the device volume was about $320ns$.

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