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Electro-thermal simulation methodologies for automotive power electronic systems

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To
the humble ones,
those who dream big.

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Chapter 1

Introduction

We can only see a short distance ahead,
but we can see plenty there that needs to be done.

– Alan Mathison Turing

Power devices are more and more used in automotive applications. The target is to improve energetic efficiency, safety, comfort, connectivity, and entertainment in modern vehicles. Such devices are meant to work, during their whole lifetime, in harsh environmental conditions, due to electric noise, temperature changes, and mechanical vibrations, just to give some instances. Then, due to the intrinsic nature of power devices (high power dissipation), and the environmental conditions they are supposed to operate in, it is necessary to develop an accurate design to avoid electric performance reduction, on the one hand, and reliability problems, on the other hand.
High power density, dissipated by power devices, can generate high temperature peaks and high temperature gradients inside them, premises which are the main causes for mechanical stress in the costituting materials. Hence, devices degradation is caused by a complex interaction among electric, thermal, and mechanical aspects. Such an interaction requires to be studied to improve safety and reliability in designing new devices, or to produce guidelines for the use of already-available ones.
The most relevant target, both in the field of industrial and academic research, is

studying the interaction and modelling of electric, thermal and mechanical aspects, concerning electronic devices for automotive application (electric performance, breaking mechanisms, strength, and reliability). As a matter of fact, the study of interaction among physical phenomena can lead to develop devices and systems apt to tolerate heavy environmental conditions.
Power electronic systems support a lot of industrial and automotive applications. This kind of applications are required to operate in harsh environments and in strong conditions. For this simple considerations, the study of power electronic systems reliability is a key element to develop reliable industrial and automotive applications. In the study of power electronics reliability, one of the main aspects modeling, which allow to reduce the number of prototypes and to have a pro-active way to improve reliability.
In this work, an overview on the importance of reliability and its main methodologies will be provided in order to model and to simulate complex power electronic systems, while in the second part new methodologies of modeling will be presented with the purpose of reducing simulation time without losing quality of the results. In particular, the methods developed could be considered lightweight methods by using standard model techniques, with the advantage to save time but with the ability to reproduce, completely or partially, the following behaviors of power electronic devices:

1. thermal;
2. electrical;
3. mechanical.

The work is structured in 7 chapters.
Chapter 1 is this chapter.
Chapter 2 presents the automotive sector in relation to the power devices, introduces a brief overview on power MOSFET and their main application, and, finally, describes concepts about quality management and reliability of power devices.
Chapter 3 introduces the main topic about thermal behavior of power MOSFETs and

explains the state of the art about thermal studies. In this chapter, numerical methods and lumped element methods are analyzed.

Chapter 4 introduces the first original methodology in order to study the thermal behavior of power devices. The methodology merges the advantages of finite element modeling with lumped element modeling in order to simplify non-stationary finite element studies.

Chapter 5 explains a new methodology able to describe the thermal behavior of a complex electronics system through the use of a lumped element models. The methodology introduces different advantages; in fact, it is able to generate a thermal model that can take into account the system's non-linearities due to materials and natural air convection. The model extracted through this approach is easy to simulate and it could be a valid alternative to finite element method simulations. The methodology proposed is presented on a system with multiple heat sources.

Chapter 6 is dedicated to electro-thermal modeling. The developed methodology allows to describe the entire electrical and thermal behavior of a complex power system through the use of a SPICE simulator. The model created through these techniques is really fast and the advantages for the designer are great; in fact, with only one tool and without thermal modeling knowledge, a system could be modeled and simulated.

Chapter 7 provides the conclusions.

Finally, it is important to remark that the main objectives of this dissertation are the results of the collaboration between the Department of Engineering and Architecture of the University of Parma and K-AI GmbH of Infineon Technologies Austria AG, within the Project EM^{2}APS (Workpackage 6.2).

Chapter 2

Automotive and power electronics

You can't trust code that you did not totally create yourself...
Especially code from companies that employ people like me.

– Kenneth Lane Thompson

This chapter provides the main concepts about power electronics systems and automotive sector companies. In fact, the purpose of this chapter is to introduce some basic topics, in order to clarify the next chapters.
In particular it is focused on:

- the relationship between power electronics and automotive sector;
- power MOSFET oveview;
- semiconductor device reliability and process improvement.

2.1 The role of power devices in automotive

This Section will briefly concern the main motivations and necessities deriving from the introduction of power electronic components into automotive industry. The intent is to present a picture of the importance that power electronic systems take on into

the different automotive applications, thus giving reasons for the relevance of studying their reliability. That is to demonstrate how pervasive electronics is in modern automobiles.

2.1.1 Overview

The use of electronic devices in cars is growing over the time. Let us just think about the fact that, in 1977, a car could contain electronic components to the amount of $ 110 [1] which was equivalent to 5% of its price, while 2010 data indicate that the value of the electronic parts has reached 35% of the whole car value [2]. Estimates suggest that, by 2030, 50% of a car cost will be due to the electronic parts [2]. Figure 2.1 [2] summarizes the cost percentage evolution of electronic components in relation to the automobile cost. Even though, initially, the use of information tech-

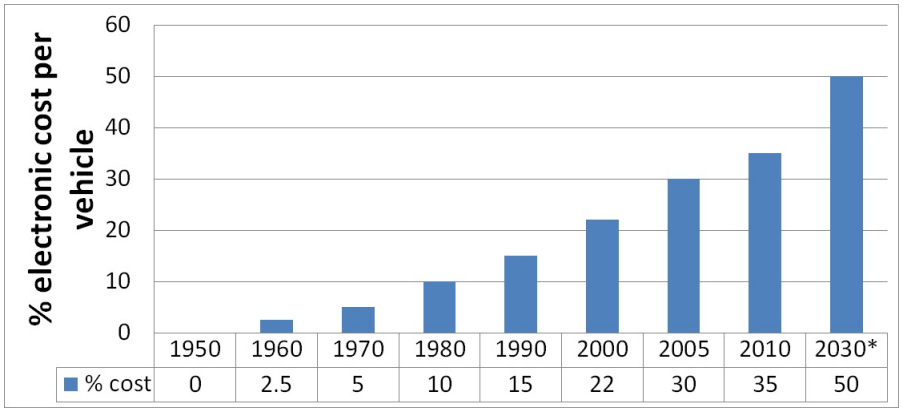

Figure 2.1: Evolution of electronic components cost % in relation to the cost of a car from 1950 to 2030 (*Forecast).

nologies in automotive produced skepticism, it is undeniable (as evolution proves) that it has become a consolidated fact [3] and a reference point for automotive innovation. Nowadays, automotive Original Equipment Manufacturer (OEM) considers electronic components as a necessary means to follow sector normative changes [2]. The evolution in the use of electronic devices and computation systems into the au-

tomotive sector has moved from non-critical applications (i.e. comfort elements) to critical applications (i.e. control on the instrumentation panel); this is due to the increase of their reliability. Therefore, the use of electronic components to implement safety features is assuming more and more importance in the last decades, since, for the next decades, the aim is to increase the vehicles' safety. It is peculiar the fact that the trigger element for the use of electronic components inside vehicles was due to unexpected necessities concerning combustion engine emissions regulation and the austerity, both having taken place in the USA and in several European states in the 70s [4]. Table 2.1 [4] presents the main uses of electronic components in vehicles. A

Category	**Example of system**
Engine and traction	Electronic Fuel Injection (EFI), Engine Control Unit (ECU), Trasmission Control Unit (TCU), Knock Control System (KCS), Cruise Control and Cooling Fan.
Cabin and safety	Active 4-wheel steering, active control suspension, Anti-lock Brake System (ABS), Traction Control System (TCS), Vehicle Stability Control (VSC) and air bag system
Comfort and economy	Preset steering wheel position, climate control, seat heating, power windows, door lock control and mirror controls
Display and audio	Radio, CD player, DVD player, TV, phone, navigation system and instrument cluster
Signals communication	Communication bus, starter, alternator, battery and diagnostic

Table 2.1: Main systems supported by electronic components.

grouping of electronic components widely used in the automotive sector is the power devices one [5]. Such devices are naturally characterized by the capacity to reach high dissipated power and, consequently, to reach high temperatures. To this characteristic, it should be added the fact that the device is positioned inside compartments containing systems able to generate high temperatures (for instance, the engine compartment). Therefore, the study of power electronic devices reliability is linked to the fact that such devices are meant to operate in extreme conditions and in critical applications, whose malfunctioning, or fault, could compromise safety. To such an end, it is quite simple that, once identified the main responsible for the damage, designing will progress by taking into account the derived constraints. The primary problems linked to power devices and systems reliability have been identified and should be attributed to the following physical phenomena [6]:

1. thermal;
2. electrical;
3. mechanical.

Particularly, electrical phenomena influence thermal phenomena, which are, in turn, influenced by electrical phenomena. Finally, mechanical phenomena are influenced by thermal phenomena. Inevitably, thermal phenomena appear as the most complex ones as they influence and are influenced by electrical and mechanical phenomena. Figure 2.2 shows an overview of the relations among the main physical phenomena that afflict power devices. Studies and designing efforts about the effects of ther-

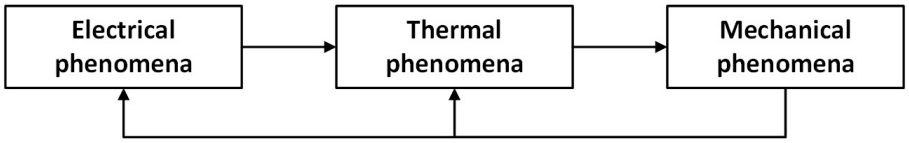

Figure 2.2: Main flux of physical phenomena that influence a power device.

mal phenomena are becoming more and more prominent. As a matter of fact, efforts are mainly concentrated on the study of thermal, thermo-electrical, and thermo-mechanical behaviors. The main power devices used inside vehicles are [7]:

1. power MOSFETs;

2. IGBTs.

Finally, Figure 2.3 shows temperature intervals at which power devices can operate. The chart concerns the first seven years of the 2000s [4].

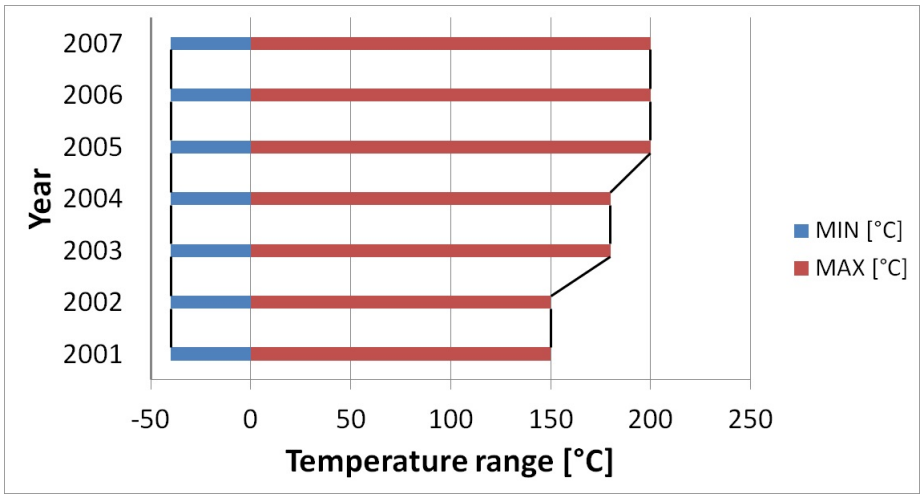

Figure 2.3: Evolution of operating temperature intervals supported by power devices.

2.1.2 Requirements of the automotive electronic components

To better understand the importance of electronic components in vehicles, specifications of requirements proposed by [2] have been reported.
A vehicle can be seen as a highly complex mass product, composed by several subsystems. Each subsystem is composed, in turn, by hundreds of components (among which electronic components). According to the classification proposed by [2], specifications can be divided into three classes:

1. functional requisites;

2. availability requisites;

3. economic requisites.

Functional requisites are those that let a function be executed. In the case of electronic car components, two categories are identified:

- body electronics;
- system electronics.

The first includes all those components that concern the management and control of information regarding the vehicle's motion. Examples of body electronics can be the doors' locking system or the informative dashboard. Concerning safety, they can be considered as non-critical; however, it is necessary to develop a basic safety to avoid behaviors that could interfere with the driving act. Concerning the second category, examples can be the breaking system or suspensions control. Electronic system components are generally pointed at control. For instance, a sensor lets a microcontroller monitor the specific system, while an implemented actuator equipped with a power device lets a system be controlled. Concerning electronic system components, reaction time is relevant and, generally, the above cited components regard critical systems. Concerning availability requisites, it is necessary to consider how availability of a vehicle's components is certainly a key-factor. The fact of having a car able to work in any circumstance certainly adds in value. To say something about electronic car components, three categories concerning this second class can be identified:

- reliability;
- maintainability;
- vehicle safety.

The first category clearly concerns reliability, that is to say how pervasive electronic components are inside a vehicle. By taking into account the ECU in modern vehicles, which are more than 10 units per car and are associated to the main functions of the vehicle, the fault of one of these could cause stopping vehicle, as all the units should work together, thus creating consequent inconveniences. The second category,

on the contrary, is linked to maintenance since electronic components are highly complex. However, maintenance staff do not have the required competences to carry out complex fixings and directly intervene on the single electronic component. In such a case, electronic components are included in component packs named Field Replaceable Units (FRU), easily replaceable. The third, and last, category, instead, concerns car safety, which presents two elements: the first is the use of electronic components to increase the vehicle safety; the second regards electronic components safety by adopting mechanisms of fault tolerance. Finally, the economic side in automotive sector is a highly competitive and global one, so that costs decrease can be a competitive advantage, without taking into account that drivers (the market) could prefer more comfortable and safe vehicles. Concerning electronic components, the following categories are identified:

- manufacturing cost reduction;
- legal constraints;
- increased traffic safety;
- increased dependability and performance;
- increased comfort.

The first category is certainly more intuitive: lower costs, means major profit margin and reduced prices. The second one is linked to legislation, which means pollution restriction, public safety, where electronic components can play a determining role. The third one concerns the social costs deriving from accidents: the more safety is increased by electronic components, the less social costs will have a bearing. The fourth one refers to minor costs deriving from car maintenance and the reduction of costs to obtain higher performance. The fifth, and last one is comfort, that can be increased through electronic components.

2.1.3 Evolution of the use of electronics in automotive

The use of electronics in automotive started at the end of the 60s with an increasing use in the 70s.
The work proposed by [8] explores safety solutions in cars bus systems and shows the main applications divided by decades. In particular, by reporting data for each decade, the main electronic-based systems are presented [9]. Such data are reported in Table 2.2 [9]. More and more intelligent electronics-based system applications'

Decade	**Applications**
1970	Electronic fuel injection Electronic control panel Centralized door locking Cruise control
1980	Electronic gear box Antilock brake system Automatic climate regulation Automatic mirror Car phone
1990	Airbag Electronic navigation Electronic driving assistance Electronic traffic guidance Voice control
2000	Drives-by-Wire Internet Telematics Ad-hoc networks Personalization

Table 2.2: Electronics development in automotive sector divided by decades and applications.

outbreak in automotive has clearly raised energy request. In fact, from applications based on simple mechanical and hydraulic systems, applications have been based on hydraulic and hydraulic/electronic systems. Figure 2.4 properly shows how this evolution has taken place in the last 40-50 years. In particular, Figure 2.4 focuses on driving control systems technologies and automotive applications in accordance with [1]. Clearly, applications based on electronic components consume power and,

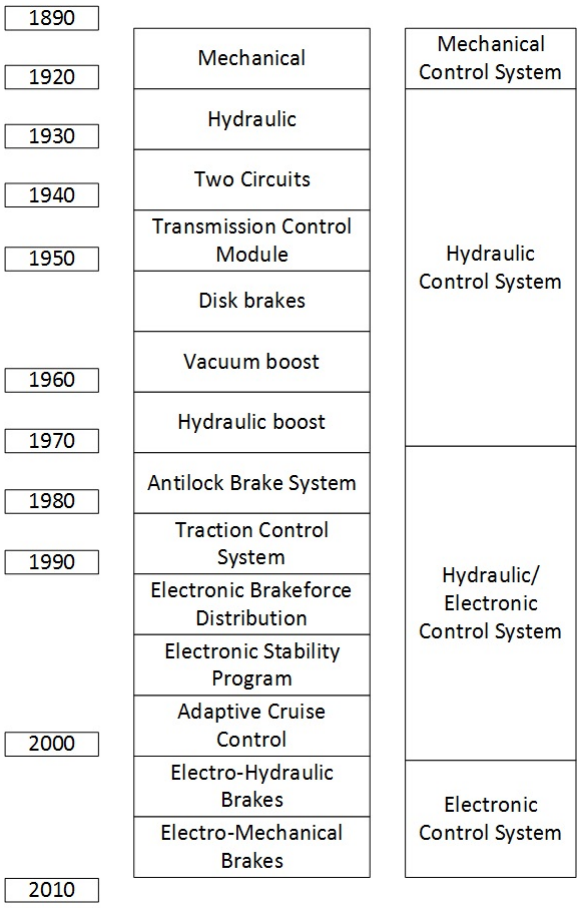

Figure 2.4: Evolution of driving control systems and automotive applications.

consequently, modern cars have far more remarkable energy requests as compared

to cars of the past. It is considered that, nowadays, premium sector cars, on average, consume 2.5 kW. This is due to the integration of applications not strictly linked to the automotive world, but also entertainment applications. In the present decade, this continuous evolution will bring to automobiles requiring energy around 3 kW, partly due to this sector emerging technologies [1]. To face the increasing power request of automotive applications, 42 V electrical systems are being developed. Hybrid cars are particularly involved in this aspect, but, in the future, this could be extended to ordinary cars. This is a remarkable advantage, concerning power involved, but, at the same time, it will ask for partial re-designing and, certainly, it will give prominence to the study of power device reliability in automobile development. Figure 2.5 demonstrates the growth of power request by applications integrated in cars. Figure 2.5 also shows that in the 70s only 0.6 kW were needed, this to demonstrate how electronics in cars was limited, while the graph's trend will reach 3 kW by 2020.
Concerning the main loads, [10], [11] and [12] certified that, in 2005, the main loads could be divided as in Table 2.3. Last, but not least, is the role electronics plays in reducing CO_2 emissions by cars. As a matter of fact, the observance of more and more strict pollution legislation is mainly implemented by the use of electronic components. On this matter, reference should be made to the clamor caused by [13]. To conclude, for a detailed description of power electronic systems supporting modern cars' features, reference should be made to [14].

2.1.4 Discussion

As previously noted, electronic components have assumed a noteworthy role in automotive industry. Remarkable are several aspects concerning this issue, such as the turnover due to the intense use for managing different systems inside the vehicle, but also for unrelentingly strengthening the reliability aspect. Therefore, nowadays the electric system is completely supported by power electronic; let us just think about the way power MOSFETs have supplanted the relays.
If, on the one hand, new introduced features can more and more easily be integrated thanks to the insertion of massive power electronics, on the other hand, power electronics costs inside a car considerably affect the complex cost of the vehicle itself.

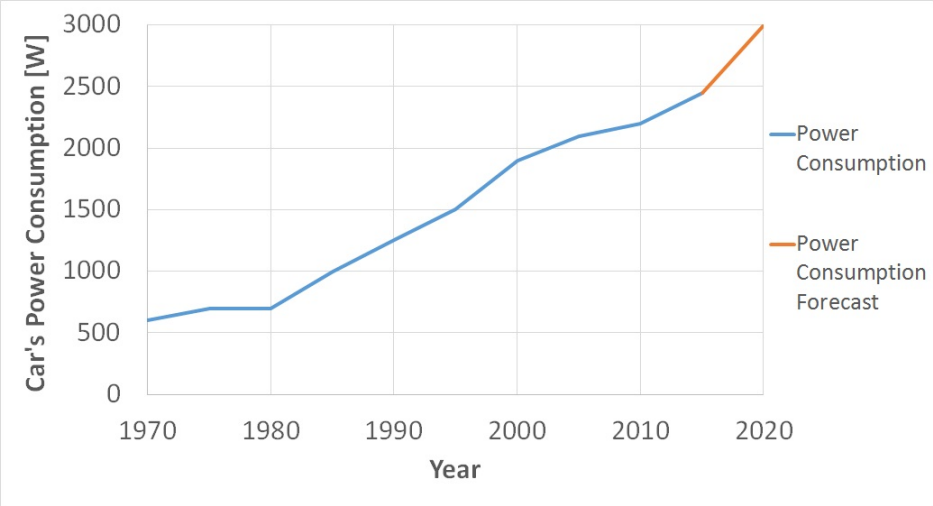

Figure 2.5: Evolution of power electronics power request between 1970 and 2020.

Load	**Average power consumption [W]**
Electro-mechanical valves	800
Water pump	300
Engine cooling fan	150
Power steering	100
Heated windshield	165
Catalytic converter	90
Active suspension	360
Communication	100
TOTAL	2065

Table 2.3: A car's main loads in 2005.

Therefore, a power electronics costs reduction can be realized through the use of simulation methodologies more and more efficient and effective, that let reliability be increased and the number of prototypes and tests reduced. Automotive industry has inexorably requested power electronic devices more and more prone to support hard environmental conditions, thus influencing their designing. According to [14], a power device for automotive must be designed to work in complete safety by taking into account the following aspects:

1. static and transient voltage ranges;
2. high environment temperatures;
3. electromagnetic interference and compatibility requirements;
4. shock and mechanical vibrations.

Concerning the wide spectrum of static voltage range, which considerably influences power devices self-heating, reference should be made to Table 2.4 [15] to give an overview. Even if the four aspects cited previously should certainly be considered

Condition	**Static voltage [V]**
Nominal voltage with engine off	12.6
Maximum operating voltage	16
Jump start voltage	24
Reverse battery voltage	-12
Maximum voltage in failure conditions	130

Table 2.4: Overview about voltage static range in accordance with.

in the designing phase, high temperatures are the hardest factor to manage for automotive power electronic systems [14]. As a matter of fact, operating temperature can be extremely low, around -40 °C, but into a car's engine compartment, it can be extremely high and, if associated to important thermal cycles and vibrations, can considerably reduce the device lifetime as reported in Table 2.5 [15]. In particular, thermal cycles can reach extreme conditions over 200 °C. Extreme temperatures observed

in different parts of a vehicle are reported as indicated by [15] and [14]. Concerning

Vehicle part	Min temperature [°C]	Max temperature [°C]
Exterior	-40	85
Chassis isolated location	-40	85
Drive train	-40	177
Interior and trunk	-40	85
Instrumentation panel	-40	177
Rear deck	-40	121
Near radiator	-40	100
Near alternator	-40	131
Dash panel	-40	141
Exhaust manifold	-40	649

Table 2.5: Overview of automotive temperatures.

industry applications, automotive is a sub-sector of the more general industrial one. As a matter of fact, a wider spectrum of power device typologies are used in industrial applications (generally power MOSFETs and IGBT in automotive), in addition to the voltage ranges, that generally can exceed thousands of Volts (some hundreds in automotive).

2.2 Power MOSFETs basic concepts

Since the introduction of power devices, dating back to the coming of SCR in 1957, the evolution of power devices has been enormous. As a matter of fact, along the years, more and more power devices have entered the market by covering a wide spectrum of industrial applications. Differently from signal devices, whose choice is mainly guided by voltage rating, current rating, and operating frequency, when considering power devices, in addition, it is necessary to conveniently take into account three other factors:

1. Safe Operating Area (SOA), it permits to identify the limits of static and dynamic electrical current and the voltage that let the power loss be identified for a safe use of the device;

2. maximum temperature, it permits to identify the acceptable maximum operative temperature and the maximum storage temperature;

3. thermal resistance, it permits to evaluate the maximum heat dissipation in case of thermal resistance junction-ambient, and to consider the potential insertion of a heat sink.

This section will deal with a brief overview of power MOSFETs, which will be the most used devices in the development of modeling and simulation methodologies presented further on. Finally, it should be remembered that, according to [16], N-Channel Enhancement power MOSFET can be subdivided into two macro-categories:

1. conventional;

2. CoolMOS™.

2.2.1 MOSFET SOA, ON-state resistance, and thermal resistance

A MOSFET is a voltage-controlled three terminal device, which requires a small dynamic gate current to be turned on. Generally, it is the faster device used in switching circuits. Figure 2.6 shows schematically the physical structure of a power MOSFET, while Figure 2.7 the reference electrical circuit. Depending on the operating region, ohmic and saturation current I_D is calculated by (2.1) and (2.2), respectively.

$$I_D = K\left[2\left(V_{GS}-V_T\right)V_{DS}-V_{DS}^2\right] \quad \text{for } V_{GS} > V_T \text{ and } V_{DS} < \left(V_{GS}-V_T\right) \tag{2.1}$$

$$I_D = K\left(V_{GS}-V_T\right)^2 \quad \text{for } V_{GS} > V_T \text{ and } V_{DS} > \left(V_{GS}-V_T\right) \tag{2.2}$$

Here K is the MOSFET device parameter, V_{GS} is the voltage between gate and source, V_{DS} is the voltage between drain and source, and V_T is the threshold voltage of the

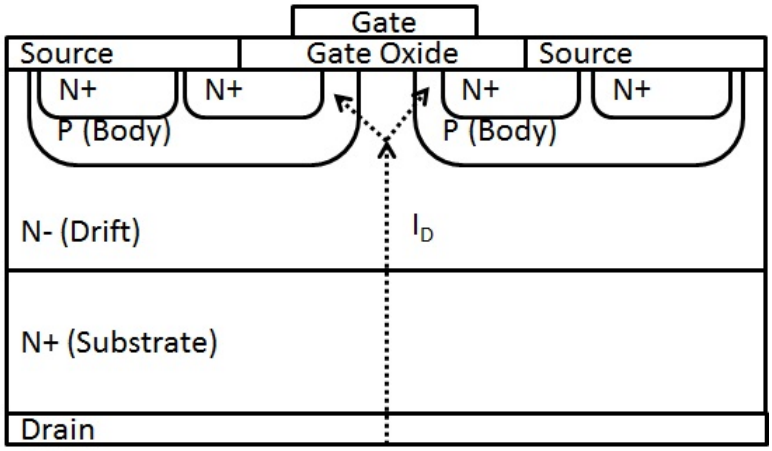

Figure 2.6: Basic MOSFET physical structure.

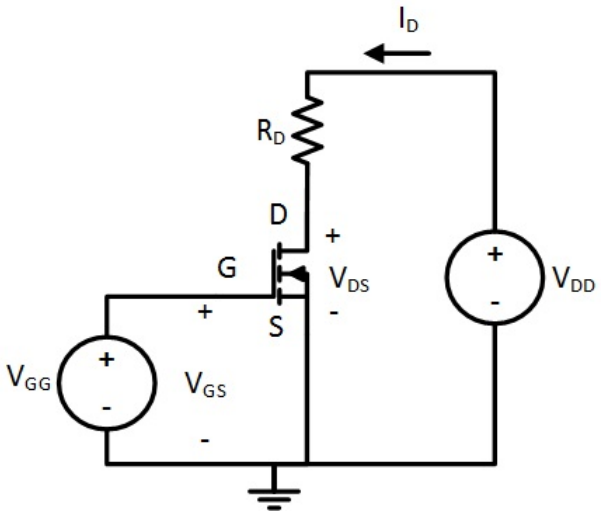

Figure 2.7: Basic MOSFET circuit with the main parameters.

device. K is defined by (2.3), whereas oxide capacity per area unit c_{ox} is defined by (2.4).

$$K = \mu_n c_{ox} \frac{W}{L} \tag{2.3}$$

$$c_{ox} = \frac{\varepsilon_{ox}}{x_{ox}} \tag{2.4}$$

Here μ_n is mobility, W and L are the channel width and lenght respectively, ε_{ox} is the dielectric constant of Silicon Dioxide, and, finally, x_{ox} is the thickness of the oxide. Differently from the signal MOSFET, the power MOSFET presents a highly asymmetrical structure [16]. Under its most famous configuration, the Vertical Diffused MOSFET (VDMOS) and its derivatives, the structure development appears vertical. This kind of structure presents parasitic devices:

1. a BJT;
2. a PN-diode.

By taking as reference Figure 2.8 [17] which shows the output characteristics of a power MOSFET, it is possible to affirm that resistance $R_{DS(ON)}$ is computable through the equation (2.5).

$$R_{DS(ON)} = R_S + R_{ch} + R_{acc} + R_{body} + R_{drift} + R_{substrate} + R_{bond} \tag{2.5}$$

The elements in (2.5) represent:

- R_S is the resistance associated to the source;
- R_{ch} is the channel resistance;
- R_{acc} is the accumulation resistance;
- R_{body} is the body areas resistance;
- R_{drift} is the drift resistance;
- $R_{substrate}$ is the substrate resistance;
- R_{bond} is the bond resistance.

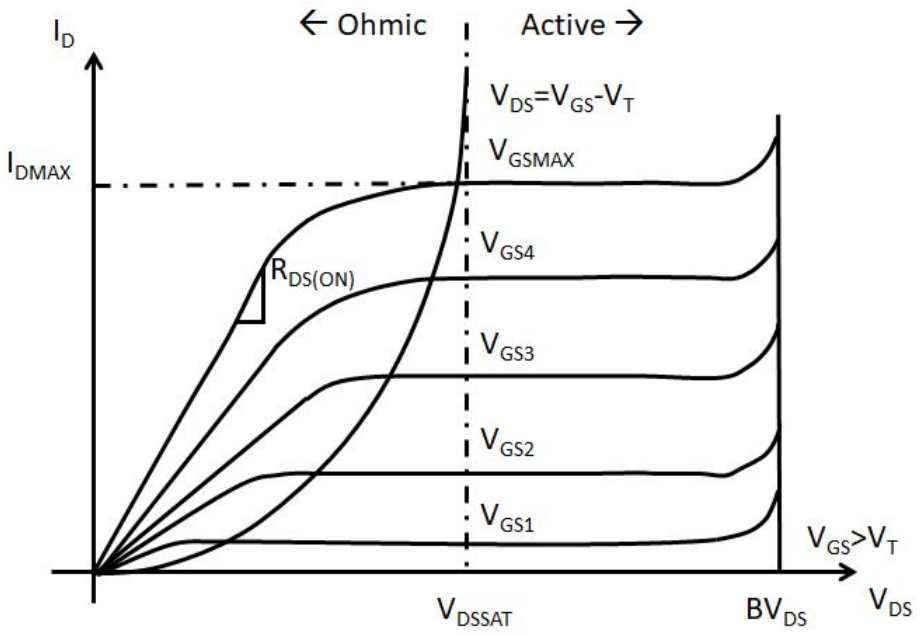

Figure 2.8: Output characteristic of the power MOSFET.

The value of such a resistance is also computable through output characteristic reported in Figure 2.8:

$$R_{DS(ON)} = \frac{V_{DS}}{I_D} \tag{2.6}$$

The ON-state resistance of the power MOSFET decreases when V_{GS} increases. $R_{DS(ON)}$ is important to evaluate the parallel between power MOSFETs, where the MOSFET with a lower $R_{DS(ON)}$ conducts higher current. If V_{GS} reaches higher levels than V_{GSMAX}, this entails the breaking of Oxide and, consequently, of the device, whereas V_{DSSAT} divides the operating regions in two. BV is the V_{DS} voltage that entails the device breakdown. High V_{DS} levels are acceptable in the designing phase under particular precautions. Now, having identified $R_{DS(ON)}$, the dissipated power in ON-state P_D can simply be calculated by using (2.7).

$$P_D = R_{DS(ON)} I_D^2 = V_{DS} I_D \tag{2.7}$$

P_D calculation given by (2.7), even if banal, proves important, since the result would have been achieved by exploiting SOA and the temperatures involved. As a matter of fact, P_D can be calculated from Figure 2.9 as from (2.8). In (2.8), to calculate the potential power dissipation, reference is made to the junction temperature T_j and to the case temperature T_c by introducing the concept of thermal impedance Z_{TH}. Still in (2.8), it is possible to see how to obtain the value of the power P_D without resort to voltages and currents, but rather by exploiting temperatures and thermal impedances. More details about Z_{TH} will be given in Chapter 2.

$$P_D = \frac{(T_j - T_c)}{Z_{TH(j-c)}} \tag{2.8}$$

In Figure 2.9 the SOA limits can be identified through:

1. $R_{DS(ON)}$ given by the relation between the voltage V_{DS} and the current I_D;
2. electro thermal stability, given by the level of high V_{DS}, as compared to a relatively low I_D;
3. P_D given by the dissipated power and seen as the product of I_D and V_{DS} deriving from a variable length impulse (the shorter it is, the higher P_D can be);

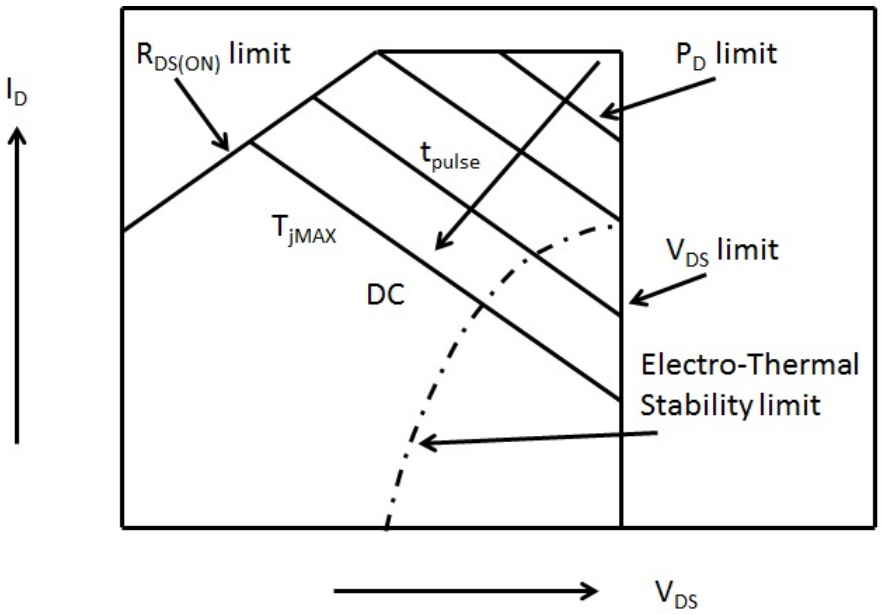

Figure 2.9: Typical SOA of a power MOSFET.

4. T_{jMAX}, junction temperature, which is a limit analogous to that imposed for P_D under continuous current.

Therefore, in order to comply with the SOA, the duration of the pulse applied to power MOSFET makes the power-defined limit variable. Higher power, thus, can be injected only if it is generated by shorter pulses. It could seem obvious, but reliability of a power device comes from the use of the device by ensuring SOA.

2.2.2 CoolMOS™ ON-state resistance

In 2001, Infineon Technologies AG introduced a new Power MOSFET technology named CoolMOS™, which implements a new structure in the vertical drift region, which permits to reduce the ON-state resistance. Hence, a CoolMOS, can manage twice or more P_D than a conventional power MOSFET, the package being equal.
The ON-state resistance $R_{DS(ON)}$ must be redrafted as in (2.9).

$$R_{DS(ON)} = BV^{i_K} \tag{2.9}$$

Here i_K is a constant $(2.4 \div 2.6)$ [7]. By comparing the resistance $R_{DS(ON)}$ of a conventional power MOSFET to that of a CoolMOS, from a theoretical point of view, (2.10) can be written, whereas from an experimental point of view [18], (2.11) is obtained.

$$R_{DS(ON,VDMOS)} >= 40 \times R_{DS(ON,COOLMOS)} \tag{2.10}$$

$$R_{DS(ON,VDMOS)} >= 20 \times R_{DS(ON,COOLMOS)} \tag{2.11}$$

Concerning doping, it is typically unvaried for CoolMOS and conventional power MOSFET, except for the N doped drift region. As a matter of fact, for this region, BV being equal, CoolMOS doping is higher. Therefore, CoolMOS has a peculiar almost linear current-voltage with a low threshold voltage. It can substitute conventional power MOSFETs without particular shrewdness, and it is mainly used in power supplies to 2 kVA.

2.2.3 Power MOSFET SPICE Model

The introduction of the Simulation Program with Integrated Circuit Emphasis (SPICE) in 1972 [19] [20] let the electrical and electronic designer simplify the designing process of circuits. By now, SPICE is such a powerful and ascertained tool that it would be unimaginable not to benefit from it. From the initial 1972 version developed in FORTRAN in laboratories by the Electronic Research Laboratory of the University of California at Berkeley, other versions followed SPICE2 [21] and the current 1989 syntax named SPICE3 [22]. SPICE3 was written in C Language. During the years, many freeware and proprietary versions entered the market, which added countless functions to the original SPICE3 by integrating expressive capacities to the language. To give an instance, it should be remembered the freeware implementation of the Linear Technologies LTSPICE [23] and the proprietary implementation of Cadence OrCad PSPICE [24]. However, SPICE simulators, that in the years have become a de-facto standard, need, as any other simulator, accurate models to supply accurate results which were as close as possible to reality. This affects MOSFET SPICE model accuracy, that, for this reason, does not appear appropriate to model a power MOSFET. The typical MOSFET device SPICE model is not sufficiently accurate to realize simulations of circuits based on power MOSFET; the main reason is that the most important devices capacitances are constant and independent from the voltage applied to terminals. An example of SPICE model of a generic MOSFET is shown in Figure 2.10. In the example of Figure 2.10, there are two capacitances depending on the applied voltages, that are C_{BD} and C_{BS}. When considering the short between body and source, only C_{BD} proves to be dependent on voltages. However, in vertical devices, C_{GD} variation to the applied voltage cannot be neglected; therefore, model in Figure 2.10 appears unrealistic for power MOSFETs.

During the last twenty years of the 20th century, numerous power MOSFET SPICE models were suggested, each one with its own peculiarities. Some are more accurate; anyway, their implementative complexity is not to be underestimated by virtue of the solver capacity to simulate the model. As a matter of fact, many solutions of power MOSFET SPICE models use the Behavioral Model (B-Model) or the controlled sources which, as it is well-known, make SPICE simulations complex. In [25]

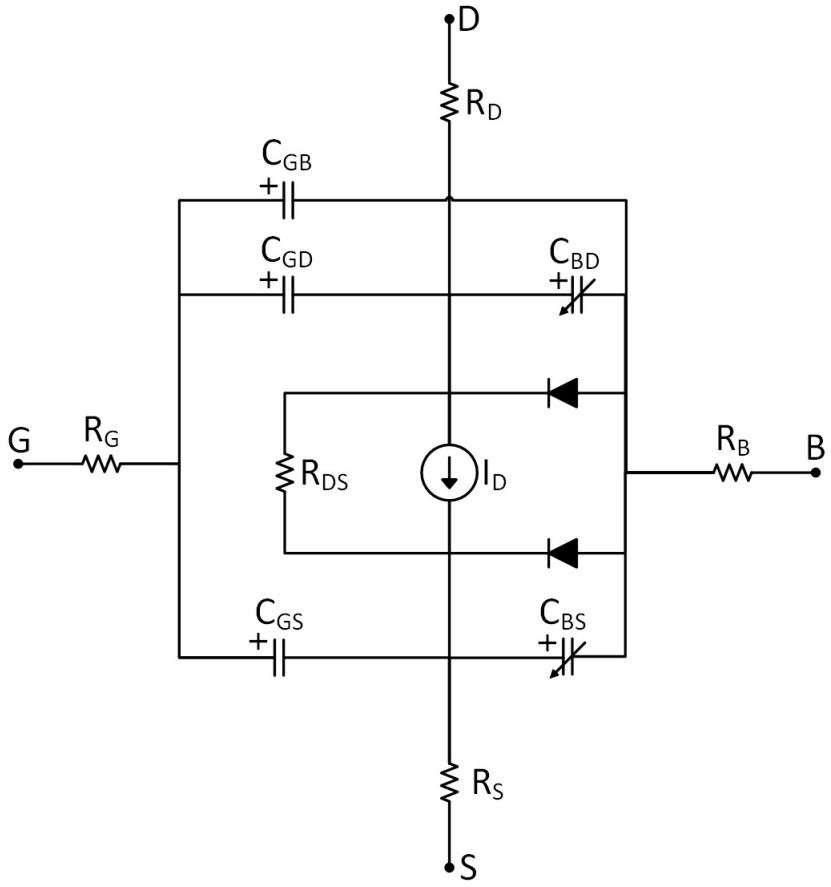

Figure 2.10: Generic MOSFET SPICE model.

examples of power MOSFET model are discussed. From these considerations and from many works about power MOSFET modeling [26][27][28][29], it seems important that the model implements at least C_{GD} dependence to the applied voltage. In the majority of power MOSFET applications (i.e. power converters and switching circuits) also the dependence of applied voltage for C_{GS} is required [30]. Table 2.6 and Table 2.7 present the main works about Power MOSFET SPICE modeling realized during the years. Therefore, Figure 2.11 and Figure 2.12 show the model proposed

Year	**Authors**	**Details**
1980	Nienhaus, Bowers and Herren [31]	Constant capacitance C_{GD}.
1985	Lauritzen and Shi [32]	Problems with high breakdown voltages.
1986	Fay and Sutor [33]	Constant capacitances.
1987	Hancock [34]	Complex model, but accurate.
1988	Simas, Piedade and Freire [35]	Simple with C_{GD} implemented with three capacitances.
1988	Xu and Schroder [36]	Simple, model uses only default MOSFET and BJT SPICE models.
1988	Yee and Lauritzen [26]	C_{GD} voltage dependent and implemented with two capacitances.
1989	Cordonnier, Maimouni, Tranduc, Rossel, Allain and Napieralska [37]	C_{GD} is dependent from voltage and diode is coupled with capacitance.
1991	Hepp and Weatley [38]	Constant capacitances are switched in accordance with operating region.
1991	Melito and Portuese [39]	Simple and quite complete, but temperature is completely neglected.
1991	Scott, Franz and Johnson [40]	Suitable for DMOS and for AC and DC analysis.

Table 2.6: Power MOSFET SPICE models in literature 1980-1991.

Year	Authors	Details
1994	Wheatley, Ronan and Dolny [41]	It uses JFET and there are troubles with turn-OFF.
1995	Budihardjo and Lauritzen [42]	It is necessary to know the internal structure.
1998	Aris, Hulley, Mariun and Sahbudin [43]	Parameters are estimated and it is derived from [26].
1999	Jang, Amborg, Yu and Dutton [44]	Simplest model, it uses a variable R.
1999	Maxim and Maxim [45]	Use of B-Models, but really complex.
2016	Stubenrauch, Seliger and Schmitt-Landsiedel [46]	Implement a method for the extraction of variable capacitances.
2016	Victory, Pearson, Benczkowski, Sarkar, Jang, Yazdi and Mao [47]	Physical model suitable for trench power MOSFET.

Table 2.7: Power MOSFET SPICE models in literature 1994-2016.

by Motorola Inc. [37] in 1989, also known as the Cordonnier Model, which, still nowadays, assumes a role of reference point. Figure 2.11 represents the power MOSFET SPICE model proposed by both [37] and [25], which necessitate an initializing terminal $INIT$ to receive a C_{GDMAX} and D_{GD} initializing step in case of transient simulations, whereas the model in Figure 2.12 [37] is not affected from the issue of the first step, even if considerably more complex.

2.2.4 Notes about smart power modules

During the last years, many intelligent power modules asserted themselves, which incorporate a peripheral circuit and in a power module. The peripheral circuit generally consists of input and output insulation, of interfaces with systems that require power signals, protection diagnostic systems. In other words, the power device gate is controlled through driver incorporated in the module; furthermore, sensors monitoring current, voltage or temperature are present.

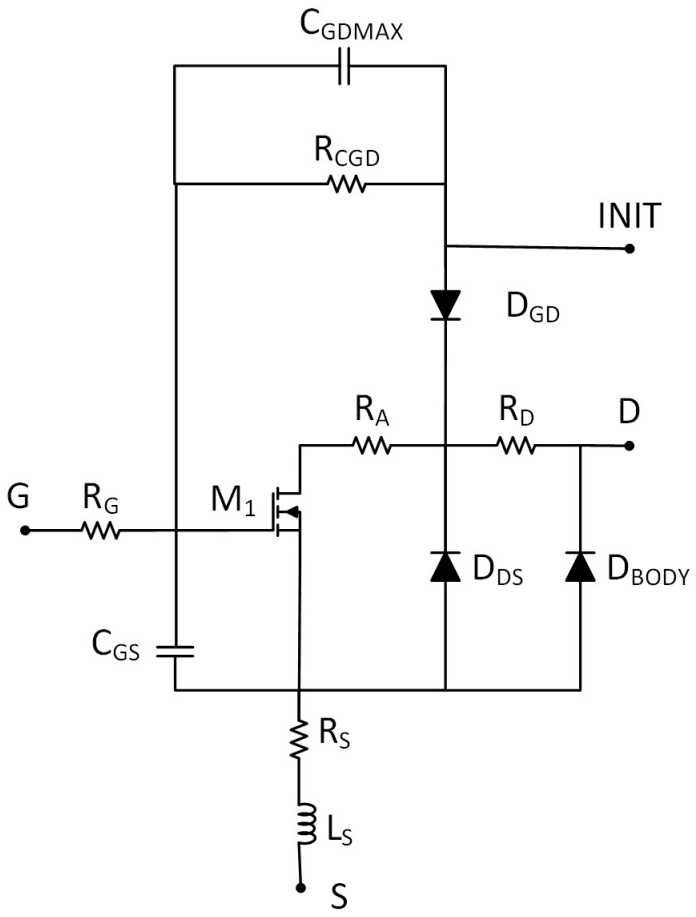

Figure 2.11: Cordonnier power MOSFET model with *INIT* pin for AC study.

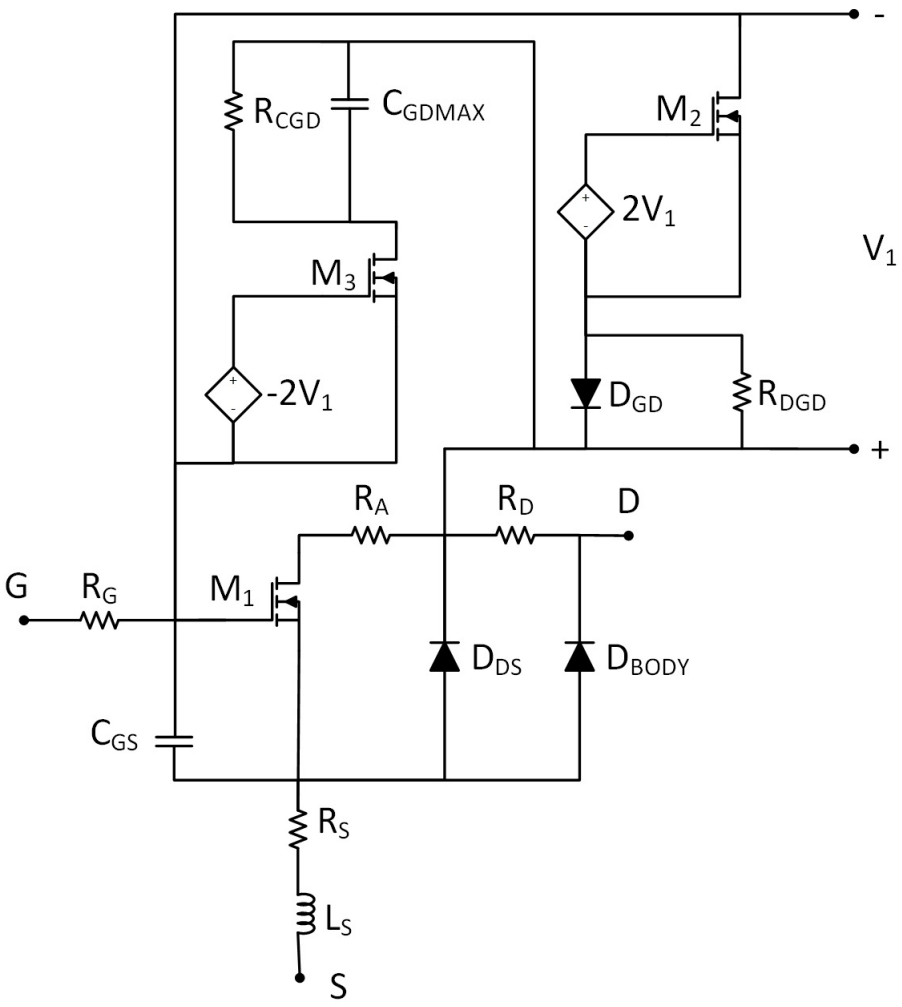

Figure 2.12: Complex Cordonnier power MOSFET model for AC study.

A commercial example of this module, is the Infineon Tecnologies AG PROFET, which is composed by a canonical power MOSFET, and a CMOS logic circuit. Therefore, PROFET products permit a protection in accordance with [7] and [48]:

1. overload;
2. overvoltage;
3. short-circuit;
4. excessive temperature;
5. loss of ground;
6. power supply loss;
7. ElectroStatic Discarge (ESD).

Furthermore, some PROFET modules can give information on:

1. the state;
   (a) temperature;
   (b) open-load;
2. the current.

PROFET modules are widely used in the automotive and industrial applications because their use does not require any additional conditioning or diagnostic circuit, thus making them compact and reliable. Furthermore, given their manageability, they can almost immediately interface to ECU, thus partly reducing the designing time.
To conclude, it is important to notice that this type of commercial products is not suitable for reliability studies, since their use is like that of a black-box. To such an end, to study power circuits, it is necessary that the module is deprived of the peripheral circuit: this could be done only during the production phase, which is clearly possible only for producers.

2.3 Reliability and techniques to improve it

As already seen before, power electronic systems reliability in the automotive and industrial applications is an important issue. This part will give relevance to the system fault causes; the main methodologies for the study of reliability will be explained, and a little analysis on methodology of Zero Defect (ZD) quality management will be proposed. As a matter of fact, in addition to the harsh conditions in which devices should operate, several fault causes can considerably influence the device lifetime. Many breaking causes acquire relevance from thermal cycles or from high temperatures. Even if reliability is a quite intuitive concept, it can be considered as one of the dimensions of quality definition and it must be clearly defined to be measurable, what will be done in this section. Finally, some elements of a methodology for quality increase, such as ZD, will be given.

2.3.1 Fault causes

By taking into consideration data from Figure 2.13 [49], it is possible to see how the main fault cause in electronic devices derives mainly (around 75%) from cycles with high temperature range and from reaching high temperatures at steady state in addition to vibrations and shocks. By taking these data into consideration, it is easily comprehensible how the electro-thermal and thermo-mechanical modeling proved to be an interpretation of the devices and electrical systems reliability. In particular, by referring to Figure 2.14 [50], the main fault causes take place into capacitors and semiconductor, into boards, solder joints [51][52] and connectors, all elements that certainly deteriorate because of thermal cycles, high temperatures and vibrations. Typical power applications make electric loads, vibrations and environmental conditions reduce device lifetime. For instance [53], an electric train can submit the device that controls the engine to $10^6 \div 10^8$ power cycles, thus provoking thermal excursions that easily reach 80 K. Still according to [54], [55] and [56], the main fault typologies concerning devices and power systems can trace back to the following list.

1. Electrical Overstress (EOS), that are the overcurrent and/or overvoltage conditions where the heat generated by the device exceeds its maximum limit. In

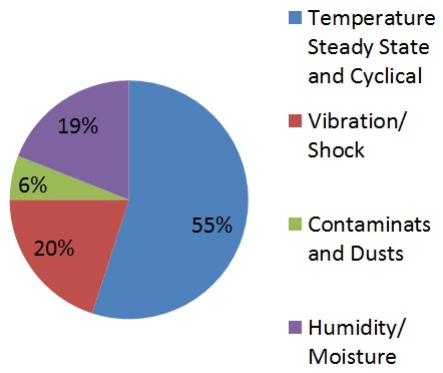

Figure 2.13: Main causes for electronic devices breakdown.

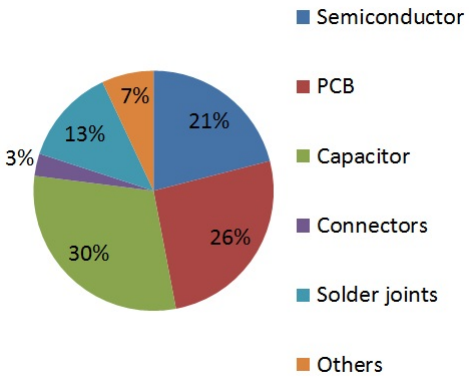

Figure 2.14: Classification of the main breakdowns for parts that undergo a damage.

such conditions, it is necessary to verify and attentively conform to the SOA and, eventually, insert a heat sink, according to applicative specifics. Depending on the type of device, the secondary breakdown or the undesired ignition can take place.

2. ElectroStatic Discharge (ESD), that is an EOS subset where electrostatic discharges can damage the device through rapid overvoltages and overcurrents. Devices may be completely damaged and keep on working for a significant period of time which is, however, reduced if compared to their common lifetime.

3. Latch-Up and triggering of parasitics, that are high voltage variations that can turn on the parasitic devices present in the structure of power devices.

4. Charge effects, mainly due to the electric field distortion caused by the accumulation of ionic contaminants and by the progressive degradation of gate oxide. This cause can be observed only in MOSFETs, the effect of which being a progressive deterioration of threshold voltages and current dissipation performances.

5. Electromigration, due to atomic migrations and to mechanic stress during the process of production. It occurs in metallic path and prevents reliability for long periods.

6. Thermal activation, that is the temperature that speeds up power devices degradation, as theorized by Arrhenius's law.

7. External radiation, that are the electromagnetic radiations coming from the magnetic field of the Earth.

8. Packaging type, that are identical devices with different package technologies that can produce different behaviors.

9. Bond wire liftoff, that is the bond breaking due to the crack widening formed in the bond wire and die interface because of the temperature variation and of different thermal coefficients.

10. Solder fatigue, due to the fatigue and successive crack of solder joints between substrate and baseplate, or between chip and substrate.

11. Bond wire heel cracking, that is the contraction and expansion of the bond that can create cracks due to bond wire bending. This type of crack occur mainly after several thermal cycles.

12. Corrosion of the interconnections, that is the corrosion of the aluminium parts due to the exposition to acids and bases.

13. Aluminium reconstruction, that is the phenomenon of terminal reconstruction due to high maximum junction temperatures. Such a phenomenon can occur with both the creation of cavities in the aluminium layer, and the formation of granular extrusions.

14. Crack propagation, it occurs in case of pre-existing flaws in the production phase.

15. Voids, that is the presence of air bubbles (in the solder layer, just to give an instance) that can relevantly (and uncommonly) elevate temperatures, thus incentivizing the creation of cracks.

16. Burnout failures, that is an unespected fault, generally produced by a short circuit inside the device.

17. Cosmic ray, that is a fault generated by cosmic rays.

2.3.2 Reliability concept

As previously explained, power electronic device reliability is a key element. However, the concept of reliability must be clarified and defined in order to be applied during the designing phase. To this end, it is necessary to introduce methodologies and metrics appropriate for reliability evaluation [57]. First of all, the probabilistic concept of reliability is defined likewise to [58], as: *"the probability that a device*

conducts a required function (the one for which it has been built) in defined conditions for a given period of time". Reliability definition can be summarized in (2.12).

$$P_R(T <= t) = F(t) = \int_0^t f_g(\tau) d\tau \tag{2.12}$$

Here $P_R(T <= t)$ is the probability depending on the time that the device takes to fulfill its function before a crack in relation to a time T, while $f_g(t)$ is the probability density function that a damage occurs, and t is the considered period of time. Now, it is necessary to define the probability that a damage may not occur before time t, and this is given by (2.13).

$$R(t) = 1 - F(t) \tag{2.13}$$

Finally, it is possible to define the failure rate $\lambda(t)$ which is particularly relevant since it is considered as a convenient index to comprehend when the damage will occur (2.14).

$$\lambda(t) = \frac{f_g(t)}{R(t)} \tag{2.14}$$

To evaluate the failure rate between two instants of time (t_1 and t_2), (2.15) can be applied.

$$\lambda(t_1, t_2 - t_1) = \frac{R(t_2) - R(t_1)}{(t_2 - t_1) R(t_1)} \tag{2.15}$$

A typical evolution of the failure rate in power electronic devices is indicated by [57] and shown in Figure 2.15. One last note concerns two concepts at the limits of reliability. As a matter of fact, independently from the system typology or the engineering field, a system has an operating life. All considerations concerning reliability are to be elaborated during the operating life time, but two added phenomena subsist:

1. infantile death rate, that is the probability of a damage in the first operating moments. Such a condition is an anomaly which must be attributed to the designing phase and not to the ambient in which the device operates;

2. failure under stress condition, that is the probability of cumulative damage which becomes prevalent once passed the operating life time.

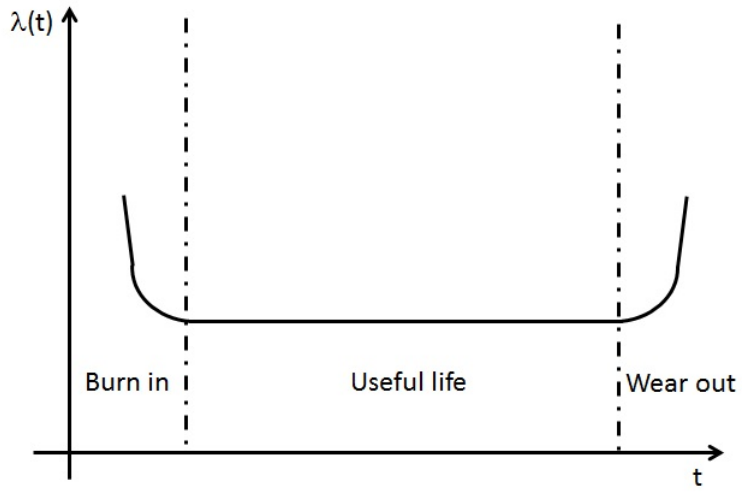

Figure 2.15: Time evolution of the failure rate in power electronic devices.

2.3.3 Evaluation of average availability

Once the failure rate is determined, it is possible to calculate an extremely relevant index that permits to evaluate power electronic devices (and not only) reliability. Such an index is named Mean Time Between Failure (MTTF) and is computable through (2.16).

$$MTTF = \int_0^{+\infty} R(t)dt \tag{2.16}$$

To define the average availability, it is necessary to define the Mean Time To Repair (MTTR) which is conceived as the average time needed to repair the damage. Finally, average availability $\bar{A_v}$ is, therefore, given by (2.17).

$$\bar{A_v} = \frac{MTTF}{MTTF + MTTR} \tag{2.17}$$

2.3.4 Damages analyses and their effects

A useful analysis of damages is given by the Failure Mode and Effect Analysis (FMEA) methodology. Such a methodology permits to analyze the effects of damages

in order to show clear ways to improve reliability. In particular, it permits to highlight, quite objectively, the priorities for an improvement and to conduct a census of all the possible damages by putting them in relation to the effects. This methodology is generic and it can be applied to different levels of details. To conclude, the FMEA is much used in Quality Management Systems (QMS) or in Integrated Management Systems (IMS), and it requires the Priority Risk Number (PRN) computation through the application of (2.18).

$$PRN = Severity \times Occurrence \times Detection \tag{2.18}$$

In (2.18), $Severity$ (evaluation of the worst scenario connected to a deleterious event), $Occurrence$ (evaluation of the probability for an inauspicious event to occur), and $Detection$ (evaluation of the capacity to observe an event) are identified. The Ford Motor Company Inc. started using such a methodology in the middle 70s and now it is a widely used methodology in the automotive sector. A technique conceptually similar to FMEA is the Failure Tree Analysis (FTA). A possible process for the creation of FMEA study in power devices/systems is suggested by [59].

2.3.5 Defects removal and thermal modeling

Automotive industry has always been interested in quality management. Toyota is famous for introducing the Lean Manufacturing as an element of competitive advantage for the production of quality products at contained costs. During the last years, given the relevance assumed by electronic components in vehicles, the concept of quality linked to automotive industry is rapidly involving the semiconductor industry. As a matter of fact, during the '90s, many automotive factories introduced the ZD concepts; consequently, many factories producing electronic components for the automotive, are now developing ZD programs as [60][61][62] show.
By avoiding dealing with the efficiency of ZD as methodology, it is clear that the stress is put on the concept of defects reduction and on the reasons why it is important to aspire to a production of devices without flaws.
The elimination of the defects goes through the design of the device itself. If, on the one hand, Technology Computer Aided Design (TCAD) software tools for devices

design, such as Synopsys Sentaurus [63], are well known by electronic designers, on the other hand, even if thermal effects are well known, thermal simulations appear to be still difficult. However a reliability conscius device design has to take into consideration the thermal behavior.
The use of FEM is a consolidated practice in thermal models simulation; anyway, despite this by-now-consolidated practice, it has some limits that restrict its use:

- the construction of a model is complex;
- long time simulation can occur;
- the designer must be a thermal simulations expert.

Therefore, the approaches presented in this work allow to obtain models that can be rapidly simulated and integrated with electric simulators that can be habitually used by designers.
Specifically, thermal models must take into consideration two main conditions.
The first one, and likely the most common, is to model and simulate the effect of a power step featuring a width compatible with the device functioning ranges. In this case, thermal modeling tries to reproduce the thermal behavior at the system level taking into account the ambient in which it operates. In fact, the ambient and the system external to the device itself influence the device thermal behavior.
The second condition, which is less common but linked to malfunctioning, requires to submit the device to a high width power pulse (out if common usage ranges) during the simulation. This is the case, which may happen during a short circuit: the ambient and the system in which the device operates are neglected, since the heat flux cannot reach the exterior of the device. In this case, extremely high die temperatures occur, while the whole system remains at the ambient temperature.
Therefore, for a designing reliability conscious design, providing tools and methodologies that allow simple simulations, which are fast and accurate at the device/system interesting points, is an essential element.

Chapter 3

Thermal modeling

We should continually be striving to transform every art
into a science: in the process, we advance the art.

– Donald Erwin Knuth

In this chapter, all the necessary elements for the comprehension of the following chapters will be provided. After an overview on the main motivations about the primary role of simulations for the development of power semiconductor devices in automotive sector, thermal modeling techniques will be presented in detail. It is important to remember that thermal modeling has great relevance in reliability conscious design of power systems.

3.1 Heat transfer

Heat transmission is the main thermal phenomenon which involves power electronic systems. Heat transmission, defined by [64], is an energy flow due to temperature gradient. That is to say that, each time a difference in temperature between two points of heat transmission subsists, a heat exchange takes place. Heat transmission physical mechanisms are three:

- conduction, which happens inside the device, or between the package and a heat sink, or between the device package and the PCB;
- convection, which concerns heat transmission between the device, or the power system and the ambient;
- radiation, which is usually negligible at temperatures below 393 K.

3.1.1 Conduction

When a means features a temperature gradient, heat exchange occurs into the means itself through conduction. Where a higher temperature is present, molecules composing the means have a higher energy than molecules featuring lower temperature. When close molecules collide, an energy transfer from those with more energy to those with less energy occurs. Conduction heat transmission can be quantified as in Figure 3.1 by means of the Fourier law. Figure 3.1 represents a monodimensional

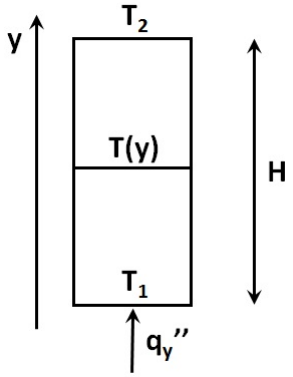

Figure 3.1: Monodimensional body where conduction heat transmission takes place.

solid body by supposing that heat transmission can occur in one direction and that T temperature distribution is linearly proportional to y, therefore $T(y)$. The Fourier law is expressed by equation (3.1) in the unidirectional case, gives the q''_y heat flux per

surface unit in y direction (with $T_2 < T_1$).

$$q''_y = -\lambda \frac{dT}{dy} \tag{3.1}$$

λ is the thermal conductivity, a property of the material costituting the means. Temperature gradient along the $\frac{dT}{dy}$ heat transfer direction can be rewritten in an intuitive way as (3.2).

$$\frac{dT}{dy} = \frac{T_2 - T_1}{H} \tag{3.2}$$

Finally, the quantification of the heat flux exchanged through the surface perpendicular to the q''_y heat flux, is obtained through (3.3).

$$q_y = A \cdot q''_y = -\lambda \frac{T_2 - T_1}{H} \tag{3.3}$$

What has been shown so far is valid in stationary conditions. By the way, it is appropriate to note that, in a 3D system in non-stationary conditions, one has to consider the volume thermal capacity (3.4) which expresses a sort of capacity of the material in gathering energy.

$$C_V = \rho \cdot C_p \tag{3.4}$$

Finally, through (3.5), thermal diffusivity, that is the ratio between thermal conductivity and volume thermal capacity, is defined.

$$\alpha = \frac{\lambda}{\rho \cdot C_p} \tag{3.5}$$

It should be remembered that ρ and C_p are materials properties. Table 3.1 reports the main properties of materials commonly used in power electronic systems.

3.1.2 Convection

Convection is heat transmission between a solid and a fluid. Here, two mechanisms occur which let heat exchange: the first is due to random molecular movements, while the second is linked to the fluid macroscopic motion. Heat exchange through convection can be classified according to the nature of the flux:

Material	**Thermal conductivity λ [W/(mK)]**	**Heat capacity at constant pressure C_p [J/(kgK)]**	**Density ρ [kg/m^3]**
Silicon (Si)	130 [65]	700 [66]	2329 [66]
Glass-reinforced epoxy (FR4)	0.3 [65]	1369 [67]	1850 [67]
Aluminium (Al)	237 [68]	900 [65]	2700 [68]
Copper (Cu)	401 [69]	385 [65]	8960 [69]
Epoxy molding compound	0.731 [70]	1000 [71]	1760 [70]
Solder 60Sn-40Pb	50 [65]	150 [65]	9000 [65]

Table 3.1: Values of thermal properties of the main materials used in power electronic systems.

- forced convection, when the flux is caused by external factors, such as a fan (gas), or a pump (liquids);
- natural convection, when the motion is given by floating forces, which derive from density differences due to the different fluid temperatures.

Figure 3.2 sums up the convection. Hence, heat flux equation per surface unit is given

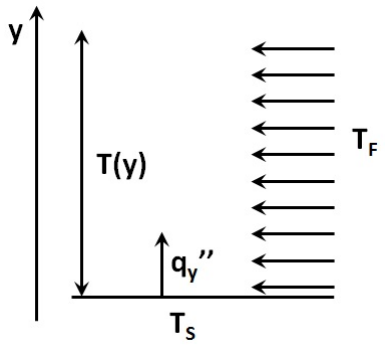

Figure 3.2: Convection, where T_S is the surface temperature of the body, while T_F is the flux temperature.

by (3.6) and is known as the Newton law.

$$q_y'' = h(T_S - T_F) \tag{3.6}$$

where h is the convection thermal exchange coefficient, and condition (3.7) subsists.

$$T_S > T_F \tag{3.7}$$

Table 3.2 [72] reports coefficient h tipycal values under natural and forced convection conditions.

3.1.3 Radiation

All surfaces, at a defined temperature, release energy under the form of electromagnetic waves. So, if no means is present between the different surfaces, heat trans-

Conditions	**Gas convection h [W/(m^{2}K)]**	**Liquid convection h [W/(m^{2}K)]**
Natural convection	2-25	50-1000
Forced convection	25-250	100-20000

Table 3.2: Values of h in natural and forced conditions.

fer occurs through radiation, given that the two surfaces feature different temperatures. Differently from conduction and convection, radiation does not exchange heat through a means, being it the only way in vacuum. The maximum limit at which energy is radiated per unit of surface is called E_{bb} (emissive power of the surface) and is given by the Stefan-Boltzmann law (3.8).

$$E_{BB} = \sigma T_S^4 \tag{3.8}$$

where $\sigma = 5.67 \times 10^8$ W$/$(m^{2}K^4) is the constant of Stefan-Boltzmann and T_S is the surface temperature. If a body could radiate E_{BB}, it would be a black body. Therefore, in real cases (3.9) is more realistic:

$$E = \varepsilon \cdot E_{BB} \tag{3.9}$$

where ε is called emissivity and it varies from 0 to 1. Such value mainly depends on the surface. Contrarily to emissivity E, G radiation can be absorbed, that is to say that energy penetrates a material from other radiant sources (see Figure 3.3). The parameter ζ (absorption coefficient) is defined between 0 and 1 as well; such data let comprehend the quantity of absorbed energy per unit of time and surface (3.10).

$$G_A = \zeta \cdot G \tag{3.10}$$

In case of ζ is greater than one, part of the received energy is reflected. Formula in (3.11), giving the net flux per area unit, is obtained under the condition of T_{AMB} different from T_S:

$$q''_{irr} = \varepsilon\sigma(T_S^4 - T_{AMB}^4) \tag{3.11}$$

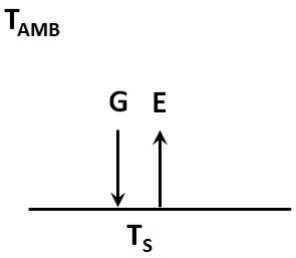

Figure 3.3: Effects of E with emissivity coefficient ε and G with absorption coefficient ζ on a surface at T_S in an ambient at T_{AMB}.

Finally, the net heat exchange occurring on the surface taken into consideration can be represented by (3.12).

$$q''_{irr} = h_{irr} A (T_S - T_{AMB}) \tag{3.12}$$

Where h_{irr} is the irradiant thermal exchange coefficient defined by (3.13).

$$h_{irr} = \varepsilon \sigma (T_S + T_{AMB})(T_S^2 + T_{AMB}^2) \tag{3.13}$$

3.1.4 Preliminary considerations on thermal modeling

When modeling the thermal behavior of a power device, it is necessary to keep in mind that, in simulations, an energetic balance in the unit of time must always subsist; therefore, (3.14) must always be valid, in every instant.

$$\dot{E}_i + \dot{E}_g = \dot{E}_u + \dot{E}_{acc} \tag{3.14}$$

In (3.14), and by the help of Figure 3.4, $\dot{E}_i$ is defined as in-coming energy, $\dot{E}_u$ as out-coming energy, $\dot{E}_g$ as the energy generated inside the system, and $\dot{E}_{acc}$ as the energy accumulated inside the system. It is worth noting that the last term, in a stationary system, equals 0; therefore (3.14), in stationary conditions, is expressed by (3.15).

$$\dot{E}_i + \dot{E}_g = \dot{E}_u \tag{3.15}$$

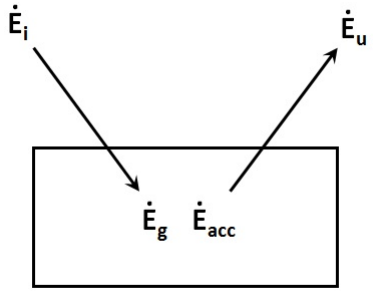

Figure 3.4: Energy conservation in each time instant.

In each real system, there are boundary and initial conditions which must be necessarily taken into consideration:

- system initial temperature T_0;
- T_{AMB}, ambient temperature where the system works;
- presence of uniform T_S temperature surfaces;
- presence of adiabatic surfaces which prevent heat exchange.

By exemplifying the role of thermal modeling in electronics, Figure 3.5 presents a simple power electronic system composed by a MOSFET device in SO-8 bond-less [73] package and by a PCB in FR4 with copper traces. If such a system were placed in the air, which means kept suspended, the following conditions would occur:

- the system initial temperature T_0 is, most likely, the same as the ambient one T_{AMB};
- convection will be substantial only on horizontal faces, that is on the top and on the bottom of the PCB;
- h convection coefficient will be different from the top and from the bottom of the PCB;

- power generated internally the device will equal the power out-coming through convective surfaces.

By supposing that the inferior surface of the PCB is placed on a Peltier cell, in the model, the inferior surface should be placed at a uniform and constant temperature; given the case where a glass wool layer is interposed, it should be considered as an isolated surface. To conclude, h convection coefficient will be considered uniform only in case of forced convection; differently, under natural convection conditions, the coefficient will not be uniform anymore.

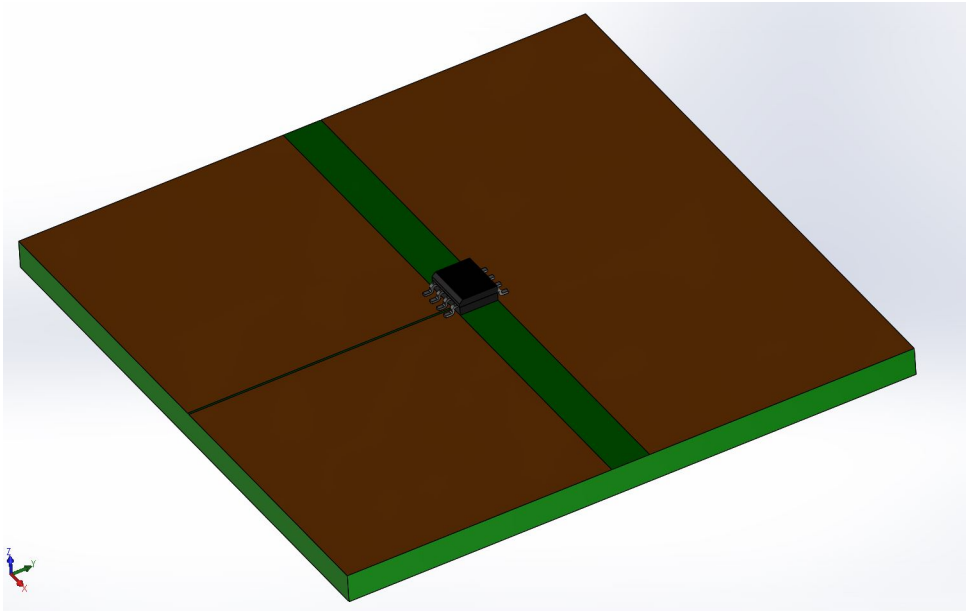

Figure 3.5: MOSFET in SO-8 bond-less package mounted on a FR-4 PCB.

3.2 Modeling physical systems

By considering thermal phenomena as physical phenomena, thermal modeling can be considered as a subset of physical modeling. In general terms, from a mathematic point of view, it is possible to assume that the creation of a model inevitably entails

approximations as compared to a physical real model. As a matter of fact, Figure 3.6 shows how to achieve a numerical model, where errors are introduced [74]. By not lingering on the meaning of each error, a systematic approach to model creation that can be used in physical-based simulations will be proposed.

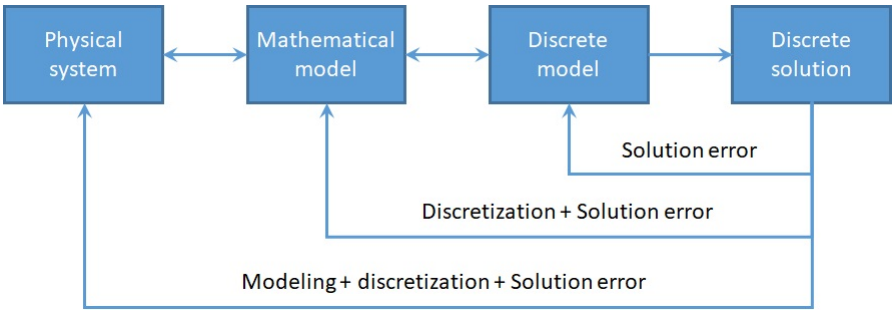

Figure 3.6: A simplified view of the physical modeling process.

3.2.1 Modeling a device

An electronic device can be considered as the totality of the parts which is composed. Each part of the device, in addition to a specific function inside the device, is marked by some physical peculiarities which are linked to the material by which it is composed, to its dimensions and shapes, and to the boundary conditions applied. Each part inside the device interacts with the others by influencing their behavior. Therefore, each part can be seen as a set of physical characteristics linked to the materials by which it is composed, expressed through parameters, by a set of geometrical shapes characterized by dimensions and positioning, and boundary conditions described through parameters at their turn.
Hence, in a typical electronic device, systems and sub-systems can be identified [75]. As the same device can be seen as a sub-system of a more complex system, parts of the same device can be joined and can be seen as a sub-system of the entire device system. By following this logical scheme, it is plausible to consider decomposing whatever system (the physical behavior of which we need to model and simulate) in several sub-systems, each one composed by one or more parts. The atomic element

of a system is a part. In turn, this part can be, if possible, decomposed in other parts, and, in this case, the part would be a sub-system. The fact that a part should be considered as a sub-system is due to the desired granularity in describing the model, or to known information. Therefore, sets of parts that compose the sub-system can be described as an equivalent part that, for the purpose of an overall simulation of the system, does not insert variations. It is important to identify a part as a set of geometrical shapes interconnected and all composed by the same material, where the applied surrounding conditions are mutually compatible. Furthermore, an equivalent part is characterized by boundary conditions originating from the parts of which it is composed, which necessarily must be mutually compatible; the connection amongst shapes must endure; anyway, materials can be substituted by a material featuring physical peculiarities that let the system maintain the same behavior. This hierarchy in modeling can be easily defined through a Unified Modeling Language (UML) class diagram. Therefore, each part is represented by a class where materials, shapes and boundary conditions are features clearly represented by classes in their turn. One or more parts are owned by a sub-system that, in its turn, is represented by a class, while the set of several sub-systems forms the overall system.
Figure 3.7 shows an example of subdivision by following what has been explained above, which lets conceptualize interaction among parts. Such a structure, if properly described, can prove useful for three reasons:

- possibility to realize FMEA [76][77];
- knowledge management amongst several applications/people [78];
- models generation in an automatic or semi-automatic way [78].

If we place, side by side, the suggested decomposition and a function decomposition, a model is implemented which becomes a complete support for FMEA [79]. The concept of function decomposition is very similar to system decomposition, but, instead of seeing the device as a system composed by several sub-systems and parts, the device is seen as a function composed by sub-functions, subdivided in tasks. Even in this case, if we do not know the details, it is possible to make reference to the generic

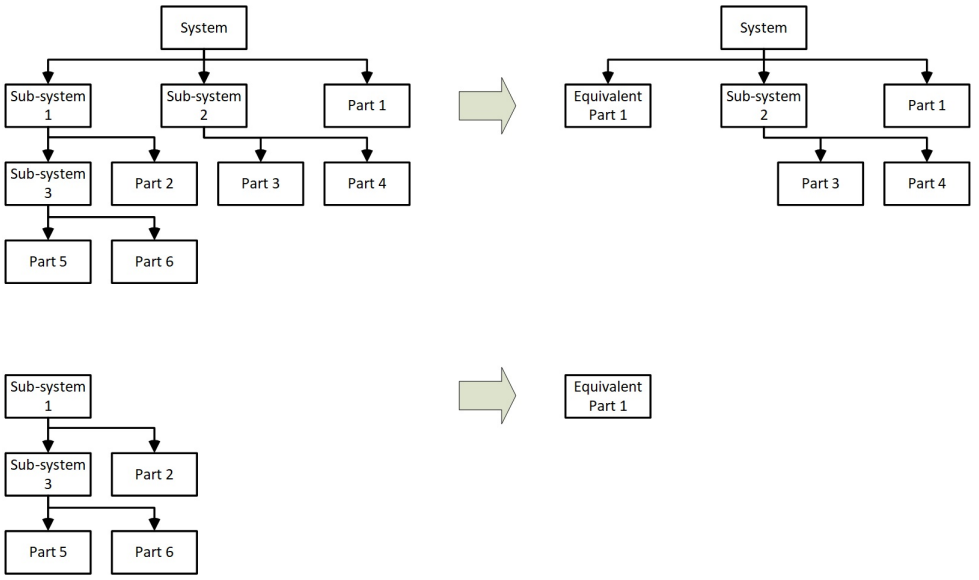

Figure 3.7: Example of System decomposition in Sub-systems and Parts. In the example of the figure, the entire system is re-designed by substituting a Sub-system with an Equivalent Part. Each tangle represents a class, the features of which have been omitted.

equivalent task which aims at summing up several tasks of which we do not know the detail in a task that appears as a sub-function.
A fictitious example is given by Figure 3.8. This way, there will be a relation between Tasks and Parts. Each Part will have one or more Tasks and each Task will have one or more Parts. It is worth noting that the minimum cardinality of the relations is one and not zero in both ways; in addition, it is also important to note that a Task can be fulfilled by several Parts and that each Part can fulfill several Tasks. Finally, it is necessary to consider the fact that no relation subsists among systems and functions. Figure 3.8 shows an example of relations between Tasks and Parts.

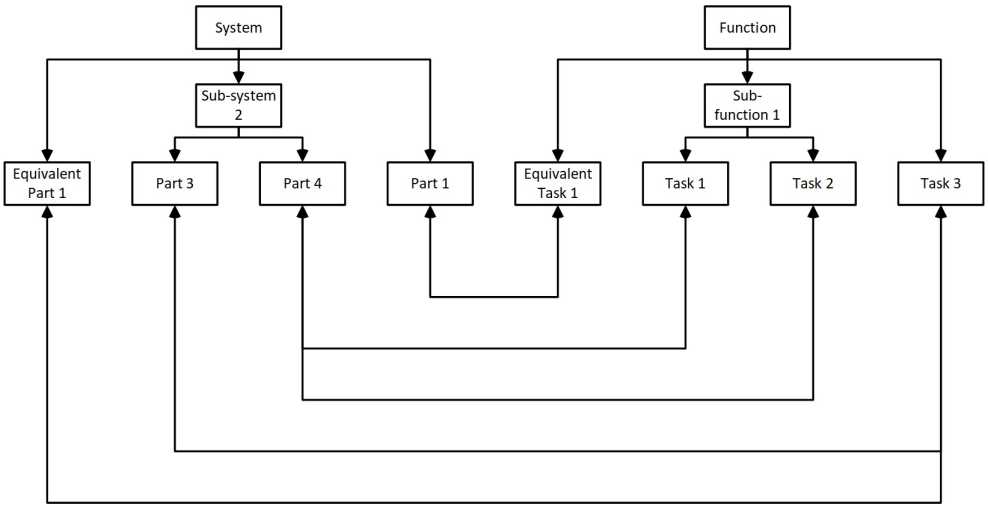

Figure 3.8: Example of System decomposition and Function decomposition and the relationship between Parts and Tasks.

3.2.2 An example of simplified modeling

The concept of parts decomposition, even if not explicitly realized, is implicitly realized every time a power electronic device model for a modern FEM tool is created. In fact, as the created models are based on one or more physics, the mental process

of the model expert guided by the software tool is comparable to a decomposition. The same tools often furnish features that let create selections, which are nothing else than sort of sub-systems. Differently from what has been proposed, FEM tools generally cover up the subdivision per class, thus privileging a hierarchy created through a set-theory logic. A concrete example of subdivision is shown in [80] where a MOSFET in package SO-8 has been proposed, even if widely simplified. Even if in [80] an explicit part decomposition has been realized, it has been, de facto, carried out to get to a simplified model. The use of decomposition, in addition to the advantages already explained before, is remarkably interesting for the purpose of didactics. As a matter of fact, as modeling a device can seem intuitive, decomposition permits to create orderly models, which are also easy to be read by the less expert users or those who are not familiar with simulations. The result is that part decomposition is an interface to machine-human and machine-machine cooperativeness.

Generally, to simulate systems with complex geometries, it is necessary to develop a simplified model in order to allow fast simulations. In [80], a methodology to build simplified models of electronic power components through the simplification of a complex FE model is presented. Such a simplified model is used in a complex power module model. The detailed model is first validated in terms of thermal behavior. In particular, in [80], 3 simplifications on 3 components are actuated, but, for the purpose of this work, only the parts of the power MOSFET are analyzed.

In [80], the simplified models are built once the detailed model of a single component is simulated with a good agreement on the real system thermal behavior. Then, the simplified model is validated through the thermal behavior of the detailed model. The MOSFET in SO-8 package without internal bondwire is modeled through a three layers structure, a great simplification of the original structure.

Figure 3.9 [80] shows the real device, a bondless SO-8 STS12NH3LL power MOSFET, the main characteristics of which are known, either from optical and SEM (Scanning Electron Microscopy) inspection.

In [80], the drain and source contacts are connected through metal flanges, while in the gate contact a bond wire is used. The 3D accurated geometry is shown in Figure 3.10. One of the simplifications is in the silicon die that could be considered as an

uniform heat-source. In the model, unkwown parameters are extracted through fitting experimental data.
The accurated model of the MOSFET is already a simplified model, but this kind of geometry includes a lot of details. In order to further simplify the model, the simplified model of Figure 3.11 is developed. In that model, the entire device is modeled through three layers with parallelepiped shape:

- Epoxy;
- Q Generation;
- Interconnection.

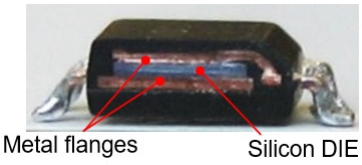

Figure 3.9: Power MOSFET SO-8 STS12NH3LL, partly decapsulated.

Figure 3.10: Power MOSFET SO-8 STS12NH3LL 3D geometry (in section).

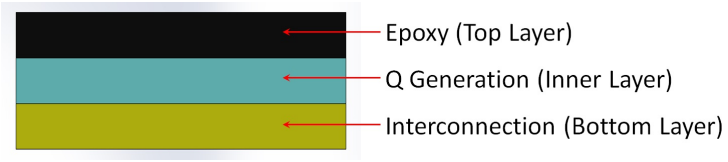

Figure 3.11: Power MOSFET SO-8 STS12NH3LL simplified geometry.

Each of the three layer of Figure 3.11 has the same external surfaces as the real package, but each layer models more than one part of the original system. Therefore, every layer represents an equivalent part. Finally, [80] demonstrates that accurate simulation results are reached with this simplified model, with a great advantage in computation time, where a complex system, with many devices has to be simulated.

3.3 The Finite Element Analysis process

The use of the Finite Element Analysis (FEA) in the electric-thermal-mechanical study of devices and power electronic systems has already become a consolidated reality. In particular, the Finite Element Method (FEM) has facilitated the production of studies about the reliability of such devices and systems, which are very accurate and complete [80]. The process linked to FEM is composed by six steps; nevertheless, in modern tools, FEM software is assimilated into one single step, thus making it totally transparent to the user. The process linked to modern FEM software tools can be summed up as follows:

1. Pre-processing: grid geometries, materials, boundary conditions, loads and dimensions are defined by the user.

2. Numerical analysis: the FEM tool solves the problem through the six steps listed in the following.

3. Post-processing: results are shown under a graphic or table form.

The FEM process, as implemented by the preceding point 2 (Numerical analysis), is decomposable into six steps, as follows [81]:

1. Division of the structure into discrete elements: the structure is subdivided into elements which must fit the structure itself [82].

2. Choice of a proper method of interpolation: some suitable structures are identified to locate the solution, which must respect some convergence parameters. Generally, the model of interpolation has a polynomial form.

3. Derivative of the stiffness matrix elements and of load vectors: from the model of interpolation and positioning, the stiffness matrix $[S^{(e)}]$ and the load vectors $[l^{(e)}]$ of element e are identified by deriving them from an appropriate variational principle (i.e. Garlenik's method [83]).

4. Assembling the equation elements to obtain the equilibrium equations: from the formation of the structure, it is possible to formulate equilibrium equations as (3.16).

$$[\bar{S}][\bar{\phi}] = [\bar{l}] \tag{3.16}$$

   where $[\bar{S}]$ is the stiffness matrix, $[\bar{\phi}]$ is the vector of the nodal positioning and $[\bar{l}]$ is the vector of nodal forces of the complete structure.

5. Solution for the unknown nodals: the equilibrium equation is modified in order to keep into consideration the boundary conditions, and is reformulated as (3.17).

$$[S][\phi] = [l] \tag{3.17}$$

   For linear problems, $[\phi]$ vector can be easily found, while, for non-linear problems, the solution can be identified only as a sequence of steps, where matrix $[S]$ and vector $[l]$ are modified.

6. Calculation of strain and stress elements: from the nodal arrangement of the elements, if required, strain and stress elements can be calculated.

The terminology used before is the general one deriving from structural mechanics; in other fields, it can appear slightly different [81]. From a conceptual point of view, the entire process concerning the COMSOL Multiphysics software tool, is represented by Figure 3.12.

3.3.1 FEM to support the designing phase and the value chain

During the last years, particularly as a consequence of the COMSOL Multiphysics 5.0 release software [84], a new trend is trying to establish itself in modernly structured enterprises, which wants to integrate the research and development function

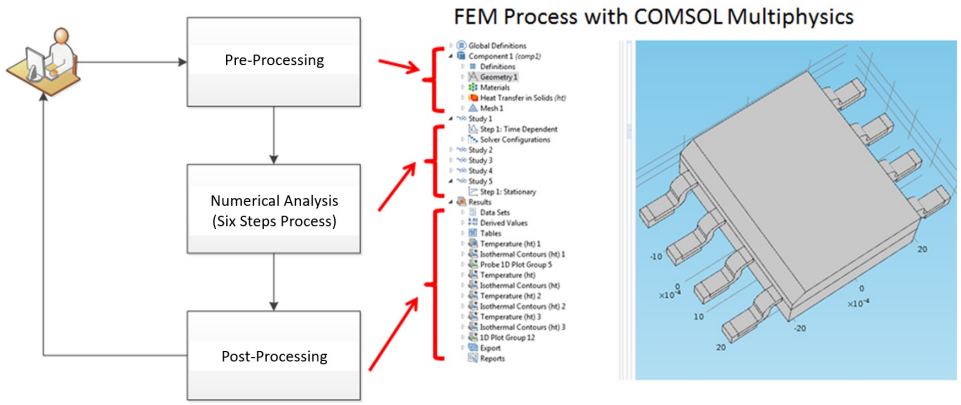

Figure 3.12: Representation of the entire process for the extraction of the solution in the COMSOL Multiphysics FEM software tool.

to production, through engineering. Such an idea is surely interesting and certainly captivating as it would permit to have an FEM software tool supporting the value chain, with consequent advantages in terms of engineering time reduction. Specifically, what research and development produce is already a starting point for engineering, that will be able to create complete executive projects to be integrated with production tools.

Certainly, apart from being a captivating idea, in some cases, it would promote a flexible and made-to-order-based production, where personalized products can be studied in a previous phase to the final designing, and in a relatively shorter time.

Finally, the introduction of the optimization module in COMSOL Multiphysics 4.0 (which has revealed many limitations) shows a certain desire to consider a designing phase which takes into consideration also aspects not merely connected to designing itself, as reliability aspects could be. Figure 3.13 quite clearly sums up the value chain as conceived by the last trends.

Finally, FEM is a way to support industry 4.0 [85].

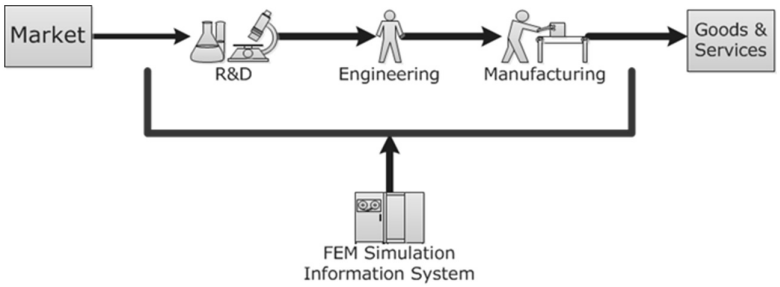

Figure 3.13: Value chain introduced by COMSOL Multiphysics 5.0.

3.3.2 FEM simulation of a simplified Power MOSFET model

The system proposed in Figure 3.14 has been used to develop a simplified FEM model in order to reproduce a system based on power MOSFET STS12NH3LL SO-8 bondless package. Figure 3.14 represents the thermal map of the last time steps of a time-dependent FEM simulation. In such a system, the boundary and initial conditions are the follows:

1. T_0 and T_{AMB} are 293.15 K;
2. h coefficent is 10 $\mathrm{W}/(\mathrm{m}^2\mathrm{K})$ and fixed only on the top of the device package;
3. on the bottom of the device package and pin, the temperature is fixed to T_{AMB};
4. heat source of 5 W in the silicon die volume.

The selected boundary conditions represent a power MOSFET on a Peltier cell in ambient with natural convection conditions. The FEM simulation of the complete system takes about 3 minutes while the proposed simplified system of Figure 3.15 takes about 20 seconds.
In order to build the simplified model the strategy of attempts is use. The attempts start with material value similar to the original one:

1. silicon;
2. epoxy molding compound.

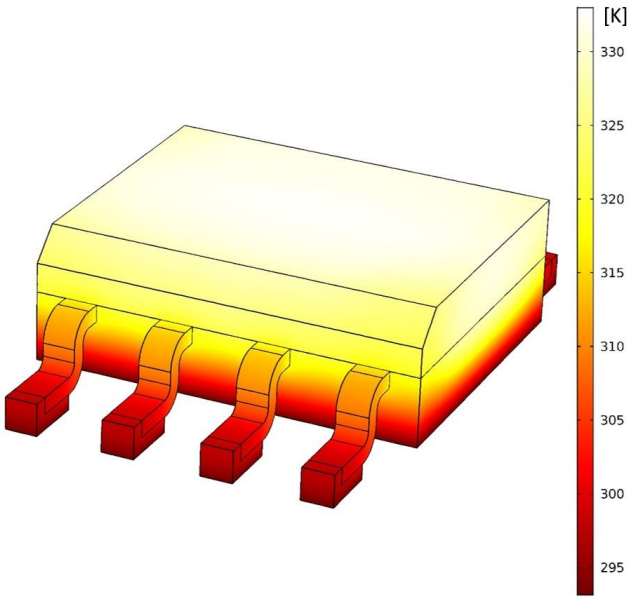

Figure 3.14: FEM COMSOL Multiphysics time dependent simulation thermal map of a detailed Power MOSFET SO-8 STS12NH3LL model at 10000 s.

The boundary conditions are the same. The heat source is put in the inner layer of the three-layer structure while the top surface is subjected to air convection and the bottom surface to a fixed temperature. The result comparison of detailed and simplified

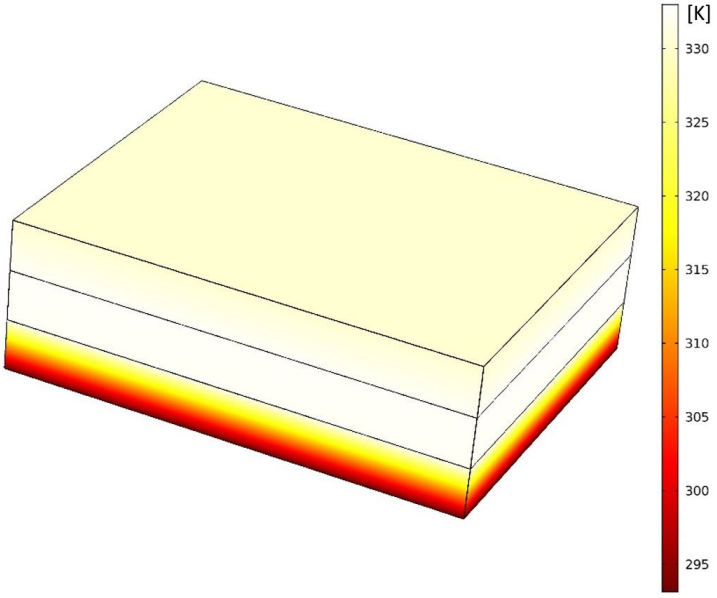

Figure 3.15: FEM COMSOL Multiphysics time dependent simulation thermal-map of a simplified Power MOSFET SO-8 STS12NH3LL model at 10000 s.

simulations are shown in Figure 3.16 and Figure 3.17. Materials paremeters of the simplified FEM Model are shown in Table 3.3. These are simplified in order to allow the creation of a successive Lumped Element Model (LEM).

3.4 Lumped Element Model

The Lumped Element Models, find their origin in electric engineering and supply a concise way to describe an electric circuit. By considering the three passive components of electric circuits (Resistor, Capacity, Inductor), one supposes that each of these components represents the respective properties (Resistance, Capacitance and

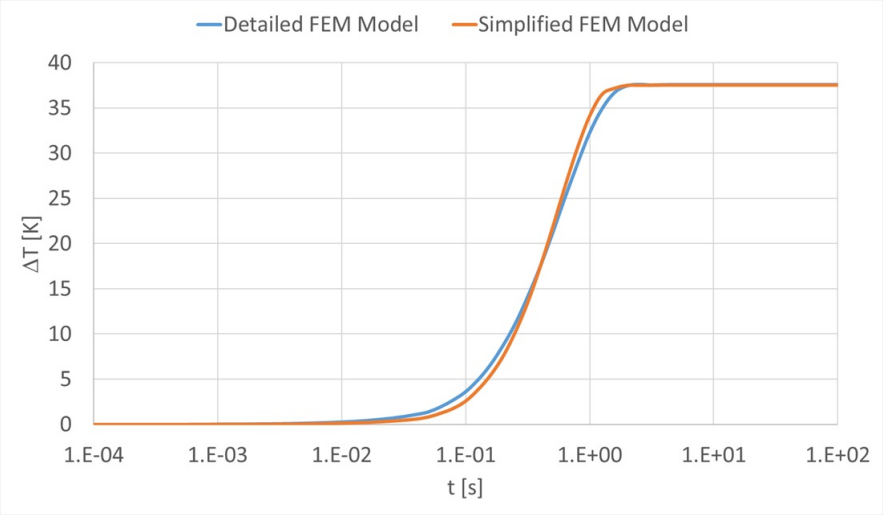

Figure 3.16: Temperature increase over time of the top surface of the detailed FEM model and of the simplified FEM model.

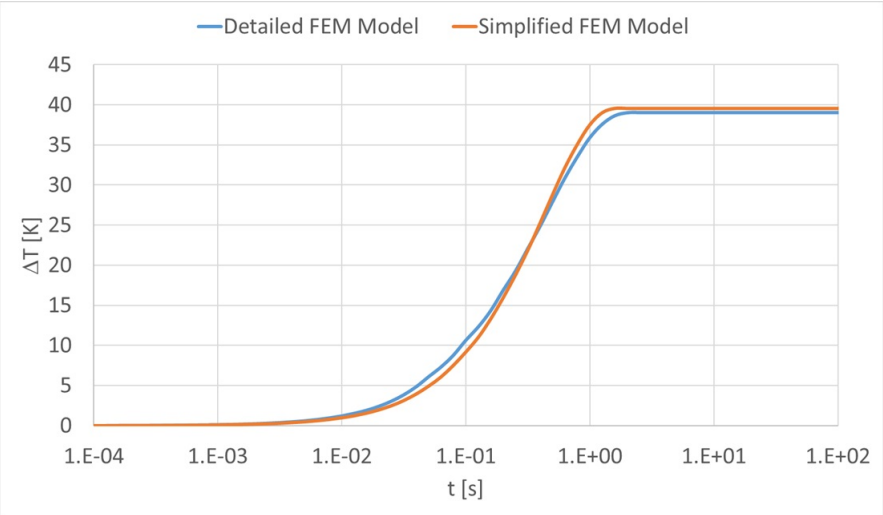

Figure 3.17: Temperature increase over time of inner layer volume of the detailed FEM model and of the simplified FEM model.

Layer	Thermal conductivity λ [W/(mK)]	Heat capacity at constant pressure C_p [J/(kgK)]	Density ρ [kg/m^3]
Inner Layer	600	1700	2329
Top Layer	0.09	50	1760
Bottom Layer	3.5	0.0001	1760

Table 3.3: Values of thermal properties of the simplified FEM model.

Inductance) in a condensed way, that is to say that each component represents its own property in a punctiform way. An eloquent example could be the resistance produced by an electric wire; surely, the resistance varies along its length, increasing with the distance from the starting extremity. In the LEM case, such a resistance is concentrated in just one point. Therefore, the wire inside an electric circuit is considered as a unique component, of which it is impossible to see its dimensions, but that has a resistance that equals its total resistance. Such a wire could also be modeled as a series of resistances, each one concerning a portion of the wire. Considering the multi-resistance model, the same wire could be thought as a multitude of resistances in series.
As already said before, the use of LEMs, apart from being widely used in electric modeling (under determined conditions), is widely widespread in thermal modeling and in other modeling typologies, such as acoustic and mechanic.
The use of LEM methodology entails the following advantages and disadvantages:

1. it simplifies the representation (advantage).
2. it can be manipulated to create equivalent circuits (advantage).
3. it is possible to realize static and dynamic analyses (advantage).
4. loss of information (disadvantage).
5. the results obtained are poor compared to 3D structures (disadvantage).

In case of thermal modeling, two typologies of LEM exist [86] that can represent the static and dynamic thermal behavior of a power device. These are:

1. Foster network representation;
2. Cauer network representation.

Both representations exploit the representational equivalences between electric and thermal problems expressed in Table 3.4.

Electrical Model	**Thermal Model**
Potential difference, V	Thermal difference, T
Electric current, I	Heat flux, P
Charge, Q	Heat, Q
Resistance, R	Thermal resistance, R_{TH}
Capacitance, C	Thermal capacitance, C_{TH}
Inductance, L	-
Kirchhoff's currents law	Thermal energy conservation
Kirchhoff's voltage law	Temperature is relative to the observation point

Table 3.4: Electric and thermal LEM equivalence.

3.4.1 Foster representation

The thermal behavior description of a power device through the Foster network representation takes place by positioning $R_{TH}C_{TH}$ paralleled couples in series. An example of such a representation is shown in Figure 3.18. Such a representation is very useful from a mathematic point of view. Anyway, it does not represent the thermal physics at intermediate points T_2 and T_3, but only at extreme points T_1 and T_4. Therefore, temperatures (or their evolution) of such a representation can be used to exclusively represent:

1. stationary conditions;

2. thermal impedance evolution.

This representation cannot be used for direct conversions from the real world to the model. The calculated thermal resistance and capacitance of the Foster network representation has not relationship with the materials of the system.

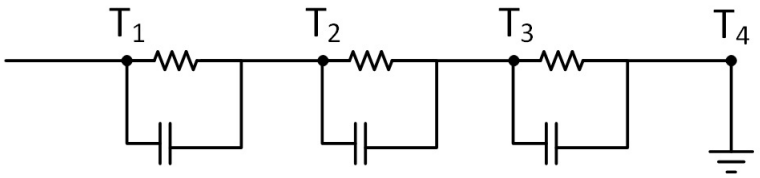

Figure 3.18: Example of Foster network representation.

3.4.2 Cauer representation

The representation through a Cauer network takes place by inserting in series couples $R_{TH}C_{TH}$ in series, where capacitance is directly connected to the ground. In this case, each intermediate point takes on significance; anyway, this cannot be used for the creation of a model starting only from the impedance evolution because it is not so easily calculable. Therefore, the Cauer representation is useful to represent:

1. stationary conditions;

2. conversion of the real world directly into a LEM model.

Figure 3.19 shows an example of Cauer network.

3.4.3 Transformation of representations

From a mathematic point of view, Foster representation can be described by (3.18), where the general case (N nodes $R_{TH}C_{TH}$) is explained.

$$Z_{TH}(t) = \sum_{i=1}^{N} R_{TH,i}(1 - \exp(-\frac{t}{\tau_i})) \tag{3.18}$$

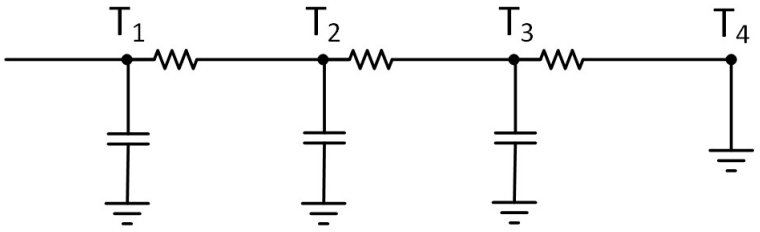

Figure 3.19: Example of Cauer network representation.

One should remember that $\tau_i = R_{TH,i}C_{TH,i}$ where, obviously, $R_{TH,i}$ and $C_{TH,i}$ represent the thermal resistance and capacitance of each i-th node $R_{TH}C_{TH}$, where N is the maximum number of nodes of a representation through the Foster network.
The transformation presented in the follow are evolutions of the work presented in [87].

From Cauer to Foster representation

The generation of a Foster representation from a Cauer representation is a recursive algorithm where, at each recursive step, the same method is applied as in Figure 3.20. In the transformation from a representation to the other, the first impedance equals zero. Therefore, to calculate the Foster representation from a Cauer representation, it

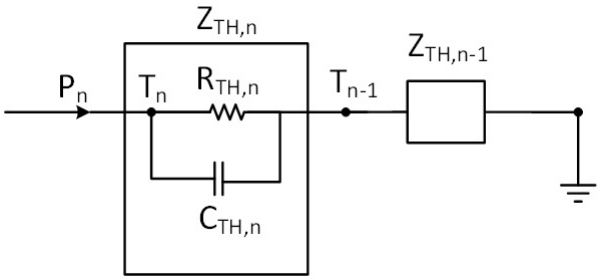

Figure 3.20: Step of the recursive algorithm for Cauer and Foster conversion representation.

is necessary to apply (3.19):

$$Z_{THF}(s) = \sum_{j=1}^{N} \frac{1}{(C_{TH,j}(s - s_j))} \tag{3.19}$$

where $s_j = -1/\tau_j$ and $\tau_j = R_{TH,j}C_{TH,j}$. At its turn Z_{THF}, is given by (3.20):

$$Z_{THF}(s) = Z_{THF,n} = \frac{1}{sC_{TH,n} + \frac{1}{R_{TH,n}}} + Z_{THF,n-1}(s) = \frac{T_n(s)}{P_n(s)} \tag{3.20}$$

Concerning $T(s)$ and $P(s)$, they are just the Laplace transformations of $T(t)$ and $P(t)$, as is in (3.21) and (3.22); respectively:

$$T(s) = \mathscr{L}\{T(t)\} = \int_0^\infty T(t)\exp(-st)dt \tag{3.21}$$

$$P(s) = \mathscr{L}\{P(t)\} = \int_0^\infty P(t)\exp(-st)dt \tag{3.22}$$

while $T(t)$ and $P(t)$, if $T(0)$ is equals to zero, they are calculated from (3.23) and (3.24); respectively:

$$T_n(t) = \int_0^t P_n(\tau)Z_{THF,n}(t-\tau)d\tau \tag{3.23}$$

$$P_n(t) = \frac{(T_n(t) - Tn - 1(t))}{R_{TH,n}} + C_{TH,n}\frac{d(T_n(t) - T_{n-1}(t))}{dt} \tag{3.24}$$

Finally, to be thorough, (3.25) and (3.26) are reported:

$$T_n(s) = P_n(s)Z_{THF,n}(s) \tag{3.25}$$

$$P_n(s) = \frac{(T_n(s) - T_{n-1}(s))}{R_n} + sC_n(T_n(s) - T_{n-1}(s)) \tag{3.26}$$

From Foster to Cauer representation

For what concerns the conversion from Foster to Cauer representation, it is helpful to resort to Figure 3.21. The process is always recursive and the starting point is the impedance Foster representation Z_{THF}, which is equaled to the Cauer one Z_{THC} (3.27).

$$Z_{THC}(s) = Z_{THF}(s) \tag{3.27}$$

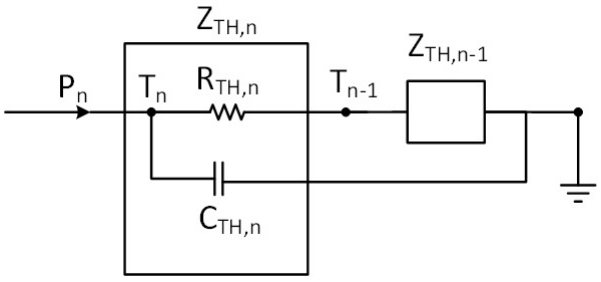

Figure 3.21: Step of the recursive algorithm for Cauer and Foster conversion representation.

At this point, by taking into consideration Figure 3.21, it is easy to understand that expression (3.28) describes the Cauer representation of the impedance reciprocal:

$$\frac{1}{Z_{THC,n}(s)} = sC'_{TH,n} + \frac{1}{R'_{TH,n} + Z_{THC,n-1}(s)} = \frac{q_n(s)}{p_n(s)} \tag{3.28}$$

One should remember that $q_n(s)$ and $p_n(s)$ are the polynomial decomposition following $Z_{THF}(s)$ Euclid's algorithm. By keeping into consideration (3.28), and by assuming the degree $q'_n(s)$ lower than the degree $p_n(s)$, it is possible to write:

$$\frac{q_n(s)}{p_n(s)} = sC_{TH,n} + k_n + \frac{q'_n(s)}{p_n(s)} \tag{3.29}$$

$$k_n + \frac{q'_n(s)}{p_n(s)} = \frac{1}{\frac{p_n(s)}{k_n p_n(s) + q'_n(s)}} \tag{3.30}$$

By using the identity of (3.30), it is possible to obtain (3.31).

$$\frac{p_n(s)}{k_n p_n(s) + q'_n(s)} = R'_{TH,n} + Z_{THC,n-1}(s) \tag{3.31}$$

From (3.31), the results (3.32), (3.33) and (3.34) can be obtained; these are necessary to get the algorithm final results.

$$R'_{TH,n} = \frac{1}{k_n} \tag{3.32}$$

$$q_{n-1}(s) = k_n p_n(s) + q'_n(s) \tag{3.33}$$

$$p_{n-1}(s) = -\frac{q'_n(s)}{k_n} \tag{3.34}$$

Finally, (3.35), (3.36), (3.37), (3.38) and (3.39) are represented:

$$Z_{THC,n}(s) = \frac{1}{sC'_n + \frac{1}{R'_{TH,n} + Z_{THC,n-1}(s)}} = \frac{T_n(s)}{P_n(s)} \tag{3.35}$$

$$T_n(s) = P_n(s) Z_{THC,n}(s) \tag{3.36}$$

$$P_n(s) = \frac{(T_n(s) - T_{n-1}(s)}{R'_n} + sC'_n T_n(s) \tag{3.37}$$

$$T_n(t) = \int_0^t P_n(\tau) Z_{THC,n}(t-\tau) d\tau \tag{3.38}$$

$$P_n(t) = \frac{(T_n(t) - T_{n-1}(t))}{R_n} + C'_n \frac{dT_n(t)}{dt} \tag{3.39}$$

3.4.4 LEM representation of FEM

First of all, the Cauer representation of the simplified model presented in the preceding section through the formula can be estracted easily. In fact with the knownledge of the materials is possible to calculate the thermal resistance and capacitance of every node of the Cauer network that represents the thermal impedance from the heat source to the ambient. This stategy is possible only with the defined boundary conditions of the system of Figure 3.15, with the help of Table 3.3.
The Cauer thermal network that represents the thermal impedance from the inner layer to the air convection (through the top layer) is composed by 3 stages:

1. a thermal resistance and a thermal capacitance representing an half of the inner layer of Figure 3.15;

2. a thermal resistance and a thermal capacitance representing an half of the top layer of Figure 3.15;

3. a thermal resistance representing the air convection.

The thermal resistance of the inner layer and of the top layer is given by:

$$R_{TH,cond} = \frac{A}{H \times \lambda} \tag{3.40}$$

where H is the thickness of the layer, A is the face area of the layer and λ is the thermal conductivity. For both layers the thickness is 0.55 mm, while the area is 20 mm^2. In the case of the inner layer, it is considered only an half of the thickness.
The thermal capacitance is calculated by:

$$C_{TH,cond} = m \times C_p = V \times \rho \times C_p = H \times A \times \rho \times C_p \tag{3.41}$$

where m is the mass calculated through density ρ and volume V. For the inner layer the volume is considered an half of volume of the top layer. Finally, the thermal resistance dues to convection effect is given by:

$$C_{TH,conv} = \frac{1}{h \times A} \tag{3.42}$$

Table 3.5 summarizes up the found thermal resistances and the capacitances. It is important to observe that thermal network represents only the upper part of the simplified model. Generally this is not the way to create the thermal network, but it is the

Step	**R_{TH} [K/W]**	**C_{TH} [J/K]**
1	6.06×10^{-5}	4.36×10^{-2}
2	4.04×10^{-1}	9.68×10^{-3}
3	5.00×10^{3}	-

Table 3.5: Cauer thermal network elements extracted from materials and geometries.

clearest way to introduce the extraction of the Foster thermal network. To the thermal network of Figure 3.22 is applied a power step of 0.1 W. The Z_{TH} extracted from the network of Figure 3.22 can be used to find the Foster thermal network through a simple fit procedure. The mathematical formulation is presented in (3.43), (3.44), (3.45) and (3.46).

$$\min \sum_{u=0}^{U} \sqrt{(Z_{THC}(t_u) - Z_{THF}(t_u))^2} \tag{3.43}$$

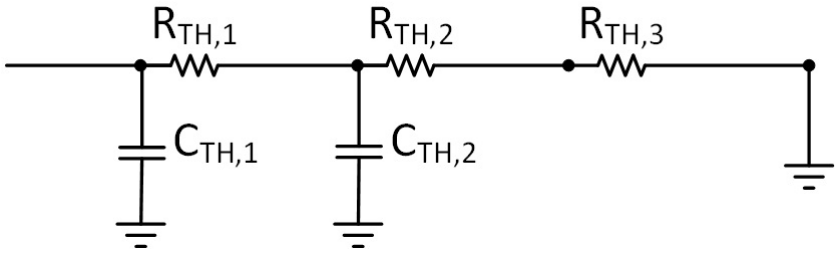

Figure 3.22: Cauer thermal network composed by elements of Table 3.5.

$$Z_{THF}(t_u) = \sum_{i=1}^{N} R_{TH,i}(1-\exp(-t_u/(R_{TH,i}C_{TH,i}))) \ \forall t_u | u = 1,...,U \tag{3.44}$$

$$R_{TH,i} > 0 \ \forall i = 1,...,N \wedge R_{TH,i} \in \mathscr{R} \tag{3.45}$$

$$C_{TH,i} > 0 \ \forall i = 1,...,N \wedge C_{TH,i} \in \mathscr{R} \tag{3.46}$$

where u is the timestep index, U is the number of timesteps, t_u is the timestep, i is the step index of the network ($R_{TH}C_{TH}$ couple), and N the number of steps.
The found Foster thermal network through the minimization problem is reported in Table 3.6 and Figure 3.23. Finally the Z_{TH} comparison between the two thermal

Step	**R_{TH} [K/W]**	**C_{TH} [J/K]**
1	2.48×10^{3}	1.08×10^{-1}
2	2.52×10^{-1}	1.05×10^{-1}
3	1.00×10^{-1}	2.00×10^{0}

Table 3.6: Foster thermal network elements extracted from Cauer thermal network.

networks is shown in Figure 3.24, showing an almost perfect superimposition in the whole frequency range.

3.4.5 Thermal modeling and reliability of power systems

Given the application field, power electronic devices are meant to work in severe use conditions during their whole lifetime. For this reason, the designing phase must

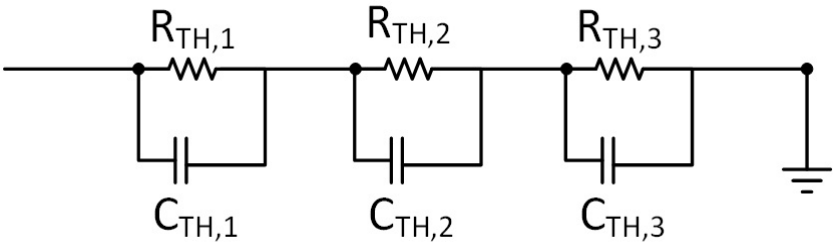

Figure 3.23: Foster thermal network composed by elements of Table 3.6.

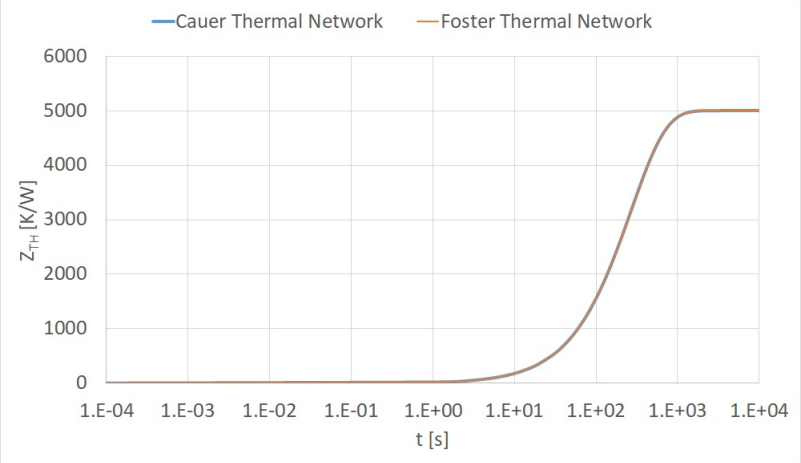

Figure 3.24: Comparison between Cauer and Foster network thermal impedances.

highly take into account electro-thermal mechanical aspects. Although during the last decades, power device studies has been focused on the comprehension of electro-thermal mechanical phenomena to improve devices reliability, it is still heavily complex to design such devices by following the guide of electro-thermal mechanical aspects. As a matter of fact, that it is well understood how the combination of electro-thermal-mechanical phenomena can have a negative impact on performance and reliability, but it is also true that, it reveals hard to predict the extent of impact during the designing phase. This is plausibly a consequence of the complexity in modeling these phenomena, and, consequently, in studying their effects on power devices through simulation [88][89].
Many techniques concerning modeling and simulation of the impact of these physical phenomena on power semiconductor devices behavior have been develop for a design guided by electro-thermal mechanical limitations (Figure 3.24).
Thermal modeling studies can be split into two main approaches:

- approches based on LEM in both Cauer and Foster methodologies;
- approaches based on FEM.

In Table 3.6 are listed the main works proposed in literature, in order to give a quite complete vision of the state of the art.

Approach based on	**References**
LEM	[86] [90] [91] [92] [93] [94] [95] [96] [87] [97] [98] [99] [100] [101] [102] [103] [104] [105] [106] [107] [108] [109] [110] [111] [112]
FEM	[113] [114] [115] [116] [117] [118] [119] [120] [121] [80] [6] [122] [123] [124]

Table 3.7: State of the art of thermal modeling.

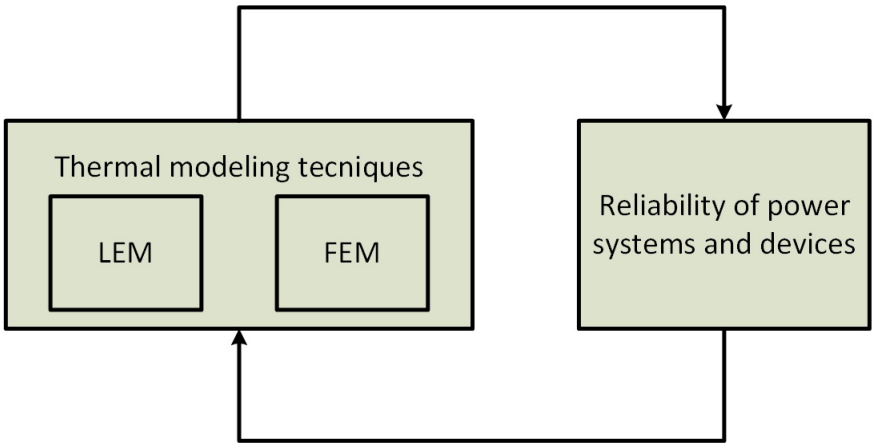

Figure 3.25: Relationship between thermal modeling and reliability.

Chapter 4

The 1-D FEM approach

You don't understand anything until
you learn it more than one way.

– Marvin Lee Minsky

This chapter presents a simple method to describe the effect of Printed Circuit Board (PCB) and environment on packaged devices thermal behavior. The approach aims at exploiting the benefit of Lumped Element (LE) compact thermal models, which are necessarily one-dimensional, together with the advantage of Finite Element (FE) modeling. FE thermal modeling allows to retain all the three-dimensional geometrical details only in the regions of the model that must be accurately described. The main focus is on correct modeling of thermal behavior in long power pulses conditions, in order to use it for subsequent electro-thermal and thermo-mechanical analysis at chip level [125].

4.1 Overview on the state of art

The main concern in automotive electronics is about producing high-level reliable devices. Strong thermal stress for such devices (e.g. in light bulbs or servo-motors), which can be due to high inrush current, long turn-off times and high inductances.

Generally, loads in automotive imply high switching losses, long turn-on and turn-off transients, and remarkable overheating in power devices. Such switchings, and consequent power cycles, that can occur up to million times, inevitably induce thermo-mechanical device degradation which may reasonably lead to electrical failure. This is why it is necessary to regulate such power cycles and to understand failure mechanisms by realizing an accurate thermal.
To capture the important thermal effects from the modeling point of view, it must be considered the relation between:

- the duration of the power dissipation pulse;
- and the necessary level of details.

Figure 4.1 [126] shows the schematic structure of a typical low voltage electronic switch. By considering a short pulses case (10 μs $\div$ 1 ms), the device should be modeled down to the die attach level. The effect of package and PCB on the overall thermal behavior should be neglected as the heat wave will not get to the latter domains.
By considering long pulses (where duration is <1 s), the internal structure of the device is reproduced in a simplified way, while maintaining the right modeling of pins, solder joints, and PCB. In this case, the situation will be reversed if compared to the previous one.
Anyway, one should keep in mind that, by simplification, some limits rise to the surface: this kind of modeling consider the device mechanically perfect and operating under a thermally stable condition, which is clearly not always true: one could just think about MOSFETs, which can operate under unstable regime below the Temperature Compensation Point (TCP) [123]. As hinted before, in the case of long pulses modeling, the PCB, as well as the packaged device itself, must necessarily be included in the electro-thermal model. This is considered as the real challenging engineering issue, as the same model has to feature detailed and general elements (such as tens-of–micrometer bonding wires, and centimeters-wide PCB).
Such issues can be solved through several different approaches [127] [128]: one for all, the method through which the PCB is simplified to reduce the simulation's De-

grees of Freedom (DoFs). The chapter will focus on the basics of the method and it will provide two case studies.

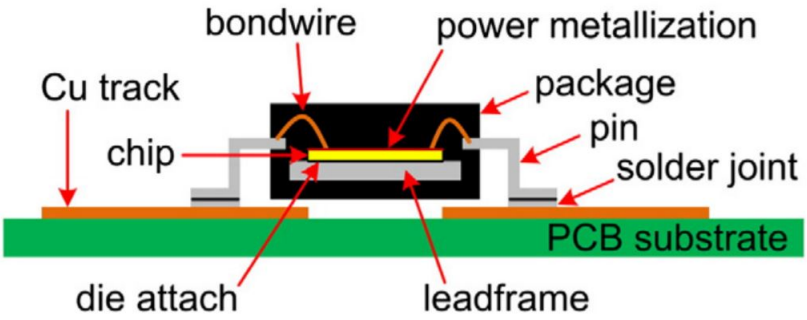

Figure 4.1: A schematic view of a packaged device mounted on PCB.

4.2 The approach

First of all, it is necessary to recall the concept of LEMs, well-known in literature, which describe a thermal system through $R_{TH}C_{TH}$ networks, where the heat flow path is modelled by thermal resistances and capacitances. They are based on the formal analogy between Fourier thermal equation and electrical circuit equations. Even if they can capture the heat flow in the structure, such physics-based models need the intervention of many other elements [94]; contrarily, the models based on Foster and Cauer networks, called empirical models [92], can be easily solved with the exception of multilayer stacks; in this case, the models don't have any physical link with the described structure. The simplified approach here suggested wants to relate the benefits of LEMs with the geometric description advantages given by FE models, by assuming that heat propagation could be modeled in a nearly 1-D way; the heat propagation taken into consideration here is that through the contact surfaces between PCB and pin, or solder joints; these last should correspond to a contact surface in Figure 4.2 [126]. Equation, by assuming 1D heat transfer, describes the thermal behavior at the contact surface. A given i-th contact surface will be run over

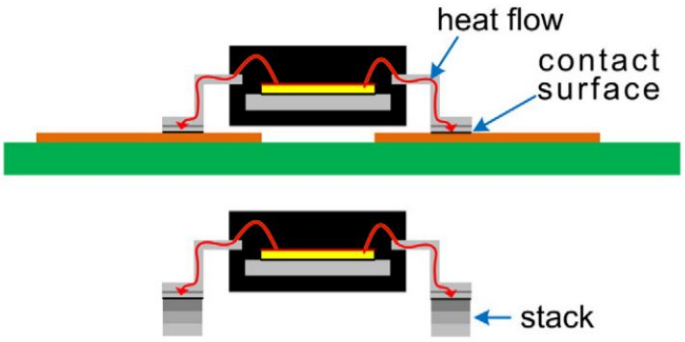

Figure 4.2: Cross-sectional view of heat path between the contact surfaces in the full model (top) and in a simplified one (bottom).

by a given heat flux $P_{S,i}$ in Watts, where $T_{S,i}$ will be the surface-averaged temperature of the contact surface itself in Kelvin. T_{AMB} reference temperature is the ambient one. The following is the calculation of the thermal impedance at the i-th contact surface $Z_{TH,i}$:

$$Z_{TH,i} = \frac{T_{S,i} - T_{AMB}}{P_{S,i}} \tag{4.1}$$

The approach requires to build a Cauer LE model fitting the above-described thermal impedance response at the contact surface. The obtained LE model ($R_{TH,m}$ - $C_{TH,m}$ values for Cauer representation set) has to be transformed into its geometrically equivalent FE model. An adiabatic-lateral-walls fictitious layer of a stack in the FE model will be created, and this will be done for each RC stage. For both LE and FE models, the same 1D thermal impedance response must be ensured; for this purpose, the properties of the material are determined (see Figure 4.3 [126]). Being A_i a contact surface, it is possible to calculate the thermal impedance at its location in order to obtain the Cauer network. When m stages are detected (if considering Figure 4.3, $M = 3$), a stack of M materials (m_1, m_2, ..., m_n) can be generated in the FE model. The bottom of such a stack must be set at $T = T_{AMB}$ and it includes the consequences of the boundary conditions fixed around the PCB in the original model. The contact surface fixes the cross-sectional area on the xy plane and the thickness of each

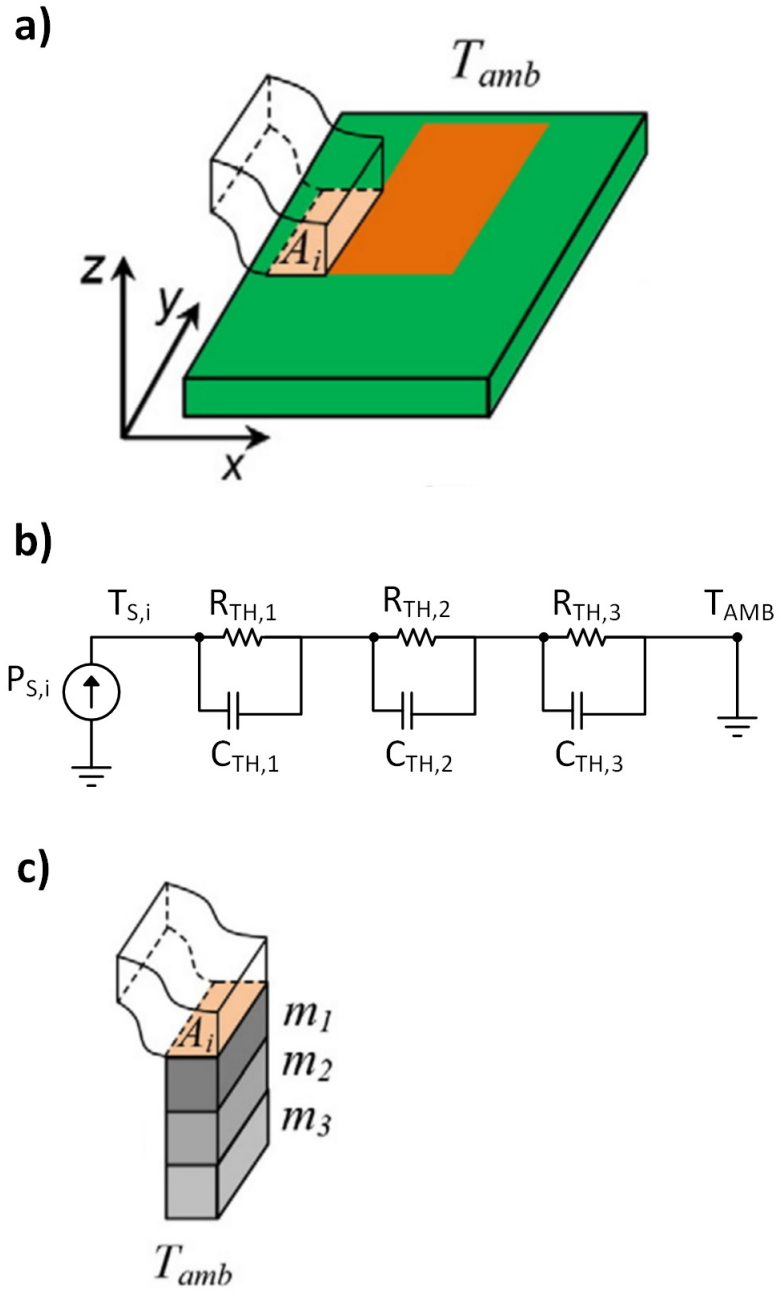

Figure 4.3: Graphical overview in order to obtaine the simplified FE model; a) A_i identification; b) Cauer network evaluation; c) PCB replacement by stack.

layer is influenced by mesh constrains, which proves to be eased when contiguous volumes show proportionate thickness. These observations are clearly represented by Figure 4.3.
Obviously, the above-discussed model cannot be considered as a Boundary Condition Independent (BCI) model [129] [130]. If the boundary conditions of the model change, it is necessary to redo the simplification process.

4.2.1 Determination of Cauer network

It is necessary to determine the Cauer network to obtain a simplified FE model featuring equivalent loads replacing the PCB under pins. The reference model here to be used is a D2PAK MOSFET mounted/placed on a PCB with a standard FR4 substrate (1.6 mm thickness, 1 oz copper). Such reference model explains the procedure for one contact surface.
The Cauer network should be determined for each contact surface (be it gate, drain or source): a stepped wave form heat-flux will be applied at each A_i, while all the other contacts will be kept thermally insulated. First of all, the corresponding Foster networks for each contact surface must be identified:

$$Z_{TH,i}(t) = \frac{T_{S,i}(t) - T_{AMB}}{P_{S,i} \cdot u(t)} \tag{4.2}$$

The equation shows the unit step function $u(t)$, the width of the stepped heat flux P as in $P = P_{S,i}u(t)$. Anyway, the simplified model does not take into consideration the reciprocal thermal influence between each A_i; for this reason, results cannot be considered satisfactory.
The consequent second approach was to apply a stepped waveform heat-flux to each contact surface simultaneously. This second attempt brought to non-satisfactory results as well, as different copper track dimensions, different area sections, and other peculiarities, generally generate different mutual influence between each A_i. As none of the above methods gives valuable results, the calculation of the Cauer network, derived from the Foster form, has to go through the consideration of:

1. the magnitudes and delays paths between the chip and the contact surfaces;

2. the $P_{S,i}(t)$ interactions in the PCB.

For the above two reasons the stepped heat source should be applied in the full model chip. By processing the simulation results, $T_{S,i}(t)$ and $P_{S,i}(t)$, which are necessary to define $Z_{TH,i}$ at each A_i, can be calculated.
In this approach, $P_{S,i}(t)$ presents a waveform smoothed by its flux from the chip through the system and, for this reason, it is not a power step; while $Z_{TH,i}(t)$ is in its Foster form:

$$Z_{TH,i}(t) = \sum_{m=1}^{M} (1 - \exp(-t/(R_{TH,m}C_{TH,m}))) \tag{4.3}$$

The next step would be to fix the M time constant values $\tau_m = R_{TH,m}C_{TH,m}$. The parameters here used were modified by employing both $R_{TH,m}$ and $C_{TH,m}$, and the maximum M of stages was fixed. For this reason, the following function has to be minimized:

$$f_{obj}(t) = \sum_{t=t_{START}}^{t_{END}} (Z_{TH,i}(t) - Z_{THF,i}(t))^2 \tag{4.4}$$

The minimization shown by (4.4) considers both $R_{TH,m}$ and $C_{TH,m}$ parameters as they are featured on the full time response of the system. The result is that couples $(R_{TH,m}, C_{TH,m})$ featuring the same time constant τ_m have to be reduced to a single equivalent Foster stage. The conversion to Cauer network takes place on the bases of [87]. By hoping for tolerable numbers of errors between the simplified model and the original one, an arbitrary number of stages N is fixed to perform the algorithm; anyway, the least squares estimator cannot guarantee it, as it is also true for other estimators. Since a single simple equivalent model is the goal of this approach, only 5 stages are needed in view of many more useless stages. Figure 4.4 is a clear example of temperature behavior in the center of the chip's mass and its error between the original and the simplified models.
(4.5) shows the error in a specific moment and at a specific point:

$$ERR(t)\% = \frac{\Delta_{OM}(t) - \Delta_{SM}(t)}{\Delta_{OM}} \tag{4.5}$$

$\Delta_{OM}(t)$ is the original model temperature increase at a given time; $\Delta_{SM}(t)$ is the simplified model temperature increase in the same moment; and Δ_{OM} represents the original model temperature increase in stationary conditions. As Figure 4.4 [126] shows,

the error during the heating phase is greater than 5% in a specific point, $M = 5$.
Such an error cannot be accepted by a coupled electro-thermal simulation of long pulses as the overall error would be greater.

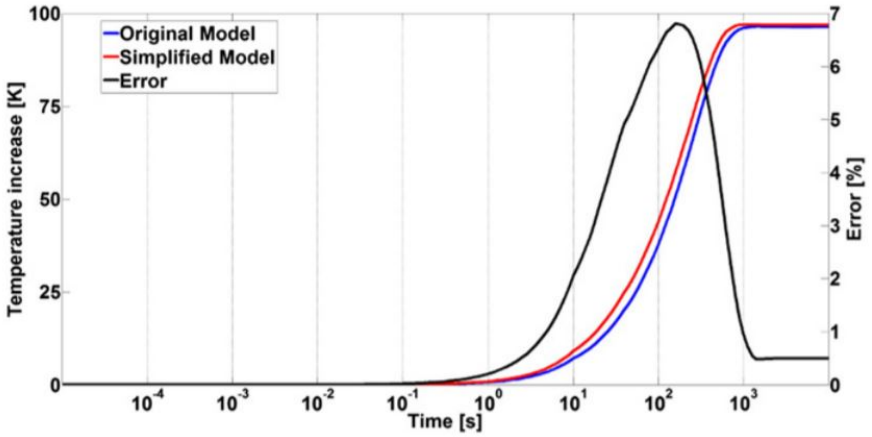

Figure 4.4: D2PAK mounted on a PCB: comparison between temperatures of the chip's mass center as a function of time. Obtained from the full original model and the simplified model built applying the $Z_{TH,i}(t)$ fit routine with $R_{TH,m}$ and $C_{TH,m}$ as fitting parameters, limiting M to 5.

4.2.2 Enhancement of the simplified model

The goal of the procedure is to reduce the error to a tolerable level through a fine-tuning phase. As seen in Figure 4.4, the two curves shift in time: the original model curve differs in breadth and positioning from the simplified one, so that this last should be modified in width and considered at a steady state. The heat spreading in the copper tracks is accounted by another $R_{TH}C_{TH}$, which is used for fine-tuning aims. Fig. 5 shows the final *RC* network.
Figure 4.3 represents the copper tracks horizontal spreading in x and y directions, while FR4 and PCB spreading flux are irrelevant due to their minimal thermal properties. Two thermal impedances have been taken as references to model the heat trans-

fer from a contact surface to the ambient: the average temperature at the bottom of a pin has been defined as T_a, while the average temperature at the top of the copper track has been defined as T_b. As the Cu track usually dissipates heat, then $T_a > T_b$. The network topology is shown in Figure 4.5, while the pin is clearly represented as disconnected from its copper track in Figure 4.6 [126]. The time dependent thermal

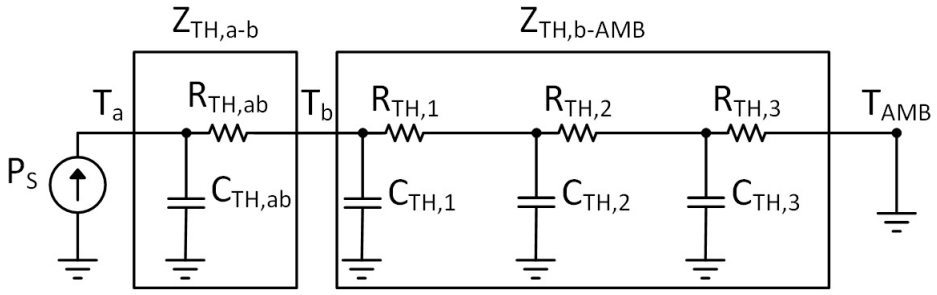

Figure 4.5: Equivalent Cauer thermal network including with the terms $R_{TH,ab}$, $C_{TH,ab}$ Figure 4.3 .

impedance between the Cu track and ambient, $Z_{TH,b-AMB}(t)$, will be calculated:

$$Z_{TH,b-AMB}(t) = \frac{T_b(t) - T_{AMB}}{P_S(t)} \tag{4.6}$$

Even if, formally speaking, (4.6) can be considered as valid only when $P_S(t)$ is a step function, this will be taken into account as a good approximation leading to a Foster model; the consequent stages are defined by:

$$Z_{THF,b-AMB}(t) = \sum_{m=1}^{M} R_{TH,m}(1 - \exp(-t/(R_{TH,m}C_{TH,m}))) \tag{4.7}$$

Now the maximum number M of stages should be set, so that the following objective function would be minimized, as specified in the previous subsection:

$$f_{obj}(t) = \sum_{t=t_{START}}^{t_{END}} (Z_{TH,b-AMB}(t) - Z_{THF,b-AMB}(t))^2 \tag{4.8}$$

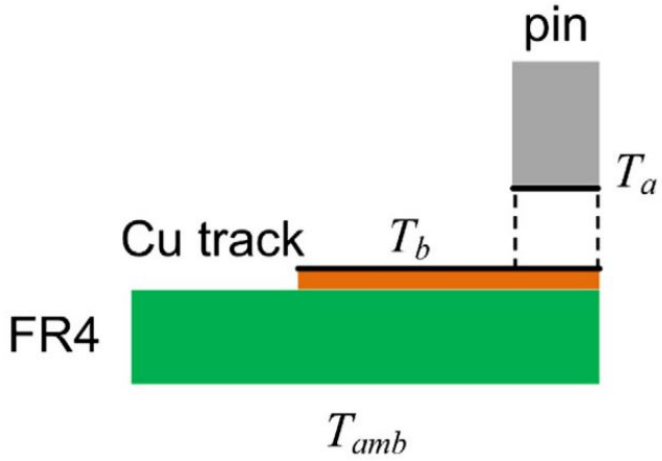

Figure 4.6: Intermediate temperature points at a contact surface; pin is disconnected from its Cu track for sake of clarity.

$2 \div 4$ stages supplied acceptable results. The last phase is the identification of $R_{TH,ab}$ and $C_{TH,ab}$ terms. In particular, $R_{TH,ab}$ is obtained as follows:

$$R_{TH,ab} = \frac{T_a - T_b}{P_S} \tag{4.9}$$

To obtain $C_{TH,ab}$ in a repetitive way, it will be crucial to apply a Perturb & Observe (P&O) technique algorithm: by influencing the time shift value τ_{ab}, it minimizes the difference between the original model and the simplified one. To guarantee the P&O algorithm association, an initial guess τ_{ab0} for an unknown time constant τ_{ab} is set. An example of valid guess is: $\tau_{ab0} = C_{TH,ab0} R_{TH,ab0}$ ($C_{TH,ab0}$ is the thermal capacitance obtained considering the volume of the copper outside the contact surface A_i). Once the Cauer network is obtained, the transformation phase to the stack of equivalent materials goes as follows: each layer's thickness H must be fixed, and its thermal conductivity λ and heat capacity C_p for every M layer of each contact surface are calculated by:

$$\lambda_{mi} = \frac{H_{mi}}{R_{TH,mi} \times A_i} \tag{4.10}$$

$$C_{p,mi} = \frac{C_{TH,mi}}{H_{mi} \times A_i \times \rho_{mi}} \tag{4.11}$$

4.3 The algorithm in detail

This section is provided in order to facilitate the development of an automatic computer procedure. The approach i based on a process made up by 8 steps summarized in Figure 4.7 and better explained in the following.

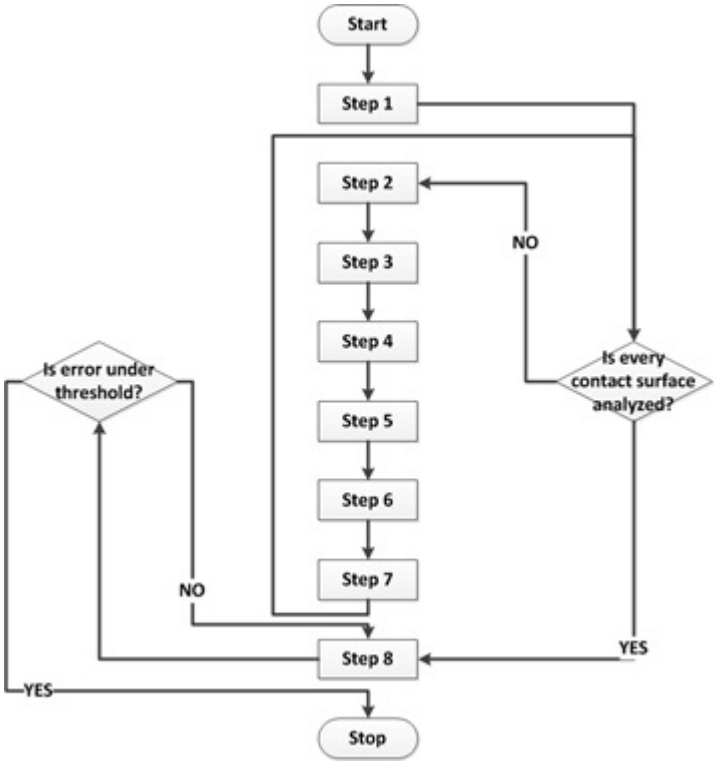

Figure 4.7: Necessary process to create a 1-D FEM model

4.3.1 Step 1

Original model FEM simulation is realized by keeping in mind that temperatures and heat fluxes going through contact surfaces must be known to use them, at a later stage, to calculate thermal resistances and capacitances of the fictitious materials constituting the stacks placed under the compact model contact surfaces. While considering temperatures, one should always relate to average temperature. Figure 4.8 shows an example of a pin in contact with a PCB, where surfaces involved in the measurement of quantities are specified. The following six steps supporting this methodology must

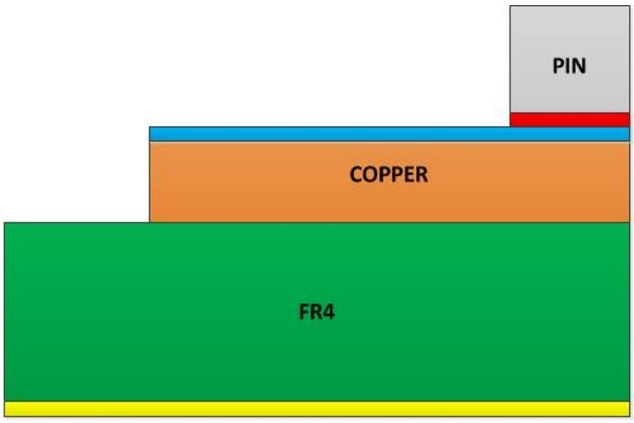

Figure 4.8: Example showing the proposed process, specifically, by schematizing the PCB structure composed of a pin (being part of a device), a copper layer, and an FR-4 layer.

be accomplished for each contact surface. In the case of a MOSFET in D2PAK package, such an activity must be performed three times. In Figure 4.8 (section of a pin), three surfaces can be identified:

- under the pin;
- above the copper layer;
- under the entire board.

Concerning quantities to be measured, it is possible to refer to Table 4.1.

Surface	Temperature [K]	Heat flux [W]
Under the pin	Yes	Yes
Above the copper layer	Yes	No
Under the entire board	Yes	No

Table 4.1: Necessary observation temperature points and heta fluxes, in order to obtain a simplified model.

4.3.2 Step 2

The calculation of contact resistance allows to relate surfaces with different dimensions. In general average temperatures on the two surfaces are different (see red and blue stripes of Figure 4.8), except in case when both surfaces feature the same geometrical area. Then, it is firstly necessary to calculate the thermal resistance between the two faces using (4.9) in steady state condition. The calculated resistance will be used for the first layer of fictitious material to be placed under the contact surface, while its thermal capacity will be calculated at a later stage. Figure 4.9 explains the function of this step in $R_{TH}C_{TH}$ notation, where $Z_{TH,B-AMB}$ is still unknown, as well as $C_{TH,ab}$.

4.3.3 Step 3

Thermal impedance calculation must be performed for each contact surface between the part of the model that will remain unchanged and the part of the model that will be simplified. With reference to Figure 4.9, it will be necessary to calculate the thermal impedance between T_b (average temperature of point surface) and T_{AMB} by taking into consideration the heat flux through the contact surface. So, the result will be an impedance for each contact surface (4.6).

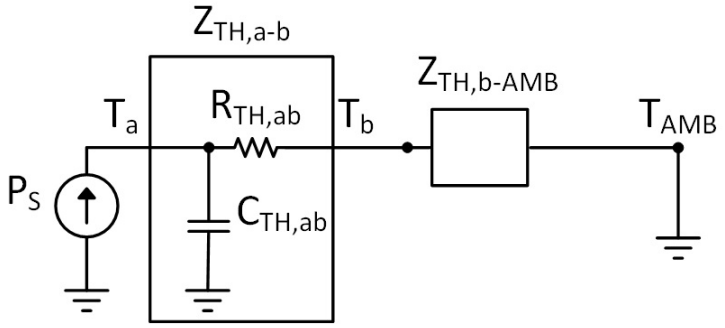

Figure 4.9: $R_{TH}C_{TH}$ notation of expressions shown in step 2. $R_{TH}C_{TH}$ network is developed for every contact surface.

4.3.4 Step 4

Calculation of $R_{TH}C_{TH}$ couples, that can generate the same impedance as calculated in the previous step, occurs through the resolution of a non-linear programming problem. For this purpose (4.8) need to be minimized simirlarly to (4.12):

$$\min \sum_{t=t_{START}}^{t_{END}} (Z_{TH,b-AMB}(t) - Z_{THF,b-AMB}(t))^2 \tag{4.12}$$

The representation is a mixed representation between Cauer and Foster notation as illustrated in Figure 4.10.

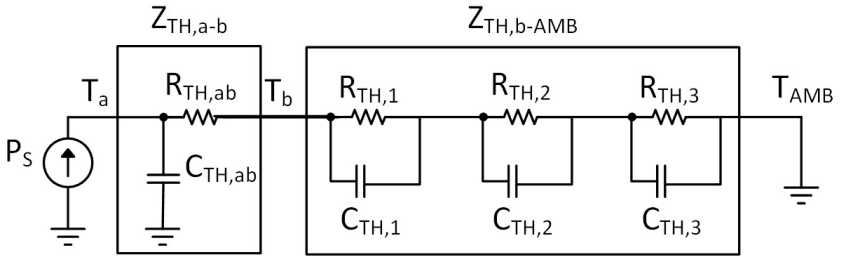

Figure 4.10: $R_{TH}C_{TH}$ intermediary representation.

4.3.5 Step 5

Transformation from Foster to Cauer representation by following the method provided by [87]. The result obtained is the same of Figure 4.5. The thermal capacitance $C_{TH,ab}$ is already unknown.

4.3.6 Step 6

Once obtained couples $R_{TH,m}C_{TH,m}$ of Cauer representation, values λ, C_p and ρ must be determined and assigned to the materials of the fictitious materials stacks. H (material thickness), A (material contact surface) and ρ will be fixed conventionally. It has to be kept in mind that $C_{TH,ab}$ is still unknown and that it will be calculated through an iterative method. For this purpose, $C_{TH,ab0}$ will be chosen through the assumption that $C_{TH,ab}$ must have a value related to that of the material directly underlying the pin as in Figure 4.8. This will actually be the starting value for the calculation of $C_{TH,ab}$.

4.3.7 Step 7

A new model for FEM simulation is, therefore, built by placing a stack of fictitious materials under each contact surface. Each material will be defined by a couple λ and C_p and by constant ρ. It will be assigned to blocks featuring H height and A surface.

4.3.8 Step 8

This last step allows to obtain the value of every $C_{TH,ab}$, starting from $C_{TH,ab0}$. The algorithm shown in Algorithm 4.1, Algorithm 4.2 and Algorithm 4.3 is simplistically referred to a single contact surface and must be applied simultaneously to all the contact surfaces. In his way, compact model FEM simulation must be compared to original model FEM simulation until the desired accuracy is achieved. This binary search algorithm is supported by P&O methodology intuition.

Algorithm 4.1 $C_{TH,ab}$ search algorithm part I

```
Cab0=initial_value();
Cab=Cab0;
Tab0=Rab*Cab0;
Error=0;
D_Error=defined_accettable_error();
Indexj=1;
Dif=MAX_REAL;
for(j=1;j<Number_t;j++)
{
   If(abs(t[j]-Tab0)<Dif)
   {
      Tab0=t[j];
      Indexj=j;
      Cab0=Tab0/Rab;
      Cab=Cab0;
      Error=Error_FEM_Compact_Model(Rab,Cab);
   }
}
```

Algorithm 4.2 $C_{TH,ab}$ search algorithm part II

```
If(Error>D_error)
{
   Tab0=t[indexj-1];
   Cab0=Tab0/Rab;
   If(Error_FEM_Compact_Model(Rab,Cab0)<Error)
   {
      Error= Error_FEM_Compact_Model(Rab,Cab0);
      Cab=Cab0;
      For(j=indexj-1;j>=0;j--)
      {
         Tab0=t[j];
         Cab0=Tab0/Rab;
         If(Error_FEM_Compact_Model(Rab,Cab0)<Error)
         {
            Error= Error_FEM_Compact_Model(Rab,Cab0);
            Cab=Cab0;
         }
      }
   }
```

Algorithm 4.3 $C_{TH,ab}$ search algorithm part III

```
   Else
   {
      If(indexj+1<Number_t)
      {
         Tab0=t[indexj+1];
         Cab0=Tab0/Rab;
         If(Error_FEM_Compact_Model(Rab,Cab0)<Error)
         {
            Error= Error_FEM_Compact_Model(Rab,Cab0);
            Cab=Cab0;
            For(j=indexj+1;j<Number_t;j++)
            {
               Tab0=t[j];
               Cab0=Tab0/Rab;
               If(Error_FEM_Compact_Model(Rab,Cab0)<Error)
               {
                  Error=Error_FEM_Compact_Model(Rab,Cab0)
                  Cab=Cab0;
               }
            }
         }
      }
   }
}
```

4.3.9 Software design and development

The entire process described between step 1 and step 6 of the previous subsections is supported by a MATLAB application. The last two steps need to be implemented through ad-hoc code inside the simulation. In the case of COMSOL Multiphysics, it is useful to write a script in Java language in the model Java code.
Compact Thermal Tool Ver. 2.1 provides a Graphical User Interface (GUI) to the main tasks about the methodology (steps from 1 to 6). Here are presented the main elements about the design (Figure 4.11 and Figure 4.12) and developed (Figure 4.13) of the MATLAB software Compact Thermal Tool Ver. 2.1, in order to provide a structured guide for future enhancement.

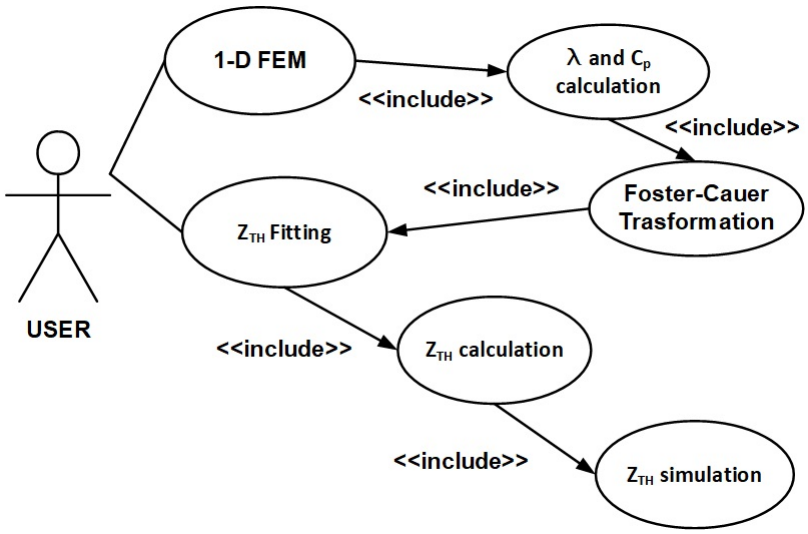

Figure 4.11: UML use case diagram of Compact Thermal Tool Ver. 2.1.

4.4 Validation of the approach

Two application cases of the suggested approach will be presented in this section. The aim is to study different topologies, and for this reason, a D2PAK and a SO-8

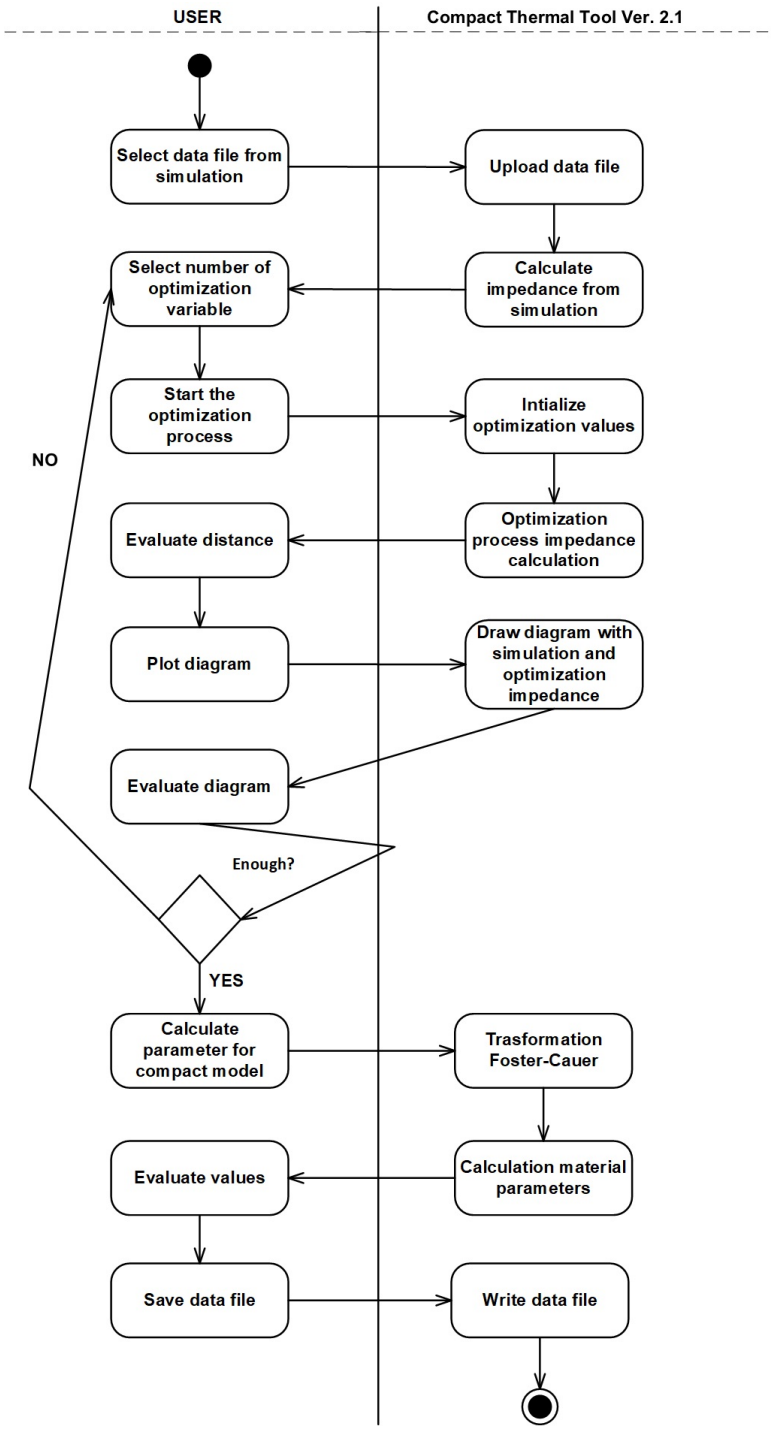

Figure 4.12: UML activity diagram of Compact Thermal Tool Ver. 2.1.

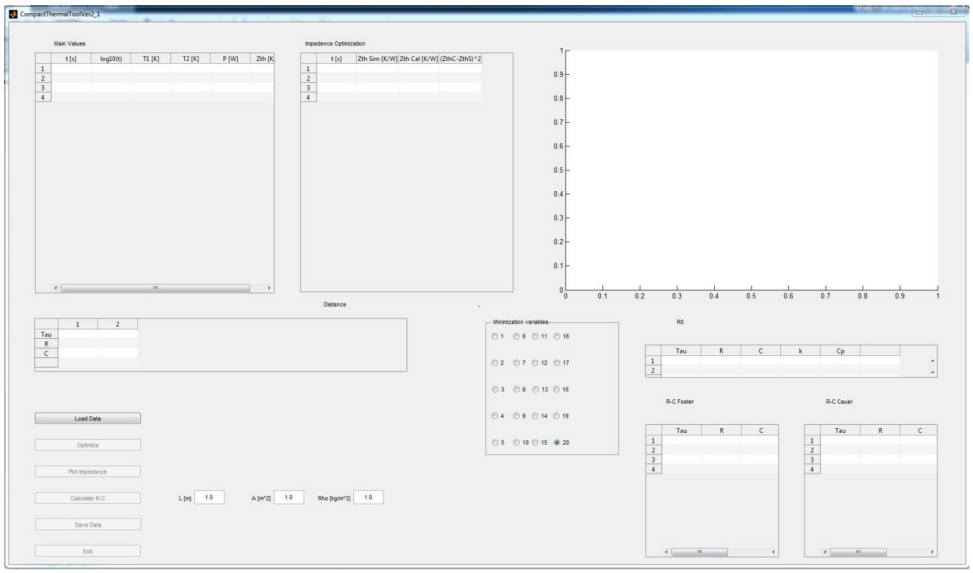

Figure 4.13: GUI of Compact Thermal Tool Ver. 2.1.

packaged devices are chosen. Two sets of boundary conditions are the bases for the devices simulations:

1. lower surface (opposite to the device) put to a fixed temperature (293 K), while other boundaries set as adiabatic;

2. boundaries set under constant convective heat flux with coefficient h equal to 10 $\mathrm{W}/(\mathrm{m}^2\mathrm{K})$.

Four original models and four simplified models are used to prove the effectiveness of this method (see Table 4.2). The resulting indication code will be essential for the next phases. The D2PAK model has already been validated against measurements, but with different boundary conditions [114].

4.4.1 D2PAK device package

The D2PAK packaged device is the focus of the first two simulation cases. Figure 4.14.a [126] shows the original 3D FE models structure of the D2PAK on a PCB;

Package	Boundary Conditions Setup	Original model mnemonic code	Simplified model mnemonic code
D2PAK	1	D2PAK_F_O	D2PAK_F_S
D2PAK	2	D2PAK_H_O	D2PAK_H_S
SO-8	1	SO8_F_O	SO8_F_S
SO-8	2	SO8_H_O	SO8_H_S

Table 4.2: Mnemonic coding for FEM models.

both boundaries setup are considered as simulation cases. The simplified models are this way generated: Figure 4.14.b [126] shows their boundary conditions, while Figure 4.14.c [126] marks some details of the device. Figure 4.15 [126] shows the comparison between D2PAK_F_O and D2PAK_F_S. Finally Figure 4.16 [126] highlights the obtained stacks for boundaries setup 1 and 2 which require, respectively, 4 and 3 layers.

Table 4.3 and Table 4.4 list the obtained $R_{TH}C_{TH}$ stages of the Cauer networks for D2PAK_F_S and D2PAK_H_S. Even if the number of layers required to generate simplified models is arbitrary, this number should be as lower as possible, so that the corresponding number of DoFs will be small. Anyway, the number of layers cannot be smaller than three, two for $Z_{TH,b-AMB}$ and one for $Z_{TH,ab}$.

Contact Area	R_{TH}/C_{TH}	Layer 0	Layer 1	Layer 2	Layer 3
D2PAK_F_S-A1	R_{TH}	8.45	23.47	40.71	4.58
D2PAK_F_S-A1	C_{TH}	0.024	0.039	0.089	2.97
D2PAK_F_S-A2	R_{TH}	29.25	4.23	8.76	0.73
D2PAK_F_S-A2	C_{TH}	0.015	0.22	0.43	20.29
D2PAK_F_S-A3	R_{TH}	1.83	2.44	5.21	0.58
D2PAK_F_S-A3	C_{TH}	0.0036	0.18	0.40	19.07

Table 4.3: D2PAK simplified model D2PAK_F_S thermal resistances [K/W] and capacitances [J/K] in Cauer representation. A1 is the gate, A2 is the source while A3 the drain.

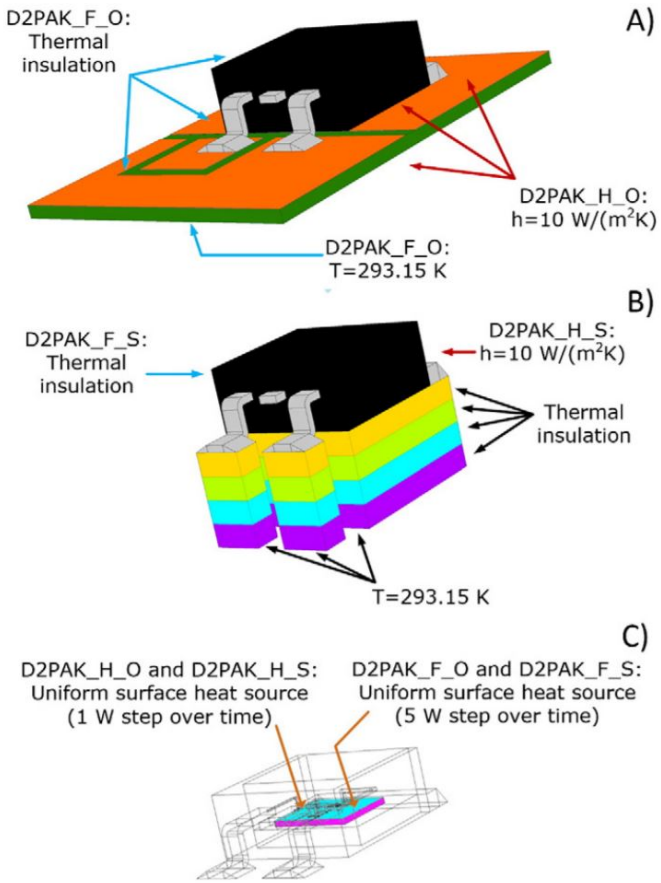

Figure 4.14: 3D FE models with the D2PAK packaged device: a) original model; b) simplified model; c) D2PAK details.

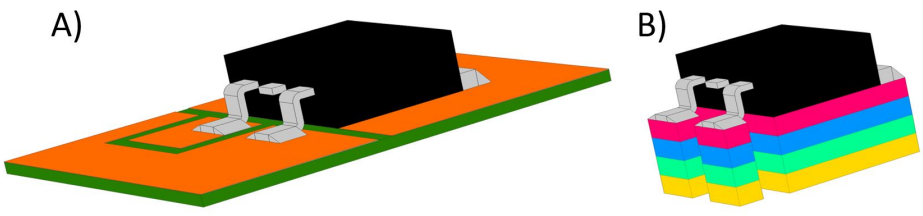

Figure 4.15: Comparison between a) D2PAK_F_O and b) D2PAK_F_S.

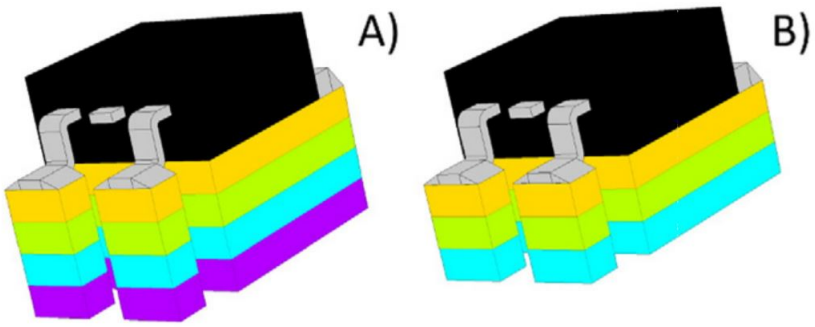

Figure 4.16: Comparison between a) D2PAK_F_S b) and D2PAK_H_S.

Contact Area	$\mathbf{R_{TH}/C_{TH}}$	**Layer 0**	**Layer 1**	**Layer 2**
D2PAK_H_S-A1	R_{TH}	11.85	507.9	448.6
D2PAK_H_S-A1	C_{TH}	0.017	0.11	0.25
D2PAK_H_S-A2	R_{TH}	42.46	270.1	57.23
D2PAK_H_S-A2	C_{TH}	0.033	0.52	1.21
D2PAK_H_S-A3	R_{TH}	2.44	82.25	81.2
D2PAK_H_S-A3	C_{TH}	0.58	0.65	1.52

Table 4.4: D2PAK simplified model D2PAK_H_S thermal resistances [K/W] and capacitances [J/K] in Cauer representation. A1 is the gate, A2 is the source while A3 the drain.

In the two simulation cases (D2PAK_F_S and D2PAK_H_S), the DoFs have been respectively reduced by 53% and 54% (if it is considered only the PCB, the reduction of DoFs are 88% and 90%). This reduction is generated in relation to the shape of the copper tracks and to the dimensions of the PCB (the larger the PCB, the higher the PCB reduction).
The temperature behavior taken into consideration is that of different points in the silicon chip. This consideration permitted to validate the method. In this case, the fine-tuning procedure explained above, reduces the error between the original and the simplified model.

Through the observation of the evolution over time of the temperature increase in the middle point of the top surface of the chip, in Figure 4.17 [126] and Figure 4.18 [126], it can be noted the error in the two simulation cases with fixed temperature at the lower surface of the PCB and convective heat flux around the structure. Concerning errors located away from the contact surfaces (as on the top of the package), this aspect has been additionally considered.

Even the temperature distribution at the time of maximum error in the center of

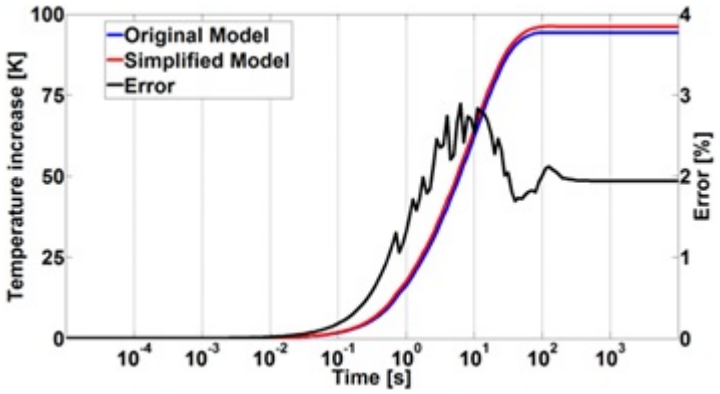

Figure 4.17: Temperature increase in the middle point of the chip for D2PAK_F_O and D2PAK_F_S. Maximum error is almost 3% at t = 8 s.

the chip's top surface has been taken into consideration in both cases. The temperature distribution simulated in a section of the structure on the chip top surface in D2PAK_F_S and D2PAK_F_O is represented by Figure 4.19.a [126] and Figure 4.19.b [126]; Figure 4.20.a [126] and Figure 4.20.b [126] show the whole structure temperature evolution in both D2PAK_F_S and D2PAK_F_O cases simultaneously.

In a similar way, a section of D2PAK_H_O and D2PAK_H_S simulations is showed by Figure 4.21.a [126] and Figure 4.21.b [126], while the entire structure is showed by Figure 4.22.a [126] and Figure 4.22.b [126]. The error found was of 3%, below the limit of 5% fixed at the beginning of the process.

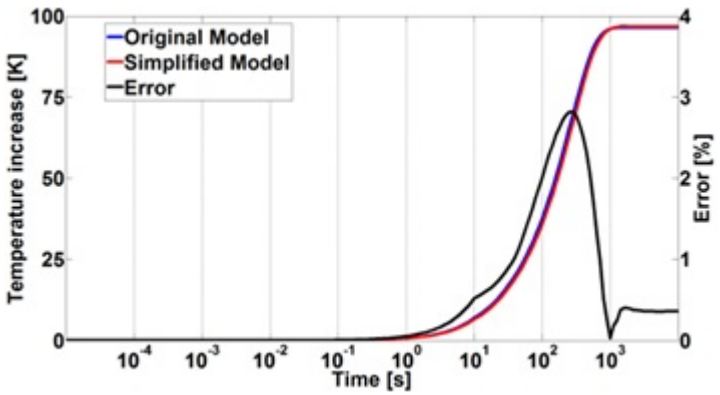

Figure 4.18: Temperature increase in the middle point of the chip for D2PAK_H_O and D2PAK_H_S. Maximum error is almost 3% at t = 251 s.

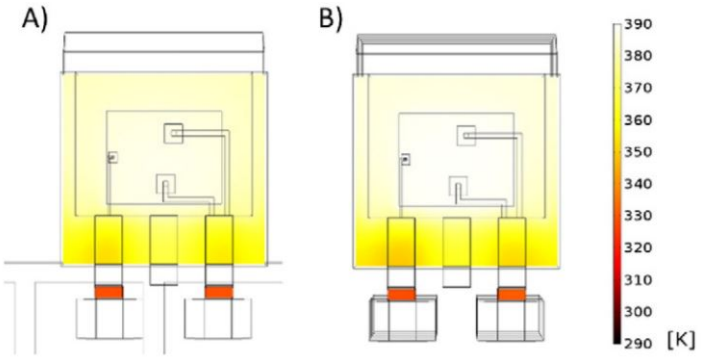

Figure 4.19: Temperature distribution at the time of maximum error in a slice (top surface of the chip) of simulation cases a) D2PAK_F_O and b) D2PAK_F_S.

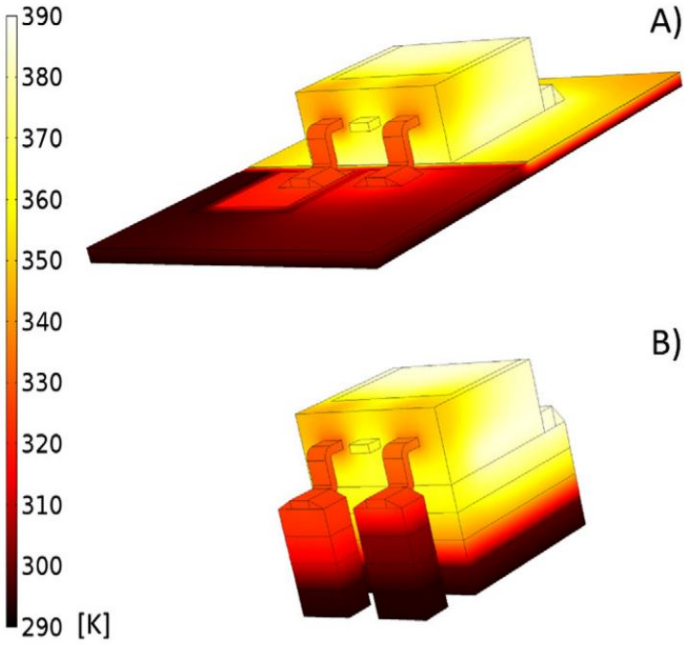

Figure 4.20: Temperature distribution at the time of maximum error in a 3D plot of simulation cases a) D2PAK_F_O and b) D2PAK_F_S.

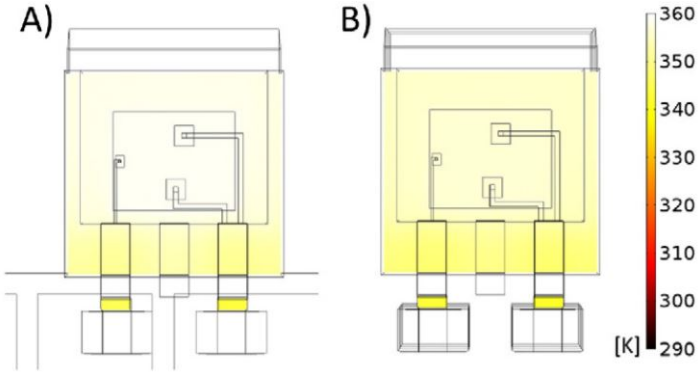

Figure 4.21: Temperature distribution at the time of maximum error in a slice (top surface of the chip) of simulation cases a) D2PAK_H_O and b) D2PAK_H_S.

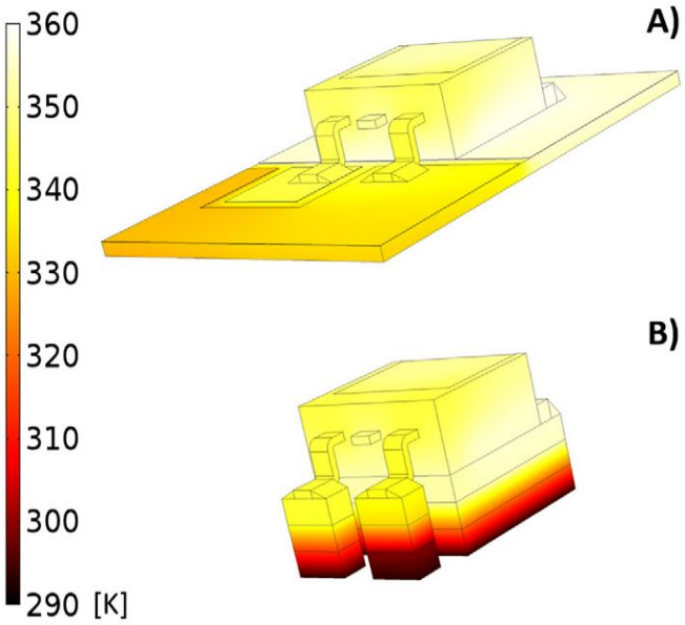

Figure 4.22: Temperature distribution at the time of maximum error in a 3D plot of simulation cases a) D2PAK_H_O and b) D2PAK_H_S.

4.4.2 SO-8 packaged device

An SO-8 bondless device is the second case study taken into consideration. Such a device presents more pins than a D2PAK, some of which share the same copper track, thus increasing the complexity of the simulation. The original and the simplified models used in the four simulations are represented by Figure 4.23 [126]. As

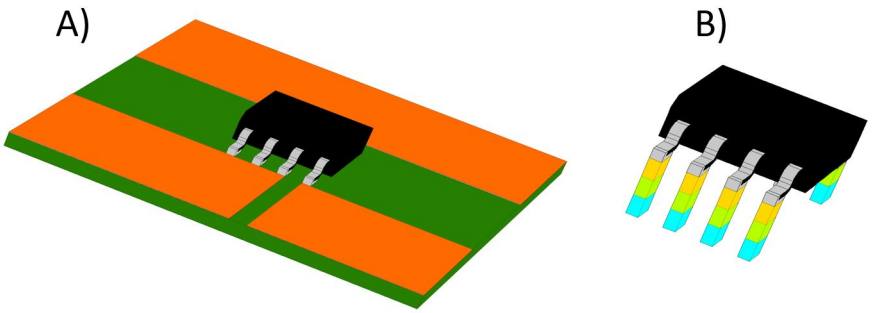

Figure 4.23: SO-8 device packaged, a) original models SO8_F_O, SO8_H_O and b) simplified models SO8_F_S and SO8_H_S.

Figure 4.19.b highlighted, for this particular/specific case, it was necessary to consider three layers in each stack. Since SO-8 features thin pins, it requires a fine mesh, which cannot be further coarsened, this model does not entail a high DoFs reduction: only 13% of reduction occurred (91% of which refers to the only PCB).
Figure 4.24 [126] (SO8_F) and Figure 4.25 [126] (SO8_H) show the results of the simulation cases simplified models: the maximum error detected is less than 2% and 4% at t = 9 s and t = 89 s, respectively.

4.5 Results discussion

This chapter introduced a method to determine 1D simplified models, in order to consider the effects of PCB and environmental conditions on a generic power device, and to implement them through a FE solver. It also highlighted the effects of heat spreading related to the copper tracks. It proved necessary to consider these effects

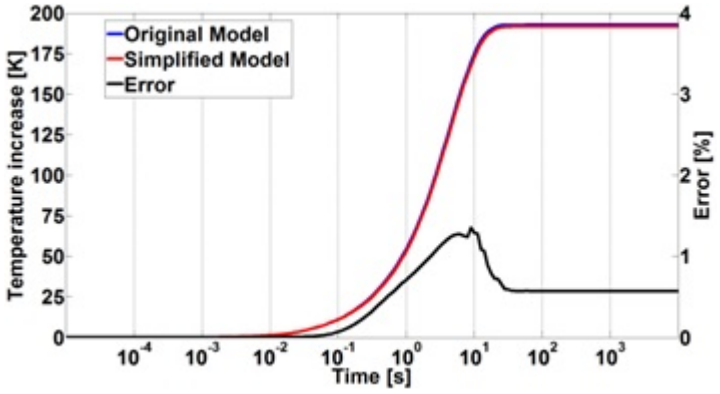

Figure 4.24: Temperature increase in the middle point of the chip for SO8_F_O and SO8_F_S. Maximum error is 2% at t = 9 s.

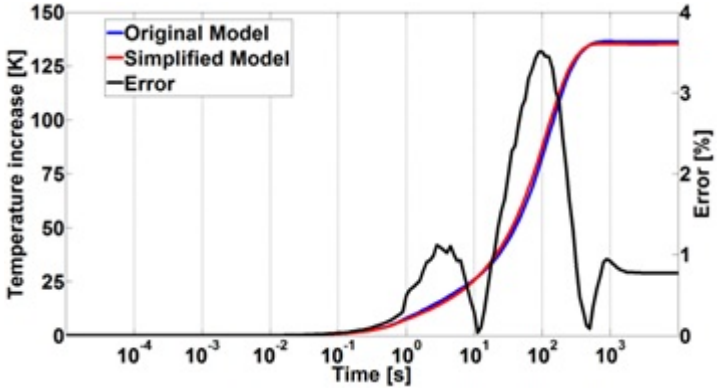

Figure 4.25: Temperature increase in the middle point of the chip for SO8_H_O and SO8_H_S. Maximum error is 4% at t = 89 s.

for the quality of modeling results.
The suggested approach has been applied to two simulated structures, thus reaching a strong reduction of the PCB modeling complexity.
What has been demonstrated is that it is possible to keep the geometrical details of a package device featuring long pulses just by substituting the complex model of the PCB with a simple material load. This method could be applied to the analysis of the chip as well, as to study the effects of small defects on the chip thermal performances.
Summing up the result, the errors are low with a great DoFs reduction (Table 4.5).

Simplified model	**Maximum error %**	**DoFs reduction (only PCB)**
D2PAK_F_S	3% at t=8 sec.	53% (88%)
D2PAK_H_S	3% at t=251 sec.	54%(90%)
SO8_F_S	2% at t=9 sec.	13% (91%)
SO8_H_S	4% at t=89 sec.	13% (91%)

Table 4.5: Comparison between maximum error and DoFs reduction in all four simulation cases.

Chapter 5

Non-linear multi-source LEM

This project is experimental
and of course comes without any warranty whatsoever.

– Tim Berners-Lee

The aim of this chapter is to present and validate a solid methodology to extract compact and accurate non-linear transient thermal models of thermal systems with multiple heat sources. Through the use of Infra-Red thermography measurements, the focus will be set on the analysis of a real example of such a system's thermal behavior, where a transient non-linear FEM-based model will be built and tuned on the measured thermal responses calculated in the locations of interest. These transient responses generate non-linear compact transient thermal models which are based on Foster network topology and can catch the effect of thermal non-linearities typical of any real thermal system deriving from the mutual interaction between different power sources. The description of the methodology will be followed by the validation of the model against measurements and by the discussion of the limitations of the process. This approach will demonstrate how it is possible to report non-linear effects in multiple-heat source systems with high accuracy, allowing more accurate but fast SPICE thermal simulations.

5.1 Overview

Methods on the determination of thermal compact models describing the propagation of heat under particular boundary conditions in certain systems by means of *RC* thermal components are well-known topics in literature. This kind of methods are widely used in applications (reliability, design, etc.) thanks to their computational lightness and their capacity to couple with electro-thermal electron devices models. If considering these methods from an pragmatical perspective, their possibility to be solved by electrical simulators, particularly in the case of thermal networks, which are easily available, simple and accurate thermal models, is highly advantageous.
Many publications focused on lumped elements thermal dynamics, as the work of Szekely about the *RC* transmission lines heat propagation description, Network Identification Deconvolution (NID) method [131], [111], and the introduction of the concept of structure function in electronic packages [132]. Another work worthy to be remembered is the one concerning the determination of Boundary Condition Independent (BCI) compact thermal models of packages in electronic industry ([129], [130]) elaborated during the DELPHI project. Other several methods have been shown by Schweitzer [133], which are aimed at determining the coefficients of thermal networks, the topology of which was defined a priori depending on the most favorable heat propagation. These methods explains the self and mutual heating when multiple sources are considered. Two categories of LEMs can be identified: physical models linked to the described systems physical layers and features [94], [91], [126]; and empirical models which capture the response of the studied system [90], [134]. Since lumped element physical models are cumbersome when built, and so they lose in computational lightness, accurate behavioral models should be developed, a general determination of which can be [135]. Instead, [136], [137], [138] and [139] are examples of applications of electro-thermally coupled simulations or different dynamics coupling. What is desirable is the identification of a methodology to determine LEM that features the following characteristics:

- high accuracy;
- high computation speed;

- capability of solving non-linearities, as those related to material properties and boundary conditions [140], [141];
- capability of solving the presence of multiple heat sources and multiple observation points.

Actually, the most thorough simulation methodology is FEM, but it loses in simulation speed [117], [114]; on the contrary, what gives a greater performance in terms of simulation speed are the standard lumped element models, but they lack in accuracy (description of non-linearities). This work focuses on the presentation of a generalized approach featuring all the required characteristics in a lumped element model. The following points/steps sum up the approach here described by considering a multiple-heat-sources and multiple-observation-points non-linear system:

1. a calibration bench is manufactured, which interacts with multiple heat sources;
2. a fully 3D non-linear FEM model is built and calibrated by measurements;
3. self and mutual non-linear thermal transient resistance curves are extracted from the calibrated FEM model;
4. the equivalent non-linear compact thermal model is determined;
5. the developed procedure is tested.

The aim of this work is the development and interconnection of non-linear Foster networks through a system description based on the representation required. As said before, this methodology will determine a non-linear Foster network that will be extended to multiple-heat-source systems, and validated against measurements.

5.2 Thermal system classification

The following is a possible classification of thermal systems.

5.2.1 SISO

A single network can model a SISO (Single Input, Single Output) thermal system (see [142] for instances). Since a linear thermal network is a constant-elements network, this can be used to fit a thermal impedance curve as its behavior does not depend on the power dissipation level. A SISO system could be described by:

$$\Delta T_1 = Z_{TH,11} P_1 \tag{5.1}$$

5.2.2 SIMO

To describe any location in the device (the hot spot, as well as any other point far from the active region) such kind of system is necessary. A system is defined as SIMO (Single Input, Multiple Output) when different points are monitored in a system, with just one heat source (see [143]). The matrix $(O \times 1)$, where O is the number of interest points in the response of the system, can mathematically define such a system:

$$\begin{bmatrix} \Delta T_1 \\ \vdots \\ \Delta T_O \end{bmatrix} = \begin{bmatrix} \Delta Z_{TH,11} \\ \vdots \\ \Delta Z_{TH,O1} \end{bmatrix} P_1 \tag{5.2}$$

The power dissipation in the active area is the power that is used as the network input; it is independent on the point it is referring to. Equation (5.3) defines the thermal impedance for systems with a single power source:

$$Z_{TH,o}(t) = \frac{\Delta T_o(t)}{P_1} = \frac{T_o(t) - T_{AMB}}{P_1} \tag{5.3}$$

5.2.3 MISO

This is the case according to which more than one dissipating device is identified, while the interest is in just one temperature location. A MISO (Multiple Input, Single Output) system is defined by a matrix notation $(1 \times F)$ as (5.4)

$$\Delta T_1 = \begin{bmatrix} Z_{TH,11} & \cdots & Z_{TH,1F} \end{bmatrix} \begin{bmatrix} P_1 \\ \vdots \\ P_F \end{bmatrix} \tag{5.4}$$

5.2.4 MIMO

The most common case is when F power sources are present and the temperature has to be observed in O different locations [144]. A MIMO (Multiple Input, Multiple Output) linear system presents an $(O \times F)$ matrix:

$$\begin{bmatrix} \Delta T_1 \\ \vdots \\ \Delta T_O \end{bmatrix} = \begin{bmatrix} Z_{TH,11} & \cdots & Z_{TH,1F} \\ \vdots & Z_{TH,of} & \vdots \\ Z_{TH,O1} & \cdots & Z_{TH,OF} \end{bmatrix} \begin{bmatrix} P_1 \\ \vdots \\ P_F \end{bmatrix} \tag{5.5}$$

here the indexes are, respectively, $o = 1, ..., O$ and $f = 1, ..., F$.

5.3 MIMO SPICE model implementation

All the descriptions previously analyzed are the application of Z_{TH}-matrix thermal systems. A circuit simulator can help in implementing all the topologies. Let us consider now a general case to give an instance: MIMO system, $O = 3$ observation points, $F = 2$ power dissipation sources, (3×2) matrix description as (5.6).

$$\begin{bmatrix} \Delta T_1 \\ \Delta T_2 \\ \Delta T_3 \end{bmatrix} = \begin{bmatrix} Z_{TH,11} & Z_{TH,12} \\ Z_{TH,21} & Z_{TH,22} \\ Z_{TH,31} & Z_{TH,32} \end{bmatrix} \begin{bmatrix} P_1 \\ P_2 \end{bmatrix} \tag{5.6}$$

Figure 5.1 shows an electrical simulator's implementation. Data are calculated separately; successively, the voltage controlled voltage sources produce the algebraic sum given by the connection in series of the generators, which are the partial contributions. Other configurations presented before can be considered as subsets of the MIMO system.

5.4 Non-linear Foster networks

The following pages will show a method to elaborate a non-linear Foster network from several thermal impedance curves deriving from different power dissipation

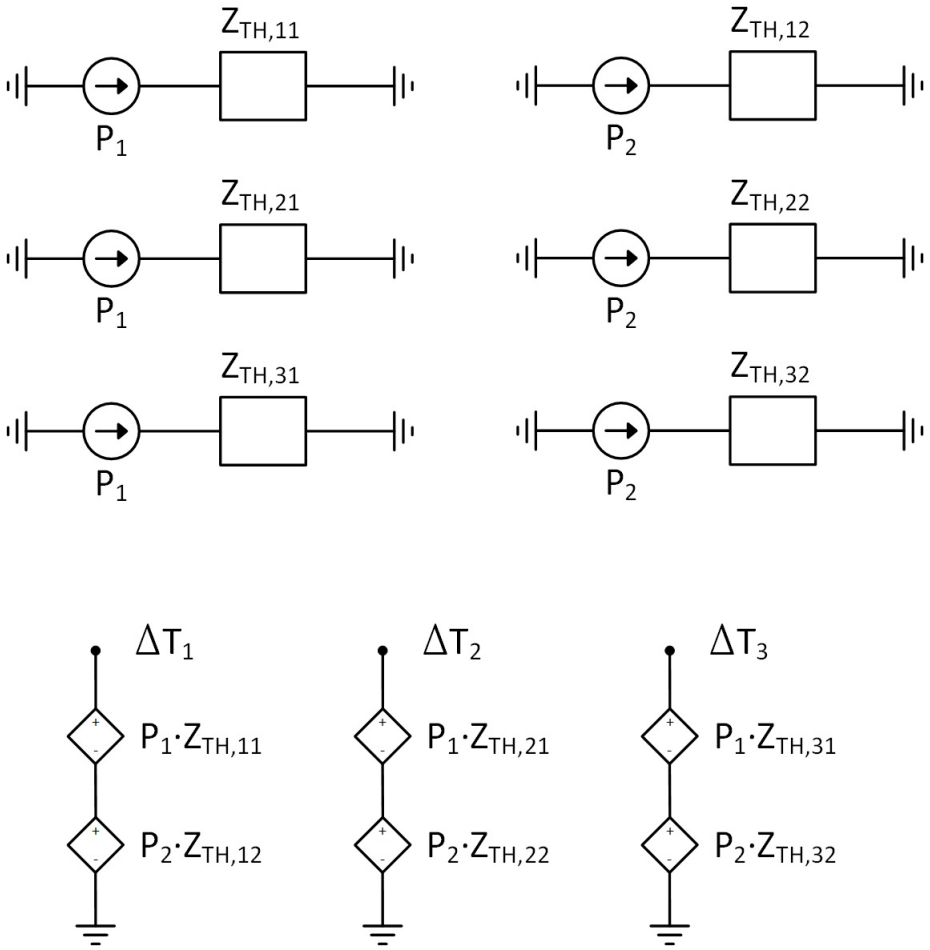

Figure 5.1: The schematic implementation of the MIMO system proposed in (5.6).

levels.

Generally, a given system produces a thermal response Z_{TH} which is commonly defined in Foster notation as a series of N exponential terms (3.18). Such kind of system is clearly linear.

A non-linear Foster network is often considered as a cluster of several Foster networks. We talk about "non-linear systems" when different power dissipation levels bring to different responses (i.e. different for P_0 and P_1).

$$Z_{TH,0}(t) = \frac{\Delta T(t)}{P_0} = \sum_{i=1}^{N_0} R_{TH,0}(1 - \exp(\frac{-t}{\tau_{i,0}})) \tag{5.7}$$

$$Z_{TH,1}(t) = \frac{\Delta T(t)}{P_1} = \sum_{i=1}^{N_1} R_{TH,1}(1 - \exp(\frac{-t}{\tau_{i,1}})) \tag{5.8}$$

In general $N_0 \neq N_1$, but it is always possible to find a N defined as (5.9), whose two responses have both the same number of terms.

$$N \geq \max(N_0, N_1) \tag{5.9}$$

If, for example, the topology of the network is fixed, so that the needed number of stages N is the same for every power dissipation level, it is possible to merge all the linear Foster networks into one single non-linear Foster network. The thermal resistances $R_{TH,1}, R_{TH,2}, ..., R_{TH,N}$ are terms that depend on the temperature of the first node of the network, the only node with a physical meaning. To be as clear as possible, Figure 5.2 describes the topology of just three stages. By keeping the capacitive terms constant [145], it is possible to build only accurate non-linear models with non-linear resistive terms. Furthermore, if the variation of each term $R_{TH,1}(T), R_{TH,2}(T), ..., R_{TH,N}(T)$ is monotonic, numerical problems are remarkably reduced. During the application of the model, the requirements were satisfied by a number of stages characterized by a nearby monotonic behavior of the terms which were non-linear and resistive as an input temperature function. If these conditions do not take place, it will be necessary to increase the number of stages N.

The following steps determine the procedure to create non-linear thermal model:

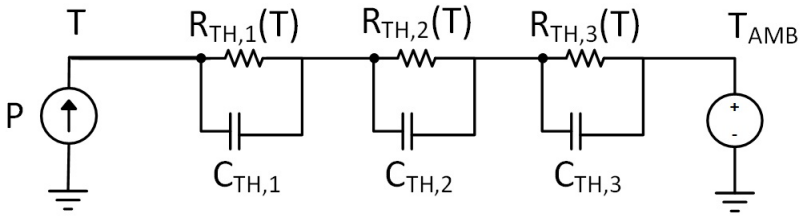

Figure 5.2: Example of 3-stage Foster network composed by R_{TH} temperature depedent thermal resistances.

1. increasing power dissipation levels $P_1, ..., P_Q$ with $P_1 < ... < P_q$ by generating a set of Z_{TH};

2. obtaining a linear Foster network which describes the thermal impedance through the performance of the standard procedure by starting from the lower power level P_q with $q = 1$; this phase will produce an initial number of stages N;

3. obtaining a linear Foster network through the use of coefficients resulting from the previous step P_q (these are considered, starting points for the optimization), by going to the next power level P_{q+1}; in other word, q Foster networks made of N stages will be obtained;

4. checking the values for $R_{TH,1}, ..., R_{TH,N}$ derived from the previous steps; the procedure will be considered successful if each power level fits the predictions and each resistive term respects its monotonicity. If the procedure cannot be considered successful, step 2) with $N = N + 1$ must be repeated.

To obtain the monotonicity of the resistive terms, a meticulous selection of the time constants should take place. The values of P_q will vary as easily as the values of a function of temperature; for this reason the monotonicity of the resistive terms should be achieved.
Essentially, the following equations represents the correct non-linear Foster network:

$$Z_{TH}(t) = \sum_{i=1}^{N} R_{TH,i}(1 - \exp(\frac{-t}{\tau_i(T)})) \tag{5.10}$$

$$\frac{R_{TH,i}(T)}{dT} \geq 0 \quad \text{or} \quad \frac{R_{TH,i}(T)}{dT} \leq 0 \; \forall i \in [1,N] \tag{5.11}$$

$$\frac{C_{TH,i}(T)}{dT} = 0 \; \forall i \in [1,N] \tag{5.12}$$

Figure 5.3 graphically illustrates the process. $R_{TH,i}(T_q)$ (where T_q is the temperature obtained at the input node of the given Foster network with an applied amplitude P_q step) is the resistance of the $i-th$ stage in case of power dissipation P_q. Resistive terms are variable and obtained through different power dissipation values. Figure 5.3.a, Figure 5.3.b and Figure 5.3.c show three examples of increasing power levels P_1, P_2 and P_3, respectively. The union of these three linear networks produces a non-linear Foster network; in this case, each resistance non-linearity is developed through a Look-Up-Table (LUT). Figure 5.3.d shows an example of a network where the LUT, in the first stage, is represented as follows: $(T_1, R_{TH,1}(T_1))$, $(T_2, R_{TH,2}(T_2))$, $(T_3, R_{TH,3}(T_3))$. To include the effect of different ambient temperatures, it is necessary to extend this approach; the result is a network where every resistive term is determined by a double-entry LUT, as seen in Figure 5.3.e.

When multiple heat sources are present and multiple locations need a modeled temperature, this process can be generalized and it will be defined as a MIMO system (Multiple Inputs, Multiple Outputs). The following defines a system with F power sources and O different locations described as an $(O \times F)$ matrix, where the temperature is monitored as in [146] and [144].

5.5 The Algorithm in detail

The designed algorithm presented before could be implemented through Algorithm 5.1, Algorithm 5.2, Algorithm 5.3 and Algorithm 5.4, that enunciate the general algorithm to obtain a non-linear Foster network.

In general, the algorithm, accomplishes an optimization process in order to extract the parameters of stages *RC* to be used in a SPICE simulation by considering the system's non-linearities.

Algorithm 5.1 receives inputs from all FEM simulations when T_{AMB} and T vary due to different power steps P. Hence, it calls the fit Algorithm 5.2, which carries out the

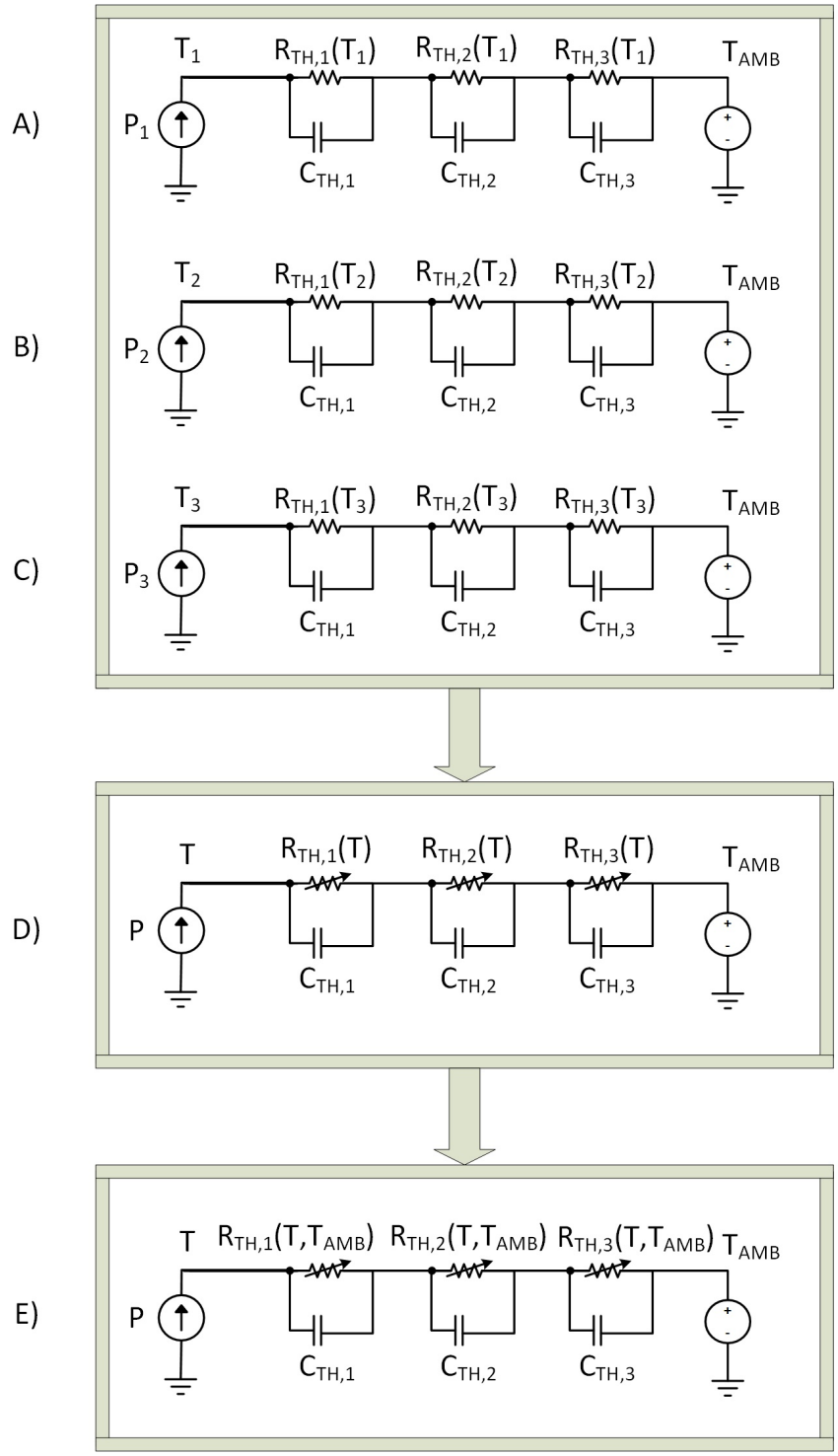

Figure 5.3: Illustration of the procedure in order to obtain a non-linear Foster network.

optimization process on FEM reference simulation (generally, the first FEM simulation with the lower power step). Squeeze Algorithm 5.3 is applied to R_{TH} and C_{TH} values, which, if necessary, reduces the number of *RC* stages (it suppresses too small values of thermal resistances). On the bases of the obtained results, the tracking Algorithm 5.4 is applied on all other FEM simulations. As a result, a Foster network able to consider non-linearities present in the system is obtained.
To conclude, it should be remembered that Algorithm 5.2 and Algorithm 5.4 use optimization solvers to solve problems introduced in (5.13) and (5.14). R_k and C_k are chosen as reference values from the previous simulation, while α, β, γ and δ are coefficients selected on the basis of the model.

$$\begin{gathered}
\min \sum_{l=0}^{Steps-1} [[\sum_{k=0}^{Stages-1} R_k(1-\exp(\frac{-t_l}{\tau_k}))] - Zth_l]^2 \\
\\
\sum_{k=0}^{Stages-1} R_k = Zth_{Steps-1} \\
R_k \leq Zth_{Steps-1} \forall k \in [1,...,Stages-1] \\
with\ k,l \in \mathscr{N} \\
with\ R_k \in \mathscr{R}^+
\end{gathered} \tag{5.13}$$

$$\begin{gathered}
\min \sum_{l=0}^{Steps-1} [[\sum_{k=0}^{Stages-1} R_k(1-\exp(\frac{-t_l}{R_k C_k}))] - Zth_l]^2 \\
\\
\sum_{k=0}^{Stages-1} R_k = Zth_{Steps-1} \\
\alpha \bar{R_k} \leq R_k \leq \beta \bar{R_k} \forall k \in [1,...,Stages-1] \\
\gamma \bar{C_k} \leq C_k \leq \delta \bar{C_k} \forall k \in [1,...,Stages-1] \\
with\ k,l \in \mathscr{N} \\
with\ R_k, C_k \in \mathscr{R}^+
\end{gathered} \tag{5.14}$$

5.6 Validation of the non-linear Foster network

This section will deal with the demonstration of the non-linear Foster network algorithm. The first step was to build a non-linear FEM model of a power device and to apply boundary conditions; the aim was to develop strong gradients, and appreciable non-linearities as a consequence, inside the structure. As Figure 5.4 [147] shows, the

Algorithm 5.1 Non-linear Foster network

```
// N_Tamb is the number of Ambient Temperatures
// N_P is the number of Powers for every Ambient
// Temperature
// RC is the object that contains thermal
// resistances (R[Stages]) and thermal capacitance
// (C[Stages])
// Thermal_experiment is the object that contains
// the experiment composed by time t[Steps],
// temperature T[Steps] and power P[Steps]
// Populate() is a function which extract datas
// from thermal simulation and organized them in a
// matrix of objects

Thermal_experiment[N_Tamb][N_P]=populate();
RC[0][0]=Algorithm1(Thermal_experiment[0][0])
Squeeze(RC[0][0])
For(i=0;i<N_Tamb;i=i+1)
For(j=0;j<N_P;j=j+1)
If(j==0)
If(i!=0)
RC[i][j]=Algorithm2(Thermal_experiment[i][j],RC[i-1][0])
Else
RC[i][j]=Algorithm2(Thermal_experiment[i][j],RC[i][j-1])
```

Algorithm 5.2 Fit-algorithm

```
// N_Tamb is the number of Ambient Temperatures
// N_P is the number of Powers for every Ambient
// Temperature
// RC is the object that contains thermal resistances
// (R[Stages]) and thermal capacitance (C[Stages])
// Experiment is the object that contains the experiment
// composed by time t[Steps], temperature T[Steps] and
// power P[Steps]
// Calc() is a function to initialize TAU

INPUT: Experiment
OUTPUT: RC
Stages=0
Obj=MAX_REAL
Min_Obj=MAX_REAL
Tempobj=NULL
While(obj>=TOLERANCE AND Stages<MAX_STAGES)
Stages=Stages+1
TAU[Stages]=calc()
obj=(4.13)
If(obj<Min_Obj)
obj=Min_Obj
Tempobj=obj.R
RC.R=Tempobj.R
RC.C=TAU/obj.R
```

Algorithm 5.3 Squeeze

```
// N_Tamb is the number of Ambient Temperatures
// N_P is the number of Powers for every Ambient
// Temperature
// RC is the object that contains thermal resistances
// (R[Stages])
// and thermal capacitance (C[Stages])
// Thermal_experiment is the object that contains the
// experiment composed by time t[Steps], temperature
// T[Steps] and power P[Steps]

Stages=Stages(RC)
For(k=0;k<Stages;k=k+1)
If(RC.R[k]<=MIN_R)
delete(RC.R[k])
delete(RC.C[k])
Stages=Stages-1
k=k-1
```

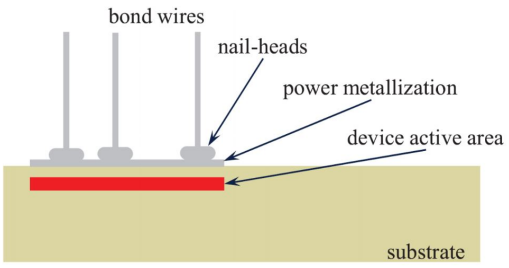

Figure 5.4: Typical device structure of a MOSFET with bonding.

Algorithm 5.4 Tracking-algorithm

```
// N_Tamb is the number of Ambient Temperatures
// N_P is the number of Powers for every Ambient
// Temperature
// RC is the object that contains thermal resistances
// (R[Stages]) and thermal capacitance (C[Stages])
// Thermal_experiment is the object that contains
// the experiment composed by time t[Steps],
// temperature T[Steps] and power P[Steps]

INPUT: Experiment, RCbar
OUTPUT: RC
Stages=Stages(RCbar)
Alpha=define()
Beta=define()
Gamma=define()
Delta=define()
Obj=(4.14)
RC.R=Obj.R
RC.C=Obj.C
```

bottom of the device is kept at constant temperature, and the power dissipation occurs in the active area:

- even if this boundary condition is practically unrealistic for long pulses, it is, anyway, numerically interesting, because of the strong gradients taking place in a transient operation, which is a relevant benchmark for the proposed algorithm;

- a realistic condition is given (as in [148] and [149]) by the boundary conditions originating from an almost constant temperature at the bottom location, where, for short pulses, the heat wave vanishes within the thick substrate.

The maximum temperature of the device corresponds to its thermal impedance and it is calculated for $Q = 3$ power dissipation levels: 10, 220 and 440 W. The effect of the non-linearity of the substrate on the thermal impedance for all the different power levels is represented by Figure 5.5 [147].
To highlight the non-linear bahvior, $Q = 45$ simulations were realized, starting the power from $P_1 = 3$ W to $P_{45} = 440$ W. Such a structure proved to be modeled by a Foster network with $N = 7$ stages. The monotonic dependence of the resistances is shown in Figure 5.6 [147], marked out as a function of the maximum temperature that the device could reach. Evidently, $R_{TH,i}$ non-linear resistive terms are dependent on the maximum temperature reached at every $q = 1,...,Q$ power step level. It is possible to note that the time constants $\tau_i = R_{TH,i}C_{TH,i}$ vary with the variation of the thermal resistances, since thermal capacitance values are kept at a constant level as a function temperature.
To supply a further validation, it was necessary to consider a series of three short-circuit pulses: at the moments of high peak power delivering, the non-linear response of the FEM model is highlighted. Figure 5.7 [147] explains the excellent agreement between the compact model and the FEM model: the most remarkable difference between the two versions is that the FEM model may need up to (few) hours to simulate, while the compact version requires just few seconds.

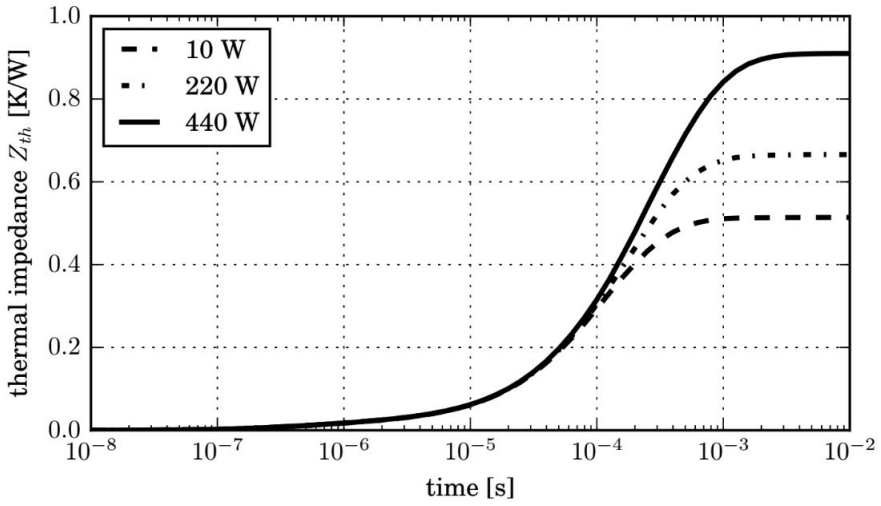

Figure 5.5: Thermal impedance of a power MOSFET subjected to different power levels.

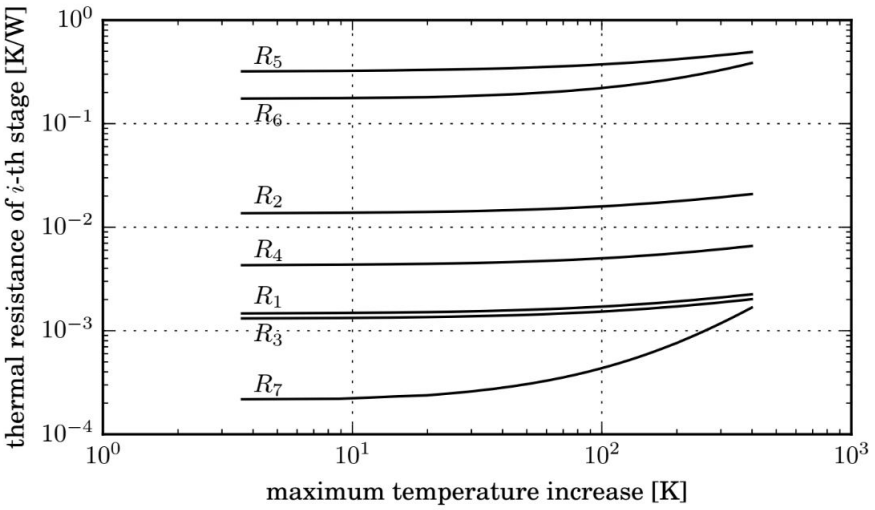

Figure 5.6: Monotonic variation of $R_{TH,i}$ as a function of temperature increase.

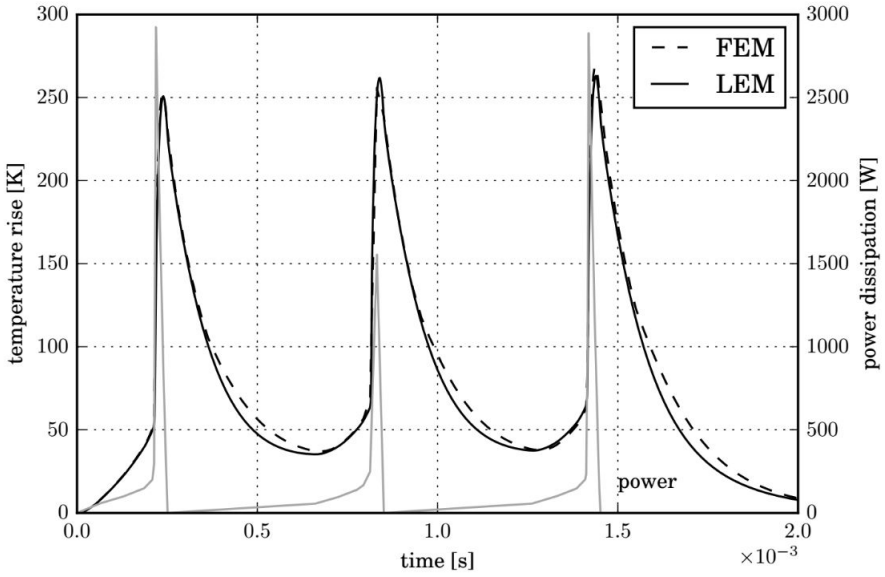

Figure 5.7: Comparison between simulation results obtaines by FEM model and non-linear Foster network of the system subjected to a power pulse.

5.7 Experimental validation

This section deals with the application of the methodology to a real case. The main steps of this approach are the following: design and manufacturing of an ad-hoc PCB, development and tuning of its non-linear transient thermal FEM model, extraction of the thermal responses of interest, and developing of the compact MIMO model.

5.7.1 Test bench design and manufacturing

As Figure 5.8 [147] shows, three MOSFETs (independently operated) constitute the PCB. Here, the components have been designed to improve their thermal interactions: the top side (Figure 5.9.a [147]) has been realized with an optically transparent matt paint so that the emissivity could be uniformed on all the surfaces made of different materials. In order to keep the top side cleared of bulky components, all the electrical biasing and test points connections are mounted on the edges of the board, on the bottom side of the PCB. Such a board is made up of a thick FR-4 substrate (1.6 mm) with a 35 μm single thick copper layer. Otherwise, the bottom side has been thermally insulated by a 6 mm thick glass wool layer (Figure 5.9.b [147]). Finally, the lateral surfaces of the board are sufficiently small to neglect the heat flow running through them. As Figure 5.10 [147] underlines, each device can be independently biased; the temperature distributed on the whole board is measured by IR thermography, while a Digital AcQuisition device (DAQ) automatically records the electrical signals.

5.7.2 Tuning of the FEM model

The simulation software library collects all the physical properties (e.g. thermal conductivity and heat capacity) of the materials that make the system up. On the contrary, the heat transfer coefficient h modeling natural convection has been set as a typical non-linear function; this method highlights the fact that heat exchange efficiency increases when the temperature difference between the surface and the surrounding ambient increases as well:

$$h = \alpha(T - T_{AMB})^{\beta} \tag{5.15}$$

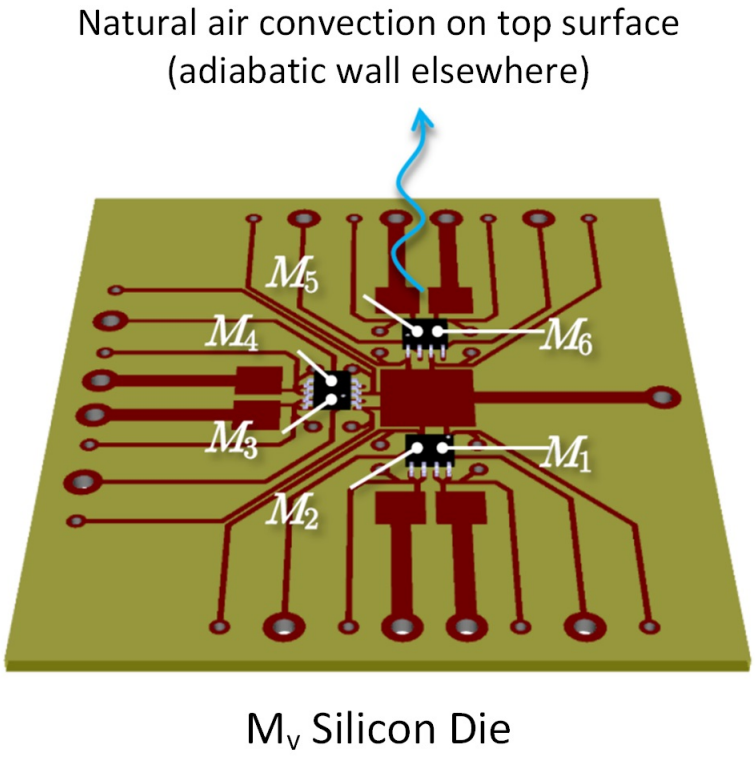

Figure 5.8: 3-D geometry of the studied system with boundary conditions (designed with KiCAD 4.0.2).

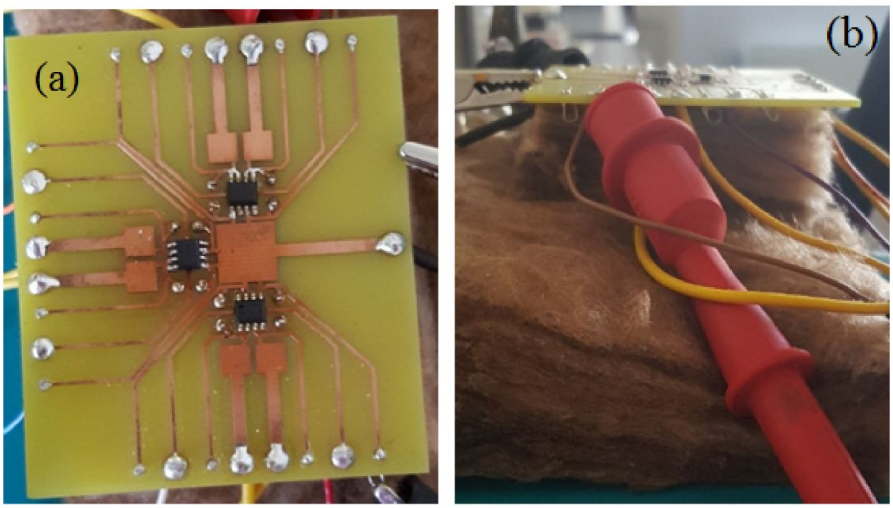

Figure 5.9: The multisource test board used to validate the studied system (glass wool in order to implement adiabatic bottom side); a) top view; b) side view.

The following figure of merit has been used to validate the fitting parameters:

$$|E\%| = \frac{|\Delta T_{meas} - \Delta T_{sim}|}{\Delta T_{meas}} \cdot 100 \tag{5.16}$$

here ΔT_{meas} represents the measured average ambient temperature increase, while ΔT_{sim} is the simulated average ambient temperature increase. The maximum allowed error corresponds to 10%. Since each package contains two devices, the surface-averaging has been obtained over half top surface of the mold compound:

$$T_{avg} = \int_{A/2} T(x,y)dA \tag{5.17}$$

COMSOL Multiphysics supplies the usual post-processing quantity; what allowed to find the coefficients in (5.15) was a series of measurements at different power dissipation levels: $\alpha = 7\mathrm{Wm^2K^{(1+)}}$ and $\beta = 0.155$. The coefficients errors listed in Table 5.1 and Table 5.2 are always far below the 10% threshold. The validated FEM simulations will extract $Z_{TH,of}(T)$. The following section will describe this process.

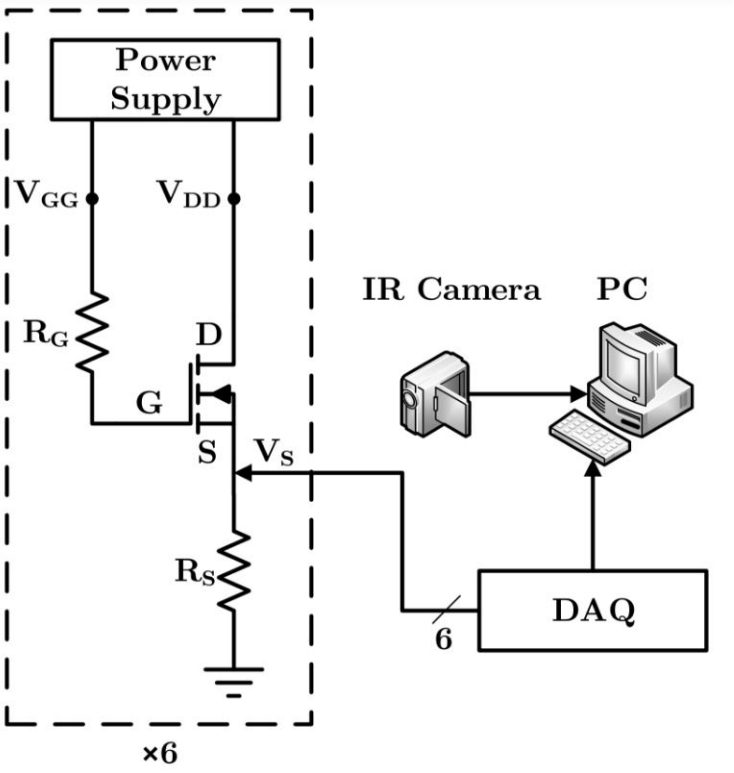

Figure 5.10: Schematic diagram of the test bench built to validate the FEM modeling of a MIMO system. An infrared camera is used to measure the temperature of the surfaces exposed to the air, a DAQ board measures the voltage of the MOSFETs' source V_S, used to evaluate the voltage V_{DS} and the current I_D. All the data are collected by a PC.

Device ON (dissipated power)	$\Delta T_{meas} - \Delta T_{sim}$ **[K]**	$\lvert E\% \rvert$
M_1 (0.68 W)	3.4	4.7
M_2 (0.64 W)	0.4	0.6
M_3 (0.60 W)	-3.7	5.3
M_4 (0.58 W)	-3.8	5.6
M_5 (0.65 W)	0.3	0.4
M_6 (0.66 W)	2.1	2.9

Table 5.1: Errors evaluation on devices turned ON.

Device ON (dissipated power)	$\Delta T_{meas} - \Delta T_{sim}$ **[K]**	$\lvert E\% \rvert$
M_1 (0.68 W)	2.6	5.1
M_2 (0.64 W)	0.3	0.6
M_3 (0.60 W)	0.6	1.3
M_4 (0.58 W)	-3.2	6.4
M_5 (0.65 W)	2.9	5.8
M_6 (0.66 W)	2.8	5.6

Table 5.2: Errors evaluation on devices beside the device turned ON.

5.7.3 Validation of the FEM model

Infrared thermal measurements validated the FEM model, concerning different power levels and configurations. Figure 5.11, Figure 5.12, Figure 5.13, Figure 5.14, Figure 5.15 and Figure 5.16 show a good agreement between measured and simulated temperature distribution. The FEM model and the measurements showed a good agreement. For this reason, the FEM model has been employed to generate the transient self- and mutual-impedances curves, later to be processed by the non-linear Foster fit algorithm.

5.7.4 Determination of the Z-matrix representing the system

The terms of the Z-matrix are obtained by indicating with o the location of interest, as the response location, and with f the device dissipating a power P:

$$Z_{TH,of} = \left.\frac{\Delta T_o}{P_f}\right|_{P_r=0,\forall r\neq f} \quad \text{for } o = 1,...,O \text{ and } f = 1,...,F \tag{5.18}$$

here, $\Delta T_o = T_o - T_{AMB}$. It is possible to rewrite (5.18) by taking into consideration the q-th level of the power steps:

$$Z_{TH,ofq} = \left.\frac{\Delta T_{oq}}{P_{fq}}\right|_{P_r=0,\forall r\neq e} \quad \text{for } o = 1,...,O \text{ and } f = 1,...,F \tag{5.19}$$

After the definition of non-linear $Z_{TH,of}(T)$, the non-linear Foster networks terms of Z-matrix can be identified. The complete system is proposed of Figure 5.8 is given by:

$$\begin{bmatrix} \Delta T_1 \\ \Delta T_2 \\ \Delta T_3 \\ \Delta T_4 \\ \Delta T_5 \\ \Delta T_6 \end{bmatrix} = \begin{bmatrix} Z_{TH,11} & Z_{TH,12} & Z_{TH,13} & Z_{TH,14} & Z_{TH,15} & Z_{TH,16} \\ Z_{TH,21} & Z_{TH,22} & Z_{TH,23} & Z_{TH,24} & Z_{TH,25} & Z_{TH,26} \\ Z_{TH,31} & Z_{TH,32} & Z_{TH,33} & Z_{TH,34} & Z_{TH,35} & Z_{TH,36} \\ Z_{TH,41} & Z_{TH,42} & Z_{TH,43} & Z_{TH,44} & Z_{TH,45} & Z_{TH,46} \\ Z_{TH,51} & Z_{TH,52} & Z_{TH,53} & Z_{TH,54} & Z_{TH,55} & Z_{TH,56} \\ Z_{TH,61} & Z_{TH,62} & Z_{TH,63} & Z_{TH,64} & Z_{TH,65} & Z_{TH,66} \end{bmatrix} \begin{bmatrix} P_1 \\ P_2 \\ P_3 \\ P_4 \\ P_5 \\ P_6 \end{bmatrix} \tag{5.20}$$

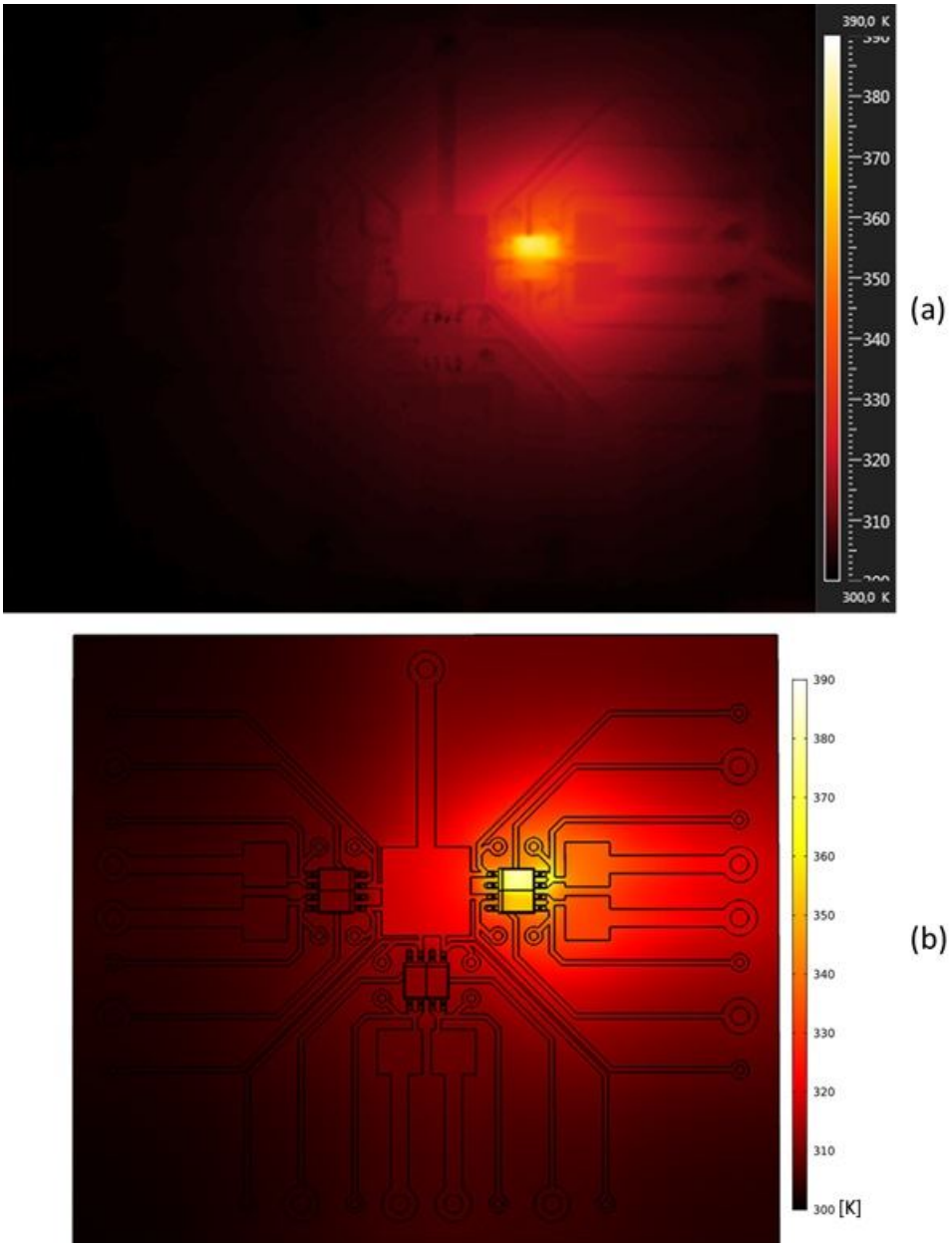

Figure 5.11: M_1 ON with $P_1 = 0.68$ W and $T_{AMB} = 298.75$ K, comparison between a) IR-thermography and b) FEM simulation.

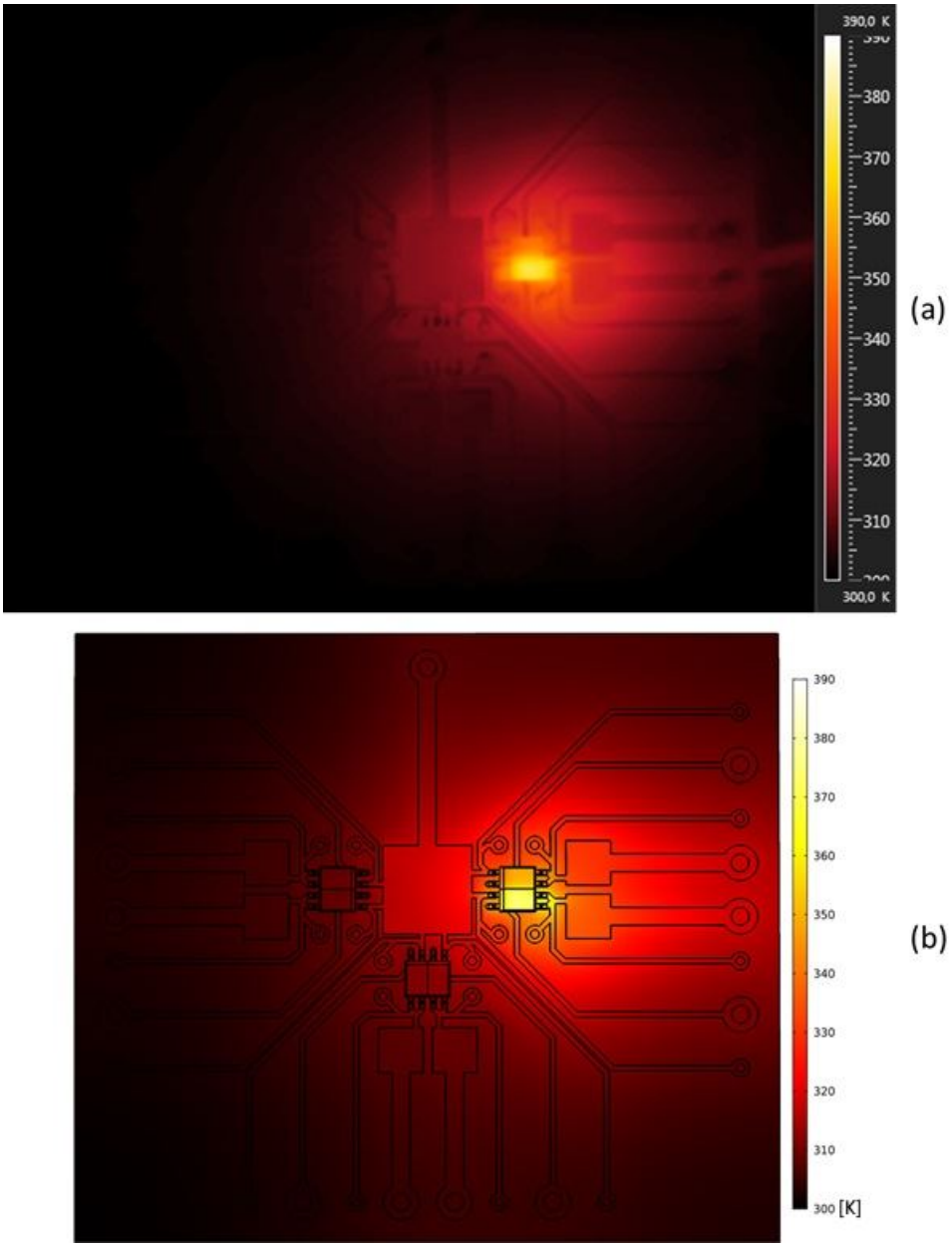

Figure 5.12: M_2 ON with $P_2 = 0.64$ W and $T_{AMB} = 298.75$ K, comparison between a) IR-thermography and b) FEM simulation.

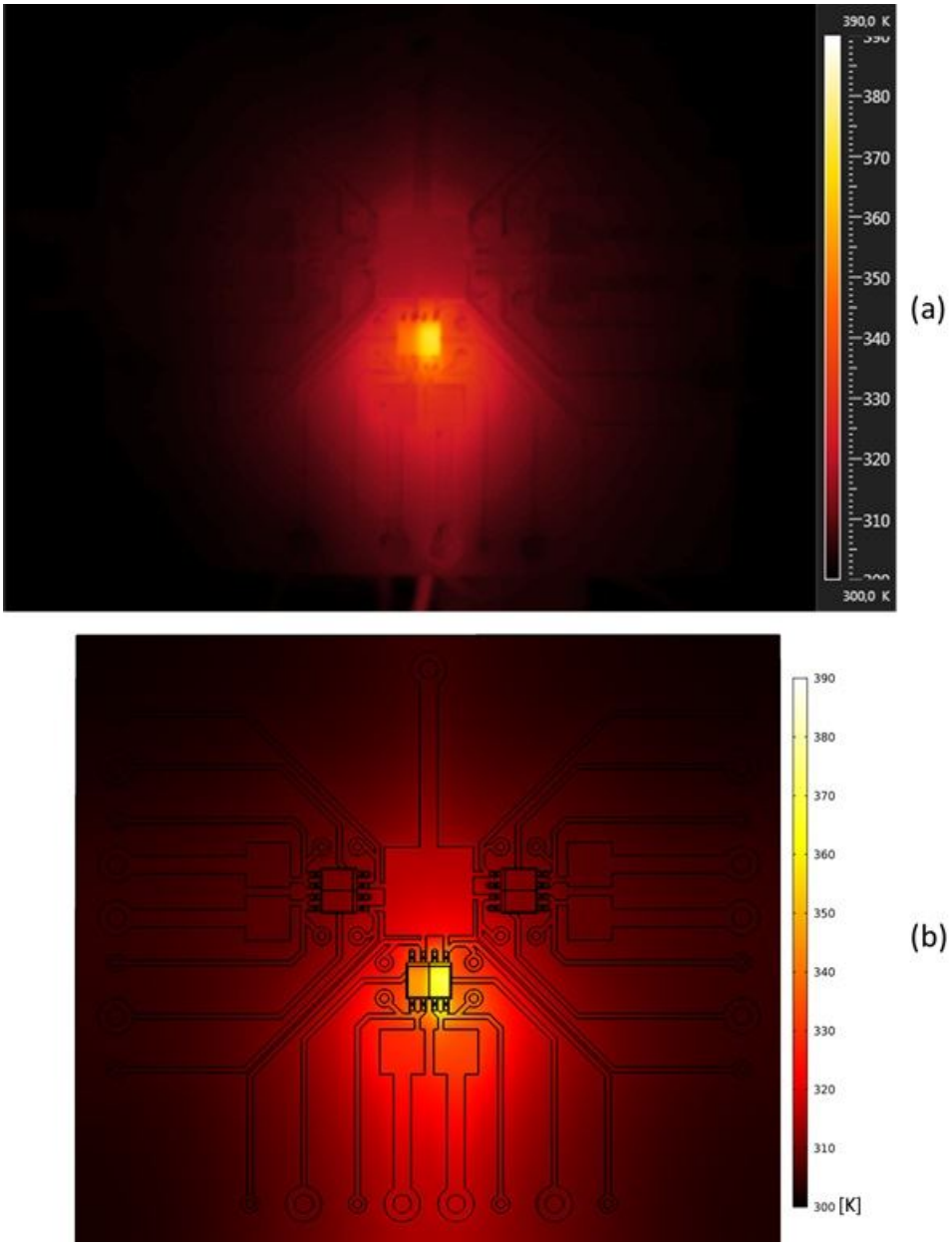

Figure 5.13: M_3 ON with $P_3 = 0.60$ W and $T_{AMB} = 298.75$ K, comparison between a) IR-thermography and b) FEM simulation.

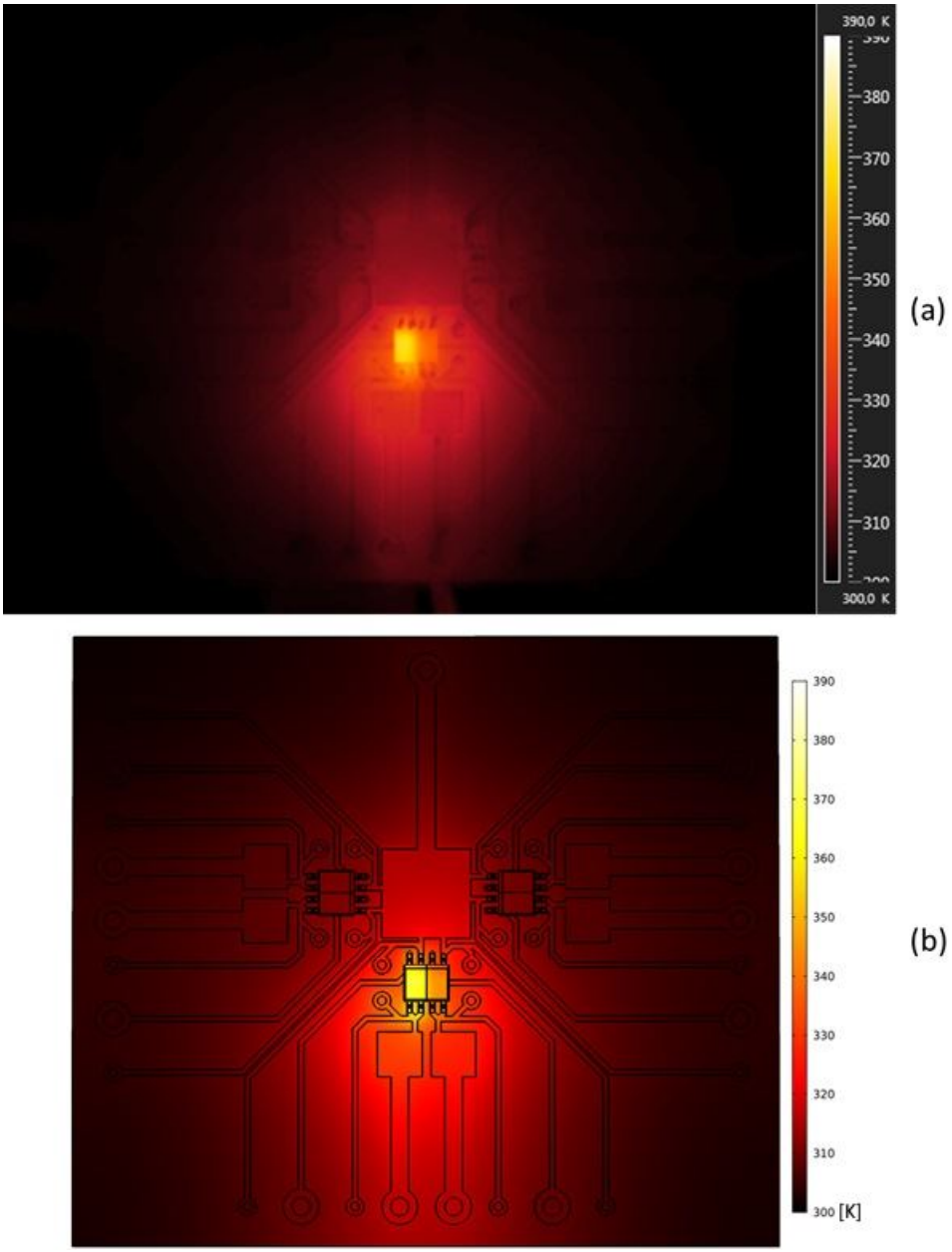

Figure 5.14: M_4 ON with $P_4 = 0.58$ W and $T_{AMB} = 298.75$ K, comparison between a) IR-thermography and b) FEM simulation.

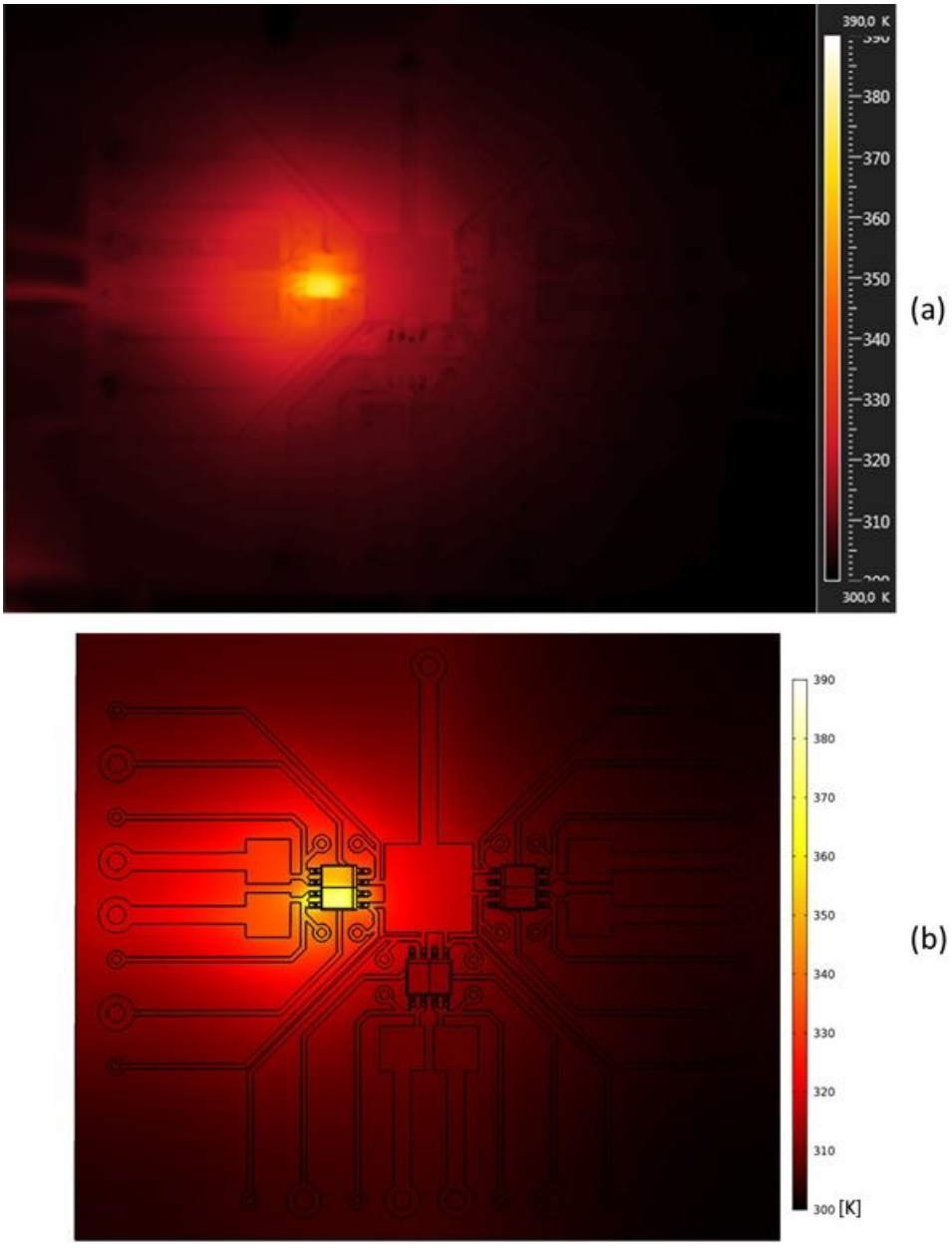

Figure 5.15: M_5 ON with $P_5 = 0.65$ W and $T_{AMB} = 298.75$ K, comparison between a) IR-thermography and b) FEM simulation.

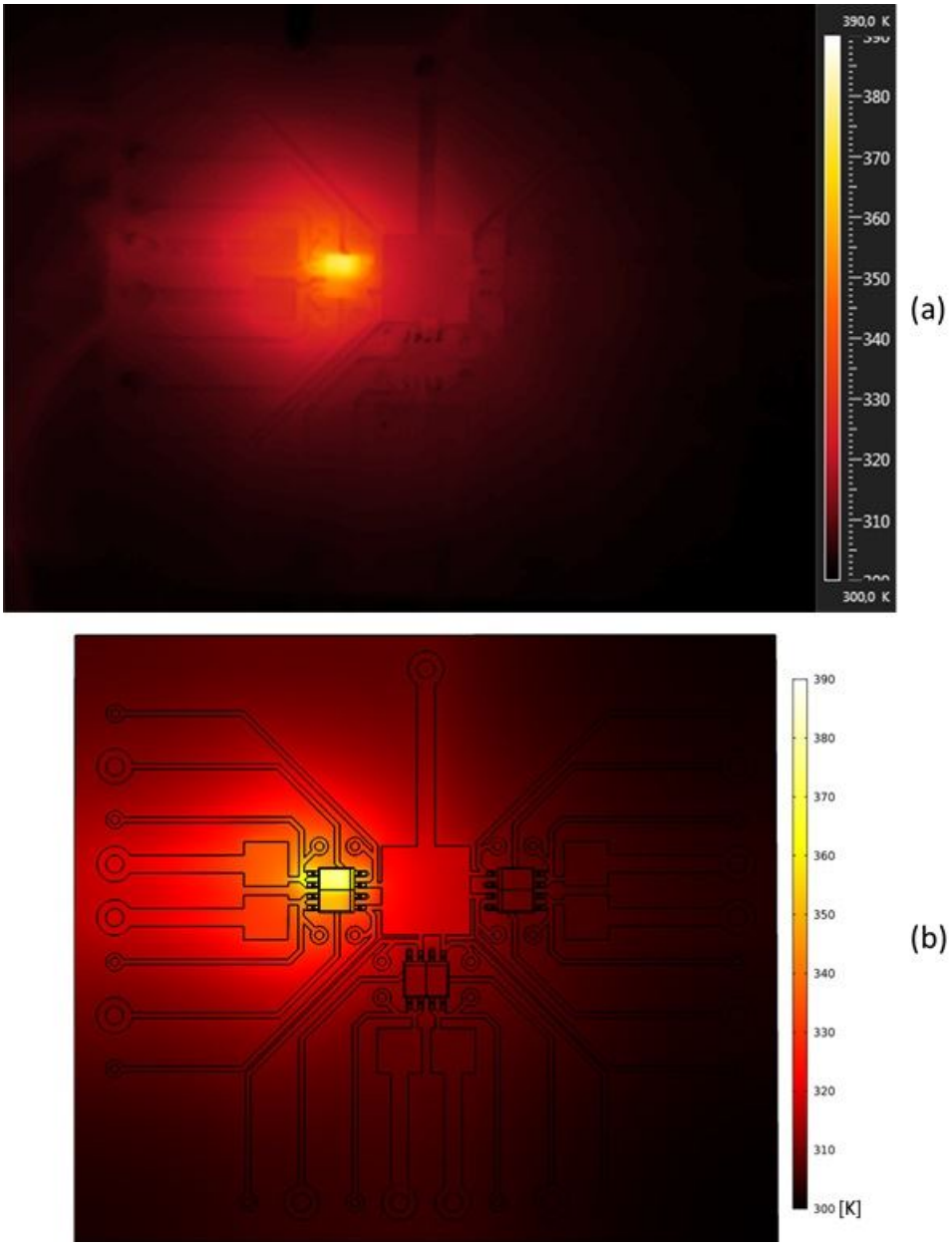

Figure 5.16: M_6 ON with $P_6 = 0.66$ W and $T_{AMB} = 298.75$ K, comparison between a) IR-thermography and b) FEM simulation.

The FEM model of Figure 5.8, which was previously validated, has been used to generate a 3-by-3 MIMO description of the system (only 3 devices were studied); in this case, the input is the dissipated power in M_2, M_4 and M_6 MOSFETs, while the outputs are the temperatures T_2, T_4 and T_6 of the same device:

$$\begin{bmatrix} \Delta T_2 \\ \Delta T_4 \\ \Delta T_6 \end{bmatrix} = \begin{bmatrix} Z_{TH,24} & Z_{TH,24} & Z_{TH,26} \\ Z_{TH,42} & Z_{TH,44} & Z_{TH,46} \\ Z_{TH,62} & Z_{TH,64} & Z_{TH,66} \end{bmatrix} \begin{bmatrix} P_2 \\ P_4 \\ P_6 \end{bmatrix} \tag{5.21}$$

Figure 5.17 shows a possible implementation of the matrix 5.21 in SPICE: by using VCVSs (Voltage Controlled Voltage Sources), the sum of the terms on each row can be implemented to a SPICE model. From FEM simulations, it has been possible to extract the $Z_{TH,of}$ terms with $T_{AMB} = 298$ K and $Q = 7$ different power steps with $P_q = 0.05, 0.1, 0.2, 0.3, 0.4, 0.5, 0.6$ W. The devices were turned on with different power steps, whereas the others were kept in OFF state. To extract the non-linear Foster networks associated to the Z-matrix, it has been necessary to run (3×7) transient simulations to obtain $(3 \times 3 \times 7)$ $Z_{TH,ofq}(t)$.

The product $(O \times Q)$ can define the number of simulations actually requested to fill any Z-matrix. Generally, O represents the number of independent heat sources operating in the system, while Q represents the number of power dissipation levels necessary to capture the non-linearity in the system. In this case, the heat sources operating in the system will be M_2, M_4 and M_6 which will be turned on singularly. New simulations will not be necessary because of the number of the observed responses, and because of the FEM simulation according to which the response of every point of the structure is consequently available to be consulted.

After the computation of the (3×7) non-linear Foster networks, the successive step would be the comparison of the responses of the compact element model with the ones obtained by FEM simulations in four different cases of application:

1. three equal steps at the same time to M_2, M_4 and M_6, 0.2 W power level;
2. three equal steps at the same time to M_2, M_4 and M_6, 0.4 W power level;
3. three different steps at the same time to M_2, M_4 and M_6, 0.2, 0.35 and 0.5 W respectively;

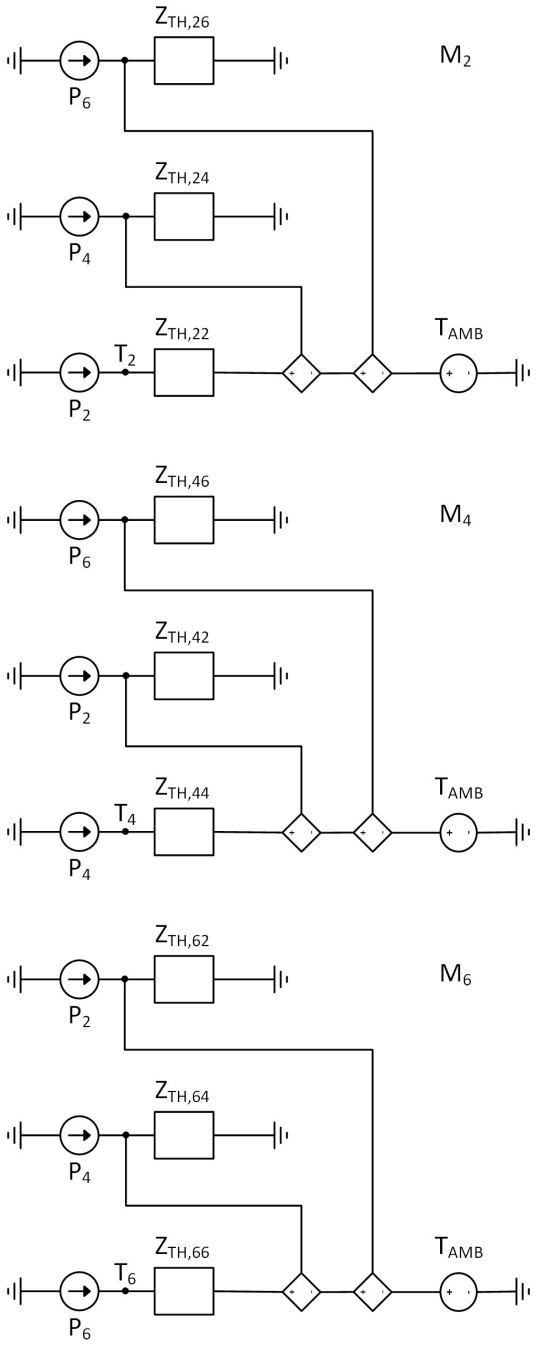

Figure 5.17: Schematic of the thermal circuit of a 3-by-3 MIMO system. VCVS elements are used to model the effect of mutual heating.

4. three different steps at the same time to M_2, M_4 and M_6, 0.55, 0.15 and 0.025 W respectively.

Table 5.3 shows the errors at steady state between FEM and SPICE simulations in these three cases, since different thermal situations from those used to generate the model were used in order to challenge it. Figure 5.18, Figure 5.19, Figure 5.20 and Figure 5.21 show the four different cases in non-stationary conditions. The proposed

Case study	$\mathbf{M_2}\|\mathbf{E}\%\|$	$\mathbf{M_4}\|\mathbf{E}\%\|$	$\mathbf{M_6}\|\mathbf{E}\%\|$
1	1.32	1.23	1.32
2	3.28	3.30	3.27
3	4.20	2.94	1.98
4	0.55	2.54	2.59

Table 5.3: Case studies errors evaluation.

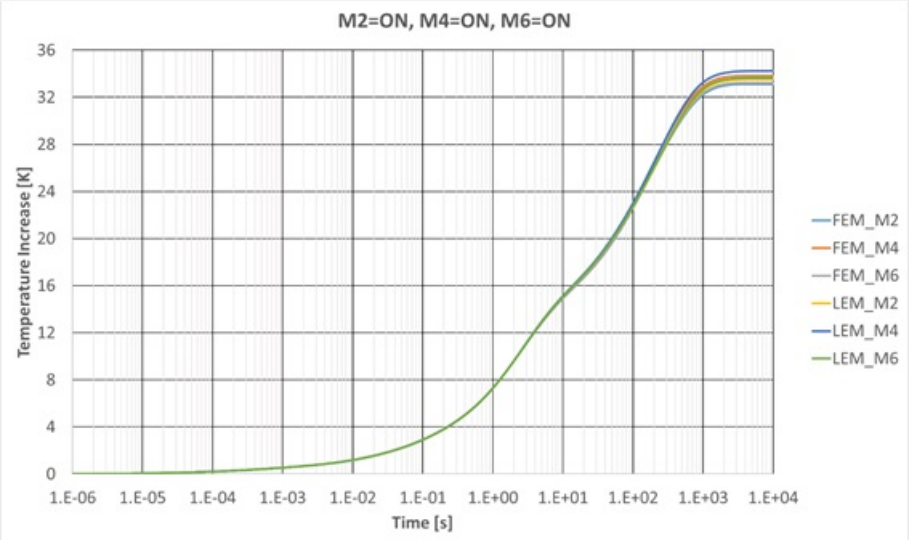

Figure 5.18: First case study; comparison between FEM and LEM developed with the new approach.

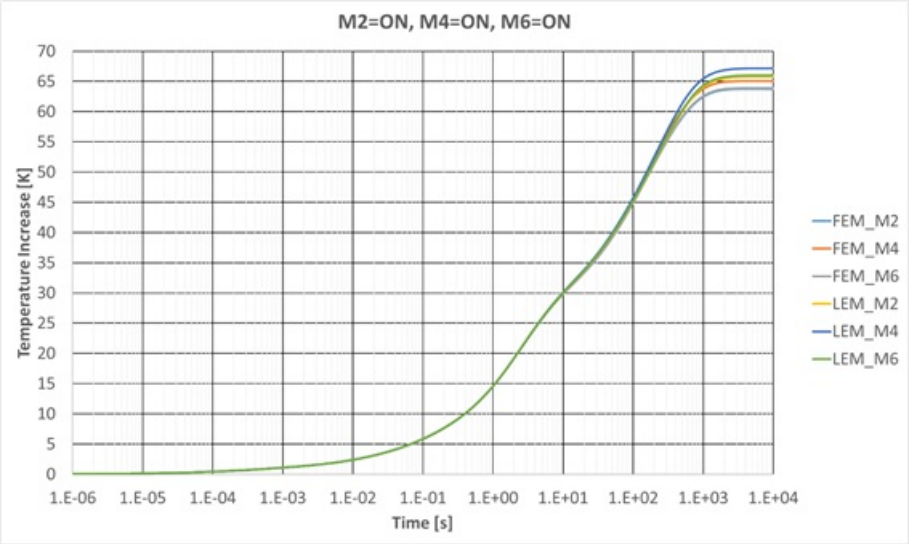

Figure 5.19: Second case study; comparison between FEM and LEM developed with the new approach.

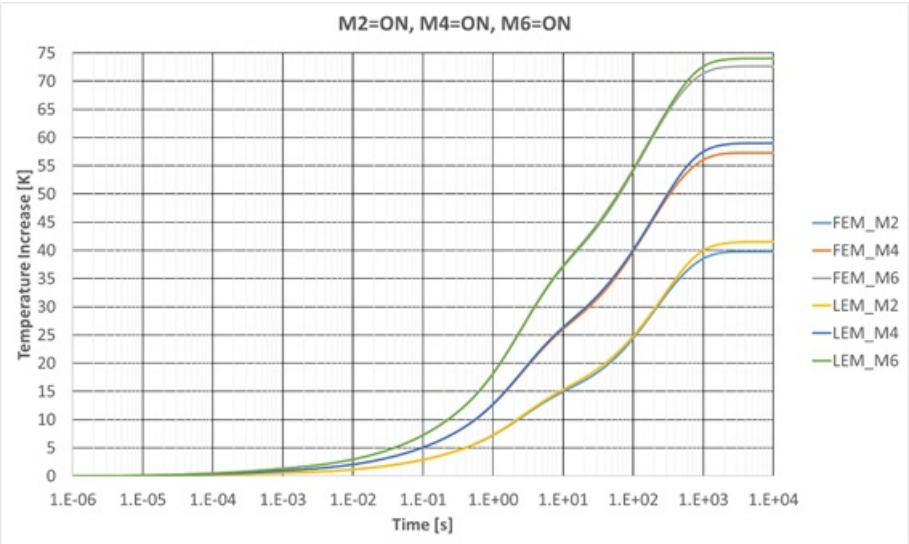

Figure 5.20: Third case study; comparison between FEM and LEM developed with the new approach.

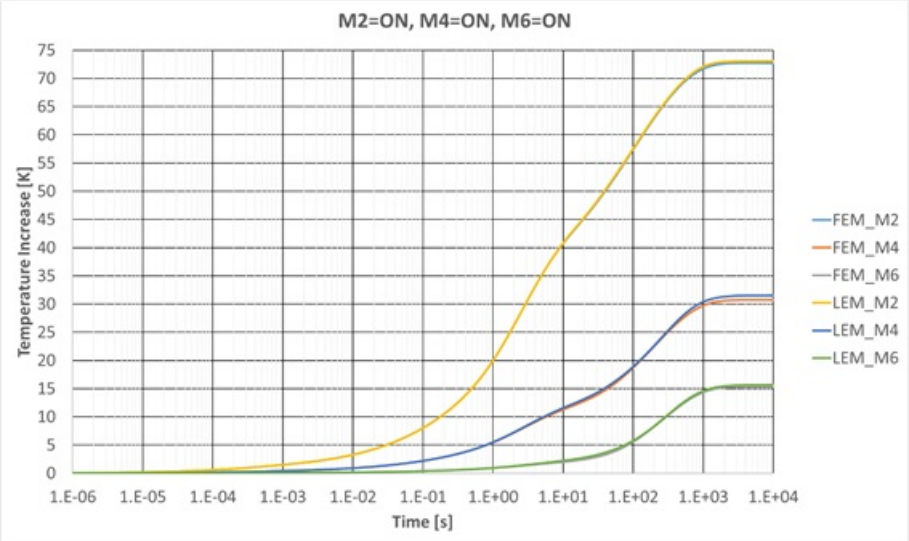

Figure 5.21: Fourth case study; comparison between FEM and LEM developed with the new approach.

procedure with multiple heat sources proves its validity as the results are valuable. As a matter of fact, the maximum recorded $|E\%|$ is lower than 5%.

5.8 Results discussion

The determination process proposed by this work concerns the creation of non-linear Foster networks and able to describe the behavior of thermal systems with strong non-linearities, multiple power dissipation nodes and multiple observed responses.
The key aspect of this kind of applications is in the coupling with other models (as the electronic devices electro-thermal ones) to realize a fully-coupled, multi-physical simulation perspective which can be solved by electrical simulators, for long and complex mission profiles, as well as fast solving models.
A family of thermal impedance curves lies at the bases of this methodology to capture the effect of non-linearities in the system. As described in this work, the curves

may be obtained through a carefully tuned FEM model of the system, or through measurements, but only if these are available. The first step to realize is to develop an appropriate FEM model to derive all the needed thermal impedance curves.
Two are the phases to validate the process: first, one should determine the non-linear Foster network through a non-linear transient FEM benchmark simulation of a MOSFET under high power dissipation levels. By assuming that the different non-linear contributions can be superposed, it is possible to model MIMO systems; this way, a Z-matrix description can be implemented in a SPICE simulator, of which validity and limitations were analyzed through an ad-hoc developed PCB. The FE model and the compact model reached good agreement. Even if this linear superposition is not theoretically justified, it generates small errors.
The benefit characterizing these model approaches is the small amount of time requested to run simulations. Lumped element model needs a shorter simulation time if compared to that asked by FEM simulations. Furthermore, it can be integrated with electro-thermal models of electron devices, while FEM cannot. An effective example can be found in this work, where a transient FEM simulation is demonstrated to be completed in 4 hours, while the SPICE equivalent simulation requires around 1 minute.
Finally, it was to be remarked the essential use of Python 3.5 [150] to develop the algorithm for the extraction of non-linear Foster networks. Moreover, the electrical simulations were realized by LT-Spice IV [23] which allows to define non-linear elements, as resistors for this case, through the use of LUTs and behavioral models.

Chapter 6

Neural network electro-thermal LEM

The better we get at getting better,
the faster we will get better.

– Douglas Carl Engelbart

This chapter presents a procedure for the creation of a compact model able to capture the thermally dependent electrical behavior of an electronic system. A novel approach is developed, with the purpose of generating models for simulation of complex electrical systems in a fast way, with a high accuracy. Such approach is based on neural networks and SPICE B-model and allows to capture the system temperature dependent electrical behavior in an easy way in order to perform light-weight simulations. The methodology is coupled with the thermal approach shown in the previous chapter in order to developed non-linear thermal models.
In order to build the model, the test bench composed by 6 MOSFETs was used, which allows to validate the proposed methodology and to extract the necessary data for the model. Therefore, for each MOSFET it was extracted, the I_D/V_{DS} characteristic for each considered V_{GS} and T.

6.1 Overview on electro-thermal simulation

An electro-thermal model is a model able to simulate consistently the thermal behavior and the electrical behavior of a system. In particular, the electrical model is constrained by thermal model and the thermal model is constrained by the electrical model. Such kind of simulations are clearly expensive in term of computational effort and good accuracy is difficult to obtain. Moreover, the presence of thermal non-linearities, due to material properties and natural air convection, are difficult to model.
Other difficulties, such as capturing the thermal behavior in a proper way, are linked to the presence of multiple heat-sources. This kind of system is not analyzed in the chapter, but it is easily developable through the proposed methodology.
In literature, different strategies are proposed to accomplish the study of the electro-thermal behavior of a MOSFETs based system (or, more in general, an electronic system), in order to obtain lightweight and accurate simulations:

1. SPICE models;
2. mixed models.

In both strategies the main concept of electro-thermal simulation could be summed up by Figure 6.1.

6.1.1 SPICE models

In this case, the manifacture provides SPICE models able to simulate the thermal behavior of the system. In particular, the SPICE model is built through the complete knowledge of the device and provides the thermal network between the die and the package.
The typical MOSFET SPICE model is provided with 3 connectors, while the enhanced thermal MOSFET SPICE models are provided with 4 or 5 connectors. For instance, Infineon enhanced thermal model has 5 pins, 3 of them are Drain, Source and Gate while the other 2 are for the thermal behavior. In particular, the first one allows to connect a thermal network that could represent the heat sink to ambient

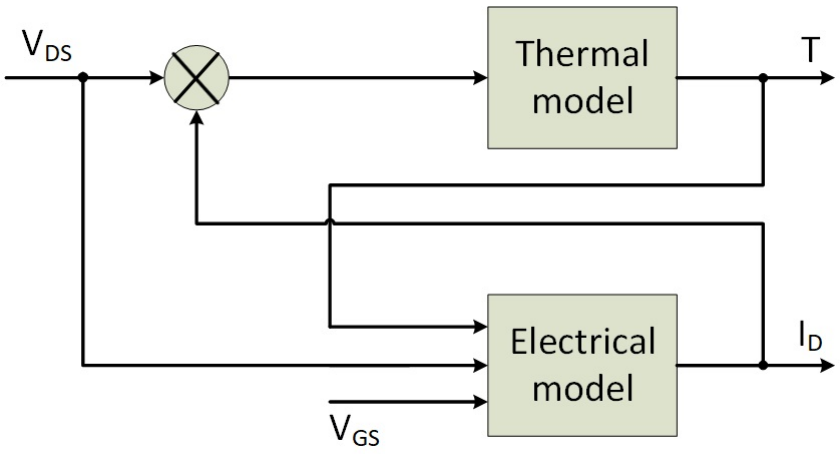

Figure 6.1: Scheme of electro-thermal simulation of a MOSFET.

thermal path and, the second one is an output pin providing the junction temperature, as shown in Figure 6.2 [151]. This kind of approach is really useful but the drawbacks are linked to the necessity of knowing the internal structure, and to the lower adaptability to a real system.

6.1.2 Mixed models

In this case only part of the simulation is run by SPICE, the other is provided through another simulation system. An example could be provided by electro-thermal studies in which the electrical part is simulated through SPICE, while the thermal part is implemented through FEM simulator. This kind of simulation could be extremely accurate but the main issue is to get a synchronization between simulators, that allows the study to converge.
On the other hand, also simulations which do not use SPICE, but implement a convergence strategy, could be considered as Mixed Models. A clear example is the FEM simulation for both the thermal and electrical behavior, but the two models are used separately and a routine allows to manage the convergence and reach the solution. Differing from the enhanced thermal SPICE model, this kind of approach is able to

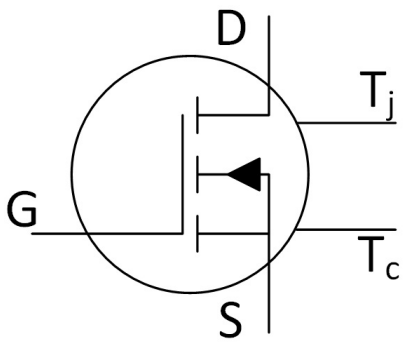

Figure 6.2: Infineon 5 pins MOSFET model; in addition to Drain, Source and Gate, there are 2 pins for T_j and T_c: the first one is an output pin while the second one allows to connect a thermal network.

model also thermal behaviors affected by non-linearities.
Mixed Models are used in [102] and [120].

6.2 LUT approach discussion

As already shown in [147] Look-Up-Tables (LUTs) are a SPICE powerful tool that expands the expressivity of SPICE language. LUTs allow to describe behavioral models in an easy way, and it is possible to model the thermal-behavior of a device affected by non-linearities. To describe the electrical model of a real system without knowledge of electrical details, LUTs could be a solution:

1. the thermal model is already represented by LUTs;
2. electrical model coupled with the thermal model could be represented also with LUTs.

Generally, to represent the electrical behavior of a MOSFET without thermal constraints, it is possible to use a LUT with just one level of nested tables. To allow the electrical model to be useful in an electro-thermal simulation, it is necessary to

develop a LUT with a two-levels nested table. In particular, the LUT describing the electrical model needs three inputs: V_{GS}, V_{DS} and T.
Clearly, the output of the LUT is the MOSFET current I_D. In SPICE, the implementation of the device electrical behavior is done through the use of B-Models.
Unfortunately, this approach is not useful in electro-thermal modeling, in fact it is complex to solve and LTSPICE is not always able to compute non-stationary simulations.
This kind of model can be considered as valid in the following conditions:

1. stationary electrical simulations;
2. non-stationary electrical simulations;
3. stationary electro-thermal simulations.

6.3 Feed-forward neural network

An Artificial Neural Network (ANN) is a computational tool introduced in the middle of the 50s. Nowadays, thanks to the work of Minsky and Papert [152], it is considered one the most important tools in Artificial Intelligence (AI) and in Machine Learning (ML). ANNs were inspired by brain modeling studies [153] [154] and they demonstrated good efficiency and ability to solve complex problems.
ANNs aim at implementing systems that reproduce the neural human behavior and are used in many fields with good results:

- robotics;
- classification;
- data processing;
- control;
- function approximation.

Different implementations are suggested in literature and they provide different features adapt to solve different problems [153]. In this specific case, that is to reproduce the MOSFET behavior, the ANN selected is the Multi-Layer Perceptron (MLP). In fact, such kind of ANN is able to approximate functions and for instance to reproduce the electrical characteristic of a MOSFET from measurements. MLP is afferent to Feed-Forward Neural Networks (FFNN), that are ANNs in which the connections do not form a close circuit. MLP is characterized by more than two layers. As a matter of fact, it provides at least one hidden layer. MLPs are efficient and effective in order to approximate a function: in fact, for the universal approximation theorem [155][156][153], the MOSFET electrical characteristic could be approximated by an MLP.

6.3.1 Artificial neuron

The main element of an ANN is the Artificial Neuron (AN) [153] [154] which allows to map a non-linear relationship between a value from $\mathscr{R}^{N-1}$ to $[0,1]$ (sometimes $[-1,1]$):

$$f_{AN} : \mathscr{R}^{N-1} \rightarrow [0,1] \tag{6.1}$$

where N is the number of AN input signals defined as:

$$x = [x_0, x_1, ..., x_{N-1}] \tag{6.2}$$

In Figure 6.3 the AN is graphically defined, and each input x_i could be an input derived from the enviroment or from another AN. To the input vector is associated the weight vector:

$$w = [w_0, w_1, ..., w_{N-1}] \tag{6.3}$$

The complete AN input is computed through:

$$I = \sum_{i=0}^{N-1} (x_i w_i) \tag{6.4}$$

To obtain the AN output is necessary to apply an activation function to the complete input $f_{AN}(I)$. Generally the activation function is the function sigmoid ($\mathrm{sig}(I)$), but it

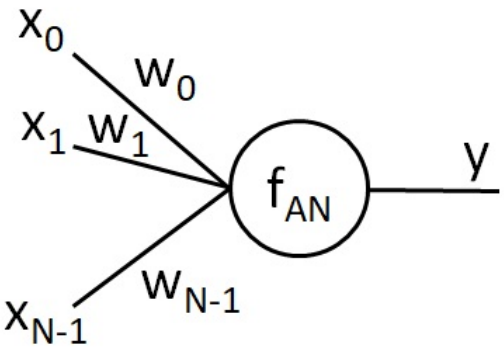

Figure 6.3: Artificial neuron graphical definition.

could be substituted by other activation functions like $\arctan(I)$. The sigmoid function is defined as:

$$\text{sig}(I) = \frac{1}{1+\exp(-I)} \tag{6.5}$$

For completeness, Figure 6.4 shows the sigmoid function. Finally, the output y of the AN is obtained by:

$$y = f_{AN}(I) = \text{sig}(\sum_{i=0}^{N-1}(x_i w_i)) \tag{6.6}$$

6.3.2 Multi-layer perceptron

An MLP is composed by several nodes in different layers. Each node of a layer is fully connected to other nodes of the following layer. For example, the MLP presented in Figure 6.5 is composed by 3 layers with 2, 3 and 1 node for each layer. The first layer is called "input layer", while the last layer is the "output layer". Every layer between the input layer and the output layer is called "hidden layer". In Figure 6.5, x_0 and x_1 are the network inputs, while y_0 is the output. For these nodes are valid (6.7), (6.8) and (6.9). The use of symbol $'$ identifies the application of the function sigmoid (if necessary).

$$x_0 = i'_0 = i_0 \tag{6.7}$$

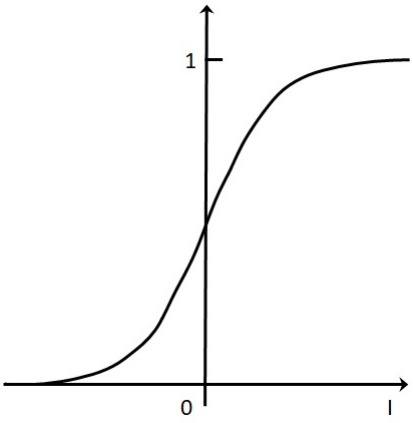

Figure 6.4: Sigmoid function sig(I).

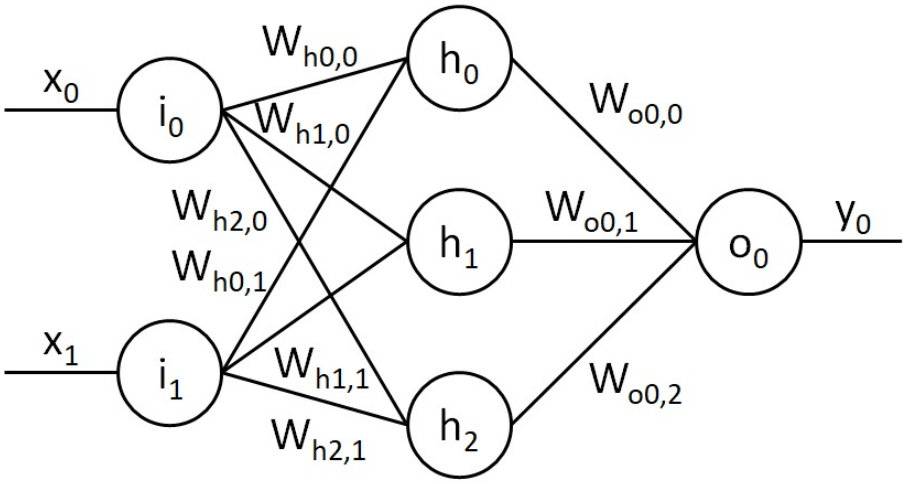

Figure 6.5: MLP composed by three layers and 6 nodes.

$$x_1 = i'_1 = i_1 \tag{6.8}$$

$$y_0 = o'_0 = \text{sig}(o_0) \tag{6.9}$$

To calculate the first node of the hidden layer, it is important to follow the two expressions, (6.10) and (6.11), where N_i is the number of input nodes and $w_{h0,k}$ are the weights:

$$h_0 = \sum_{k=0}^{N_i-1} (w_{h0,k} \cdot i'_k) \tag{6.10}$$

$$h'_0 = \text{sig}(h_0) \tag{6.11}$$

For the other two nodes of the hidden layer the expressions (6.12), (6.13), (6.14) and (6.15) are valid:

$$h_1 = \sum_{k=0}^{N_i-1} (w_{h1,k} \cdot i'_k) \tag{6.12}$$

$$h'_1 = \text{sig}(h_1) \tag{6.13}$$

$$h_2 = \sum_{k=0}^{N_i-1} (w_{h2,k} \cdot i'_k) \tag{6.14}$$

$$h'_2 = \text{sig}(h_2) \tag{6.15}$$

Finally, for the output node subsists the equation (6.16).

$$o_o = \sum_{j=0}^{N_h-1} (w_{o0,j} \cdot h'_j) \tag{6.16}$$

In general, the output of the MLP of Figure 6.5 could be written in the compact form given by (6.17):

$$y_o = \text{sig}(\sum_{j=0}^{N_h-1} (w_{o0,j} \cdot \text{sig}(\sum_{k=0}^{N_i-1} (w_{hj,k} \cdot i_k)))) \tag{6.17}$$

6.3.3 MLP learning

To determine the weights, it is necessary to do the training of the MLP. In fact, without the training the network is not able to reproduce the behavior of the function to be approximated. In the suggested case, the supervised learning is possible, in fact

output associated with the input is available and it forms the training set. The aim of supervised training is to adjust the weight values in order to minimize the error between the network output and the training set output.
The training could be made in different ways, although a good method useful to represent an electrical MOSFET behavior is to use the strategy of backpropagation. With reference of Figure 6.5 a training set is a set of N_m row composed by two input and one output.
During the training, the training set is submitted to MLP in order to calculate the weights and obtains a trained MLP. The operation to submit the training set to the MLP is done until the total net error is equal to 0 or under a defined value. For each row m of the training set and for each output of net, the error is calculated, or rather the difference between the desired value and the output of the node:

$$e_0(m) = (\hat{y}_0(m) - y_0(m)) \tag{6.18}$$

while the total error is calculated as:

$$E(m) = \frac{1}{2} \sum_{u=0}^{N_o-1} e_u(m) \tag{6.19}$$

In the case of the example in Fig. 4.1, (4.14) became:

$$E(m) = \frac{1}{2} e_0(m) \tag{6.20}$$

Finally, each weight is updated in accordance with the error and the learning rate l (generally with the gradient). l is the learning rate that could be chosen: it should not be too large in order to avoid false training, and not too small, in order to reduce the training time.

6.3.4 Use of bias

Sometimes, in order to solve the problem, it is necessary to insert bias neurons. This kind of neurons in some circumstances is mandatory in order to obtain correct results. In other cases, the use of bias neurons allows to obtain better results. Bias neurons are neurons without input, with value 1 and a weight associated (as other AN). The

ANN of Figure 6.5 with bias neurons is shown by Figure 6.6. A detailed dissertation about the use of bias is given by [157]. Finally the complete AN input and output become:

$$I = \sum_{i=0}^{N-1} (x_i w_i) + 1 \cdot w_b \tag{6.21}$$

$$y = f_{AN}(I) = \text{sig}(\sum_{i=0}^{N-1} (x_i w_i) + 1 \cdot w_b) \tag{6.22}$$

where w_b is the weight associated to the bias.

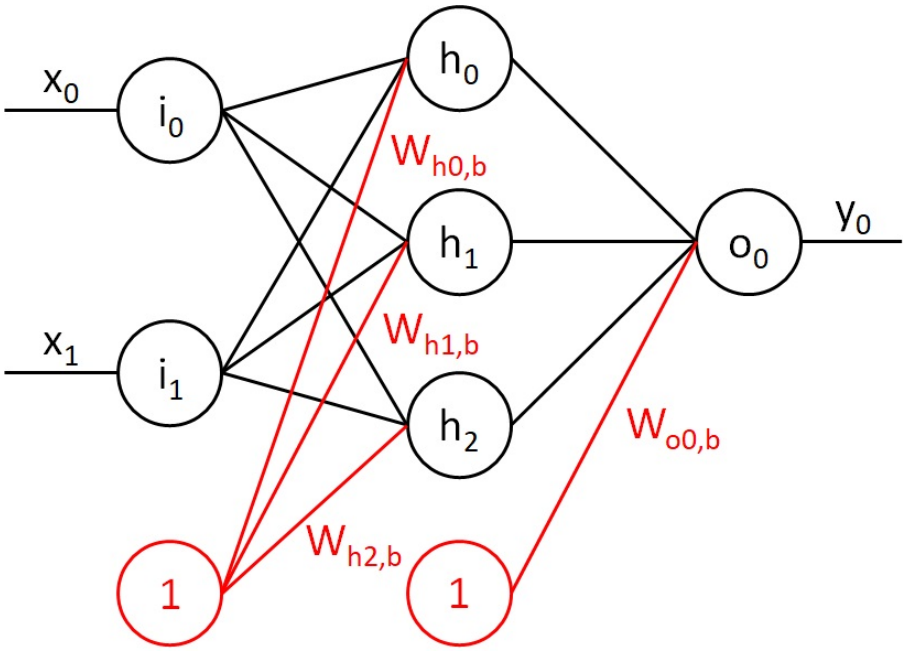

Figure 6.6: MLP composed by three layer, 6 AN and 2 bias.

6.4 Electrical characterization

In order to develop a model of a real system, it is necessary to perform an electrical characterization of the system. In the case proposed, it was developed a model of

only a part of the whole system. The system object of the study is shown in Figure 6.7 and it is composed by 6 MOSFETs in 3 SO-8 package. It was created in order to do a thermal characterization but it was also used for the electrical characterization of MOSFETs M_3. To characterize M_3, an Angelantoni-ACS Discovery climatic chamber and modular DC source/monitor unit HP 4142B were used. The block diagram

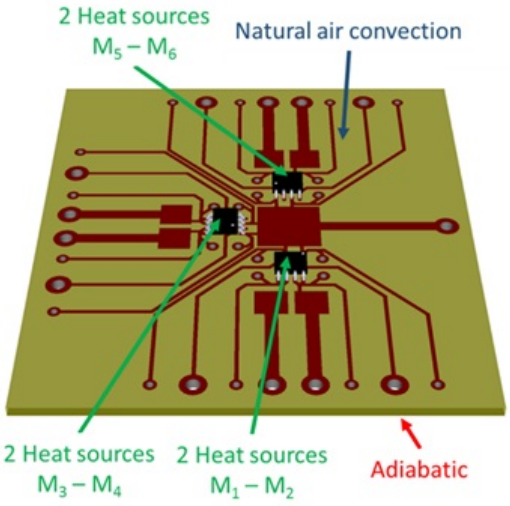

Figure 6.7: Real system used to develop an electrical model, composed by 6 MOSFETs in 3 SO-8 package. The MOSFETs share the source-ground connection.

of the test bench is shown in Figure 6.8. Two thermocouples are used to monitor the climatic chamber temperature: one was put near the Device Under Test (DUT) while the second one was put near the climatic chamber temperature sensor. The HP4142B was controlled through an ad-hoc HP VEE program. The logic of the HP VEE program is shown in Algorithm 6.1. Every cycle of the VEE program (representing a temperature of the climatic chamber), V_{GS} is fixed, selected in the range $0 \div 3$ V, and V_{DS} is sweeped from 0 to 3 V with measurements of I_D. Although V_{DS} sweep could be done in an automatic way through the HP4142B, it was done through software, in order to increase the waiting time between measurement pulses and to reduce the self-heating due to them.

In Figure 6.9, is shown the DUT in the climatic chamber, while the ranges of mea-

Algorithm 6.1 The logic of the HP VEE program

```
For (T=20;T<=140;T=T+20)
{
   For(VGS=0.0;VGS<=3;VGS=VGS+0.05)
   {
        For(VDS=0.0;VDS<=3;VDS=VDS+0.05)
        {
           ID=MeasureID(VGS,VDS);
           wait();
        }
   }
}
```

surements are presented in Table 6.1.

	T [C]	**V_{GS} [V]**	**V_{DS} [V]**
Range	20÷120	0÷3	0÷3
Step	20	0.05	0.05

Table 6.1: Ranges and steps used for the characterization.

6.4.1 Characterization details

The characterized DUT is a Dual SO-8 MOSFET. The obtained results at different temperatures are shown in Figure 6.10, Figure 6.11, Figure 6.12, Figure 6.13, Figure 6.14 and Figure 6.15 for devices M_3. It is important to remember that the configuration used with HP4142B does not allow to measure drain current larger than 10 A. In the cases in which current over than 10 A would required, the HP4142B limits the

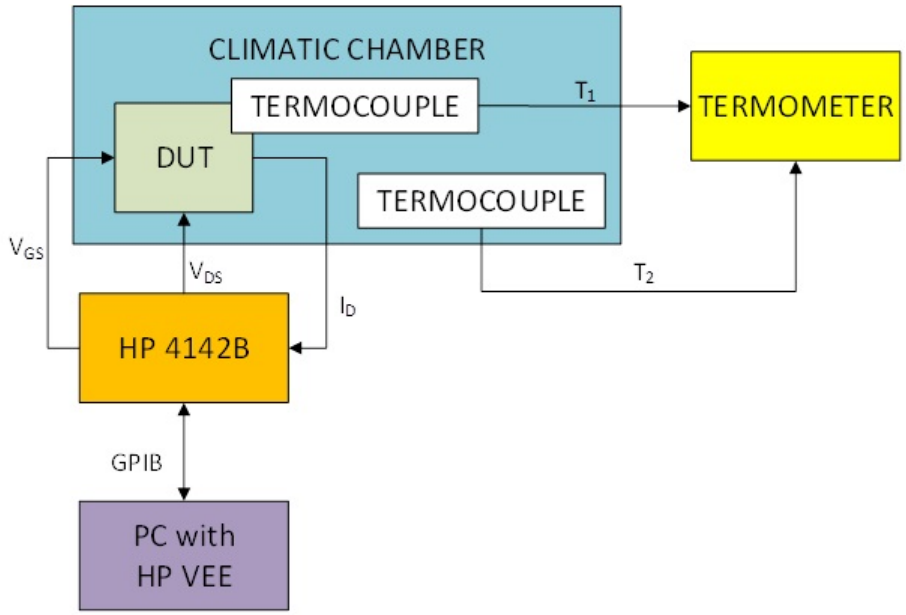

Figure 6.8: Block diagram of the test bench used to characterize MOSFET M_3.

Figure 6.9: DUT in the climatic chamber.

value of the current. In Table 6.2 are shown the maximum value of the current I_D with V_{GS} of 1.75 V (at V_{DS}=3.0 V) and the maximum value of V_{GS} where the current could be considered equal to 0 (this parameter is important in order to use an appropriate training set and to keep a light training file).

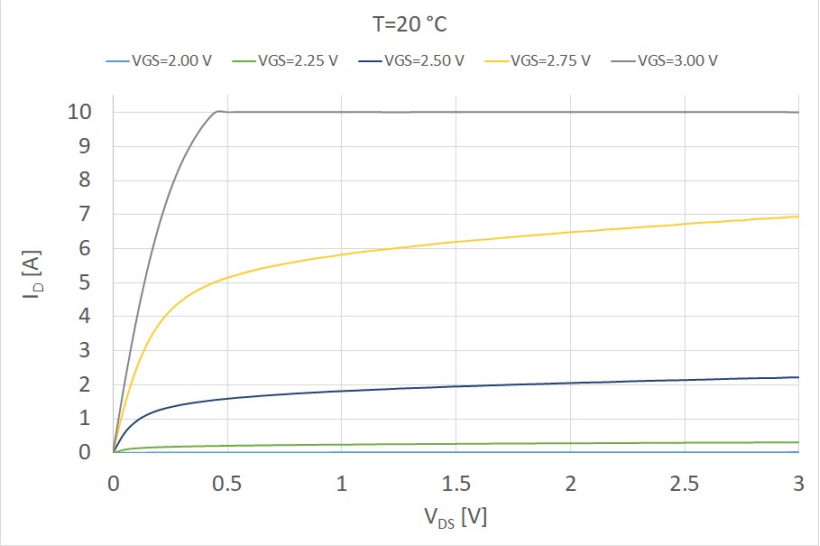

Figure 6.10: M_3 drain characteristic with $T = 20$ °C and V_{GS} =2.00, 2.25, 2.50, 2.75 and 3.00 V.

6.5 Neural network electrical model

In order to implement the necessary ANN to reproduce the electrical behavior of a MOSFET, it was used Neuroph [158]. Neuroph is Java Library that could be used to develop software, but it also provides a GUI that allows to implement an ANN in an easy way. The use of Neuroph permits to train the ANN without implementing an ad-hoc algorithm, in fact the weights extraction could be done directly from Neuroph GUI. A MOSFET model implementation through neural network was already proposed by [159] but temperature was not considered. For each MOSFET, an MLP could be implemented, which represent the electrical characteristic of each device. In

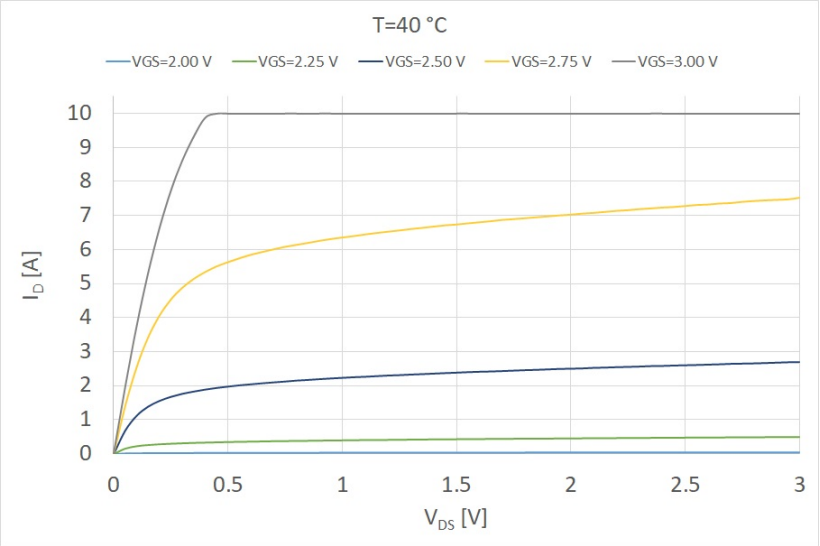

Figure 6.11: M_3 drain characteristic with $T = 40$ °C and V_{GS} =2.00, 2.25, 2.50, 2.75 and 3.00 V.

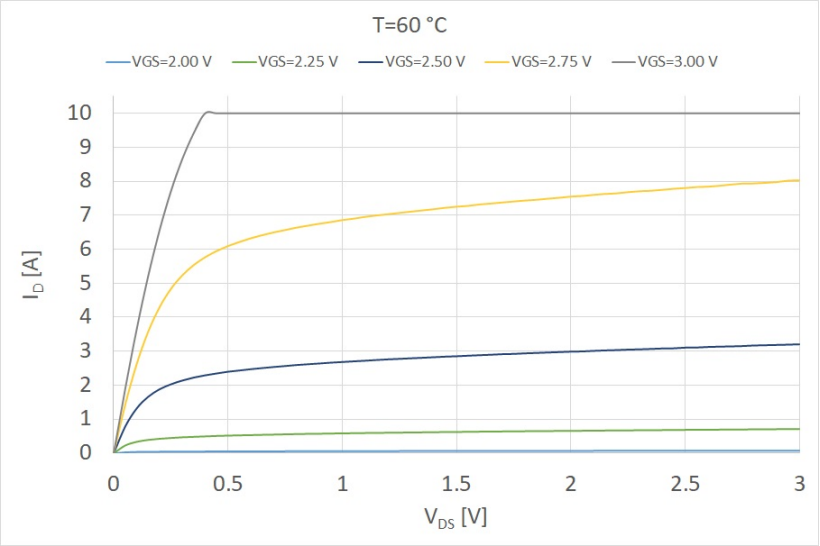

Figure 6.12: M_3 drain characteristic with $T = 60$ °C and V_{GS} =2.00, 2.25, 2.50, 2.75 and 3.00 V.

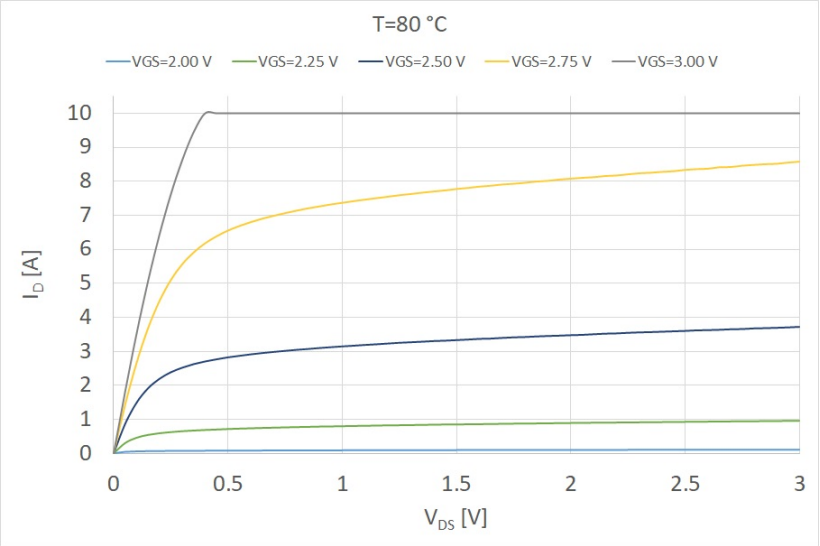

Figure 6.13: M_3 drain characteristic with $T = 80$ °C and V_{GS} =2.00, 2.25, 2.50, 2.75 and 3.00 V.

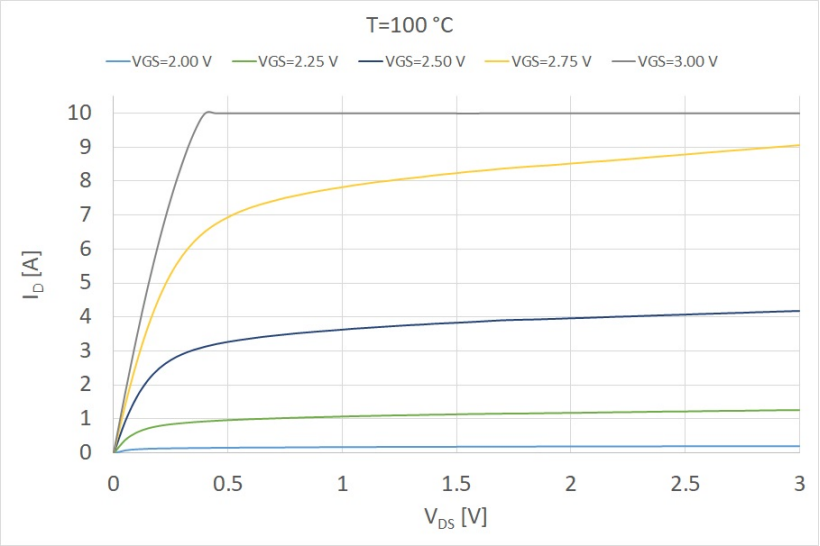

Figure 6.14: M_3 drain characteristic with $T = 100$ °C and V_{GS} =2.00, 2.25, 2.50, 2.75 and 3.00 V.

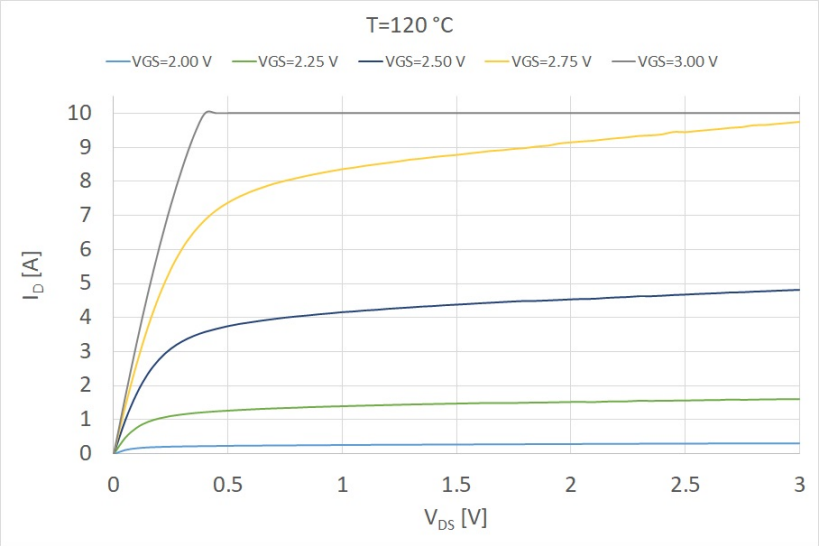

Figure 6.15: M_3 drain characteristic with $T = 120$ °C and V_{GS} =2.00, 2.25, 2.50, 2.75 and 3.00 V.

T [°C]	**I_D [mA] ($V_{GS} = 1.75$ V and $V_{DS} = 1.75$ V)**	**max V_{GS} [V] ($I_D = 0$)**
20	0.2	1.70
40	1.2	1.65
60	3.0	1.60
80	7.4	1.55
100	16.0	1.50
120	32.8	1.45

Table 6.2: Drain current I_D at V_{GS}=1.75 and V_{DS}=3.0 V and V_{GS} limit value to $I_D = 0$.

particular, an MLP for M_3 was implemented. For the sake of simplicity, it was used the same structure represented by Figure 6.16 and Table 6.3, Table 6.4, Table 6.5, Table 6.6, Table 6.7, Table 6.8, Table 6.9, Table 6.10, Table 6.11 and Table 6.12 (3 layer with 3+bias, 9+bias and 1 nodes). Each of the three input parameters before to enter the MLP are normalized in the range $[0,1]$, while the output is denormalized. AN i_3 and h_9 are bias neurons.
The MLP was trained with a specific training set developed from measurements. The MLP could represent any MOSFET, but in this work is built for M_3 and with the following set of parameters:

- $V_{GS} = 0 \div 2.5$ V
- $V_{DS} = 0 \div 3$ V
- $T = 0 \div 130$ °C
- $I_D = 0 \div 7$ A

ANN input is compatible with the above ranges, but not-limited. The possibility to represent an MLP as a single function allows to insert it in a SPICE B-Model. This is quite simple and also easier than implementing a LUT with three inputs. In fact the B-Model current output is implemented by equation (6.17) with normalized input (V_{GS},V_{DS},T) and output (I_D).

Input node/Output Node	**Weight**
i_0/h_0	-1.18039
i_1/h_0	-0.56398
i_2/h_0	-16.526
i_3/h_0	21.17943

Table 6.3: MLP structure for M_3 from input layer to node h_0.

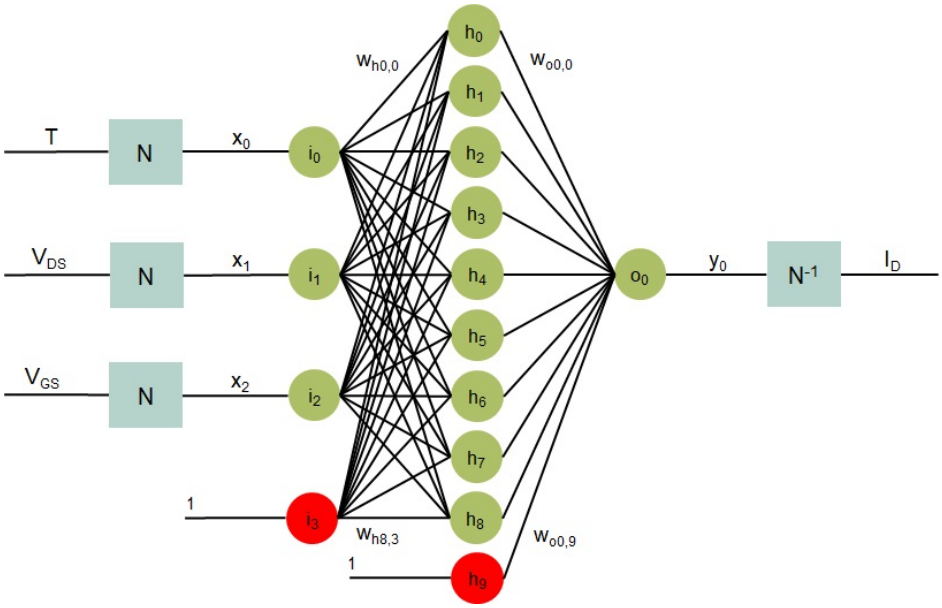

Figure 6.16: M_3 MLP electrical model.

Input node/Output Node	**Weight**
i_0/h_1	-1.25184
i_1/h_1	-0.09108
i_2/h_1	-8.7805
i_3/h_1	6.7477

Table 6.4: MLP structure for M_3 from input layer to node h_1.

Input node/Output Node	**Weight**
i_0/h_2	3.37067
i_1/h_2	-0.53338
i_2/h_2	3.88376
i_3/h_2	-3.98023

Table 6.5: MLP structure for M_3 from input layer to node h_2.

Input node/Output Node	Weight
i_0/h_3	-1.19729
i_1/h_3	29.46461
i_2/h_3	-10.7843
i_3/h_3	12.64196

Table 6.6: MLP structure for M_3 from input layer to node h_3.

Input node/Output Node	Weight
i_0/h_4	0.02396
i_1/h_4	143.1661
i_2/h_4	1.51414
i_3/h_4	0.87713

Table 6.7: MLP structure for M_3 from input layer to node h_4.

Input node/Output Node	Weight
i_0/h_5	0.2517
i_1/h_5	-4.25366
i_2/h_5	2.85541
i_3/h_5	-4.84383

Table 6.8: MLP structure for M_3 from input layer to node h_5.

Input node/Output Node	Weight
i_0/h_6	1.52339
i_1/h_6	-0.34706
i_2/h_6	-4.14328
i_3/h_6	3.93059

Table 6.9: MLP structure for M_3 from input layer to node h_6.

Input node/Output Node	Weight
i_0/h_7	-9.87704
i_1/h_7	-0.94608
i_2/h_7	-8.5032
i_3/h_7	22.90183

Table 6.10: MLP structure for M_3 from input layer to node h_7.

Input node/Output Node	Weight
i_0/h_8	-4.07722
i_1/h_8	1.45522
i_2/h_8	-11.6515
i_3/h_8	14.52395

Table 6.11: MLP structure for M_3 from input layer to node h_8.

Input node/Output Node	Weight
h_0/o_0	-16.9395
h_1/o_0	-12.468
h_2/o_0	2.45091
h_3/o_0	6.36518
h_4/o_0	38.06775
h_5/o_0	-4.01075
h_6/o_0	-4.40523
h_7/o_0	-15.056
h_8/o_0	-1.03847
h_9/o_0	-10.7037

Table 6.12: MLP structure for M_3 from hidden layer to node o_0.

6.5.1 Validation

In order to validate the MLP, a comparison between measurements used to build the MLP model and simulation based on the proposed approach is evaluated. The results are good and demonstrated a good agreement between simulations and measurements. The most useful results (chosen in an operative meaningful range of temperature and voltages) are shown in Figure 6.17, Figure 6.18, Figure 6.19 and Figure 6.20.

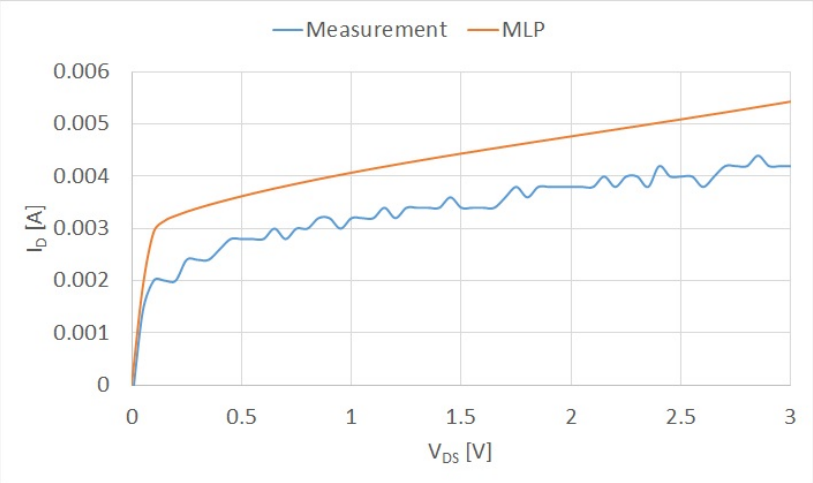

Figure 6.17: Comparison between measurement and MLP simulation of MOSFET M_3, $T = 20$ °C and $V_{GS} = 1.9$ V.

6.6 Electro-thermal model

By coupling the electric model with the thermal model, it is possible to obtain an overall electro-thermal one. Such a model has been completely built from a real system. As a matter of fact, the advantage of the methodology suggested is the capability to produce extremely accurate models, even without knowing (or partially knowing) the structure of the device. As a result, electro-thermal models can be obtained and

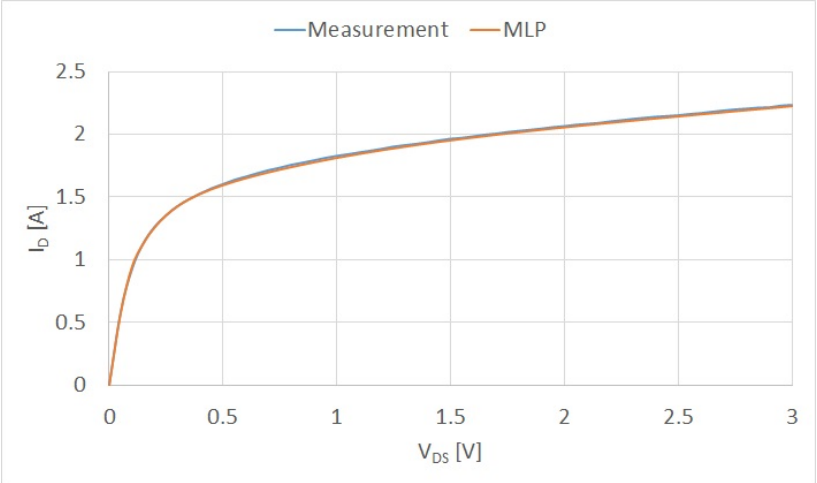

Figure 6.18: Comparison between measurement and MLP simulation of MOSFET M_3, $T = 20$ °C and $V_{GS} = 2.5$ V.

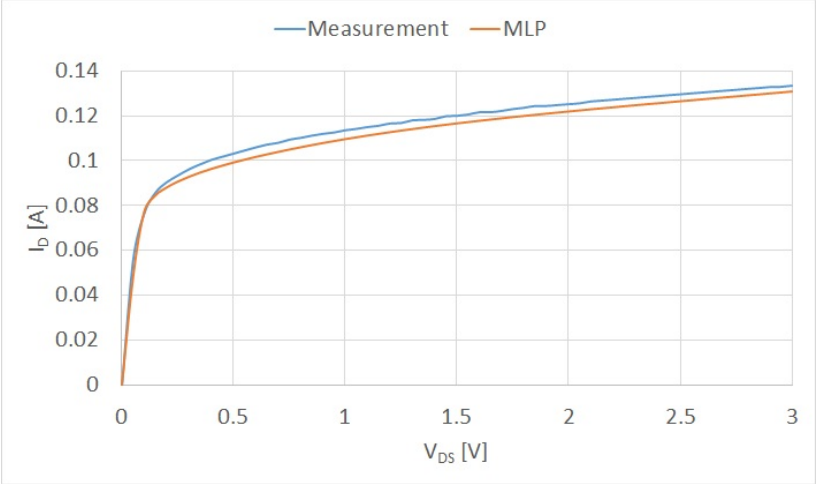

Figure 6.19: Comparison between measurement and MLP simulation of MOSFET M_3, $T = 120$ °C and $V_{GS} = 1.9$ V.

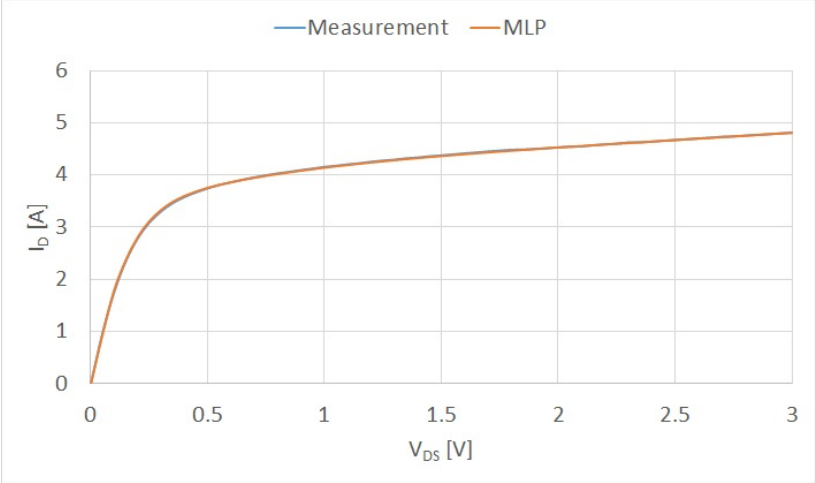

Figure 6.20: Comparison between measurement and MLP simulation of MOSFET M_3, $T = 120$ °C and $V_{GS} = 2.5$ V.

can be directly simulated through SPICE, without the help of FEM tools.
The electro-thermal model proposed is composed by:

1. an MLP network that allows to simulate the electrical behavior;
2. a non-linear Foster network that allows to simulate the thermal behavior.

The non-linear Foster network is built with the procedure previously presented. Both models are based on the use of SPICE B-Model. For the sake of clarity, LT-SPICE provides three B-MODEL:

1. R implements a variable resistance;
2. I is a current source with an arbitrary function;
3. V is a voltage source with an arbitrary function.

The real system used to validate the approach has a resistance $R_D = 4.7\ \Omega$ connected to drain MOSFET pins. In addition to the resistance R_D, it is necessary to consider the resistance R_S, due to the copper traces and solder joints. In fact, R_S is generally

negligible but in voltage conditions used to extract the model, it is not neglibible, or rather it could considerably influence the value of V_{GS}.
The entire system is presented in Figure 6.21. To calculate the value of R_S is simple and from measurements it was found $R_S = 0.072\ \Omega$.
An example of the final electro-thermal model is presented in Figure 6.22.

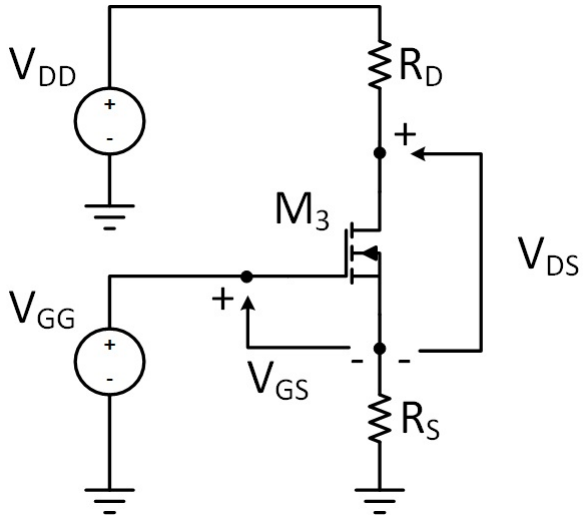

Figure 6.21: Schematic of the system composed by M_3, V_{GG}, V_{DD}, R_D and R_S. Such system is used for measurements.

6.6.1 Comparison with measurements and results

Test cases are developed in order to compare measurements with simulations. Measurements could be done only in stationary conditions while simulation are non-stationary. In addition, the chip temperature is extracted through FEM. In fact the proposed system is composed by commercial MOSFETs, parallely connected, but only M_3 is modeled. In each case, a couple of V_{GG} and V_{DD} (step signals) are submitted to the system and the time-dependent evaluation of T is observed. The evaluation of the error is done in stationary conditions on V_{DS}, I_D and T, through (6.23), (6.24)

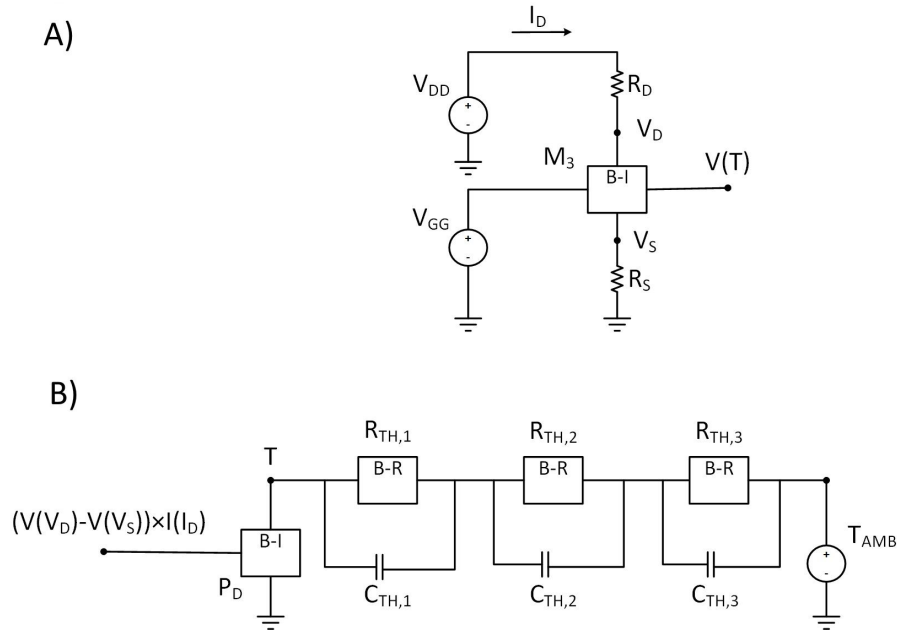

Figure 6.22: Electro-Thermal model with detailed implementation; in a) the MLP electrical model, in which M_3 is designed through a SPICE B-Model current source; in b) the non-linear Foster thermal model composed by 3 stages, with the use of a SPICE B-Model current source for P_D, while thermal variable resistances use SPICE B-Model resistance.

and (6.25):

$$|E_V\%| = \frac{|V_{DS,meas} - V_{DS,sim}|}{V_{DS,meas}} \cdot 100 \tag{6.23}$$

where $V_{DS,meas}$ is the measured voltage and $V_{DS,sim}$ is the simulated voltage,

$$|E_I\%| = \frac{|I_{D,meas} - I_{D,sim}|}{I_{D,meas}} \cdot 100 \tag{6.24}$$

where $I_{D,meas}$ is the measured current and $I_{D,sim}$ is the simulated current,

$$|E_T\%| = \frac{|\Delta T_{FEM} - \Delta T_{sim}|}{\Delta T_{FEM}} \cdot 100 \tag{6.25}$$

where ΔT_{FEM} is the temperature increase obtained through FEM simulation and ΔT_{sim} is the simulated temperature increase.
Clearly for each case, with the increase of the temperature T, the current I_D rises, while the V_{DS} over the device decreases.
Simulations present good results (Figure 6.23, Figure 6.24 and Figure 6.25) and each error is always below or near 10% (in the case studies proposed) as shown in Table 6.13.

$\mathbf{V_{DD}}$ [V]	$\mathbf{V_{GG}}$ [V]	$\lvert\mathbf{E_V}\%\rvert$	$\lvert\mathbf{E_I}\%\rvert$	$\lvert\mathbf{E_T}\%\rvert$
4.00	2.15	5.2	2.1	2.5
3.00	2.15	2.8	2.0	0.2
2.00	2.15	2.4	2.8	1.4
4.00	2.30	8.0	1.2	4.8
3.00	2.30	7.8	1.3	4.5
2.00	2.30	8.2	1.1	4.5
4.00	2.45	6.9	0.2	3.9
3.00	2.45	1.4	0.0	2.1
2.00	2.45	10.4	0.2	8.3

Table 6.13: Error evaluation between measurements and simulations.

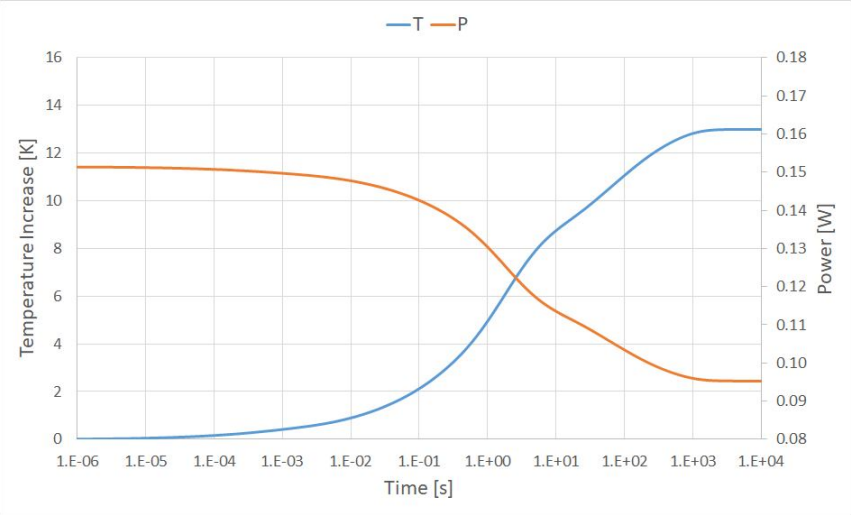

Figure 6.23: Simulation of the system with MOSFET M_3 in ON-state and $V_{GG} = 2.30$ V and $V_{DD} = 2.00$ V.

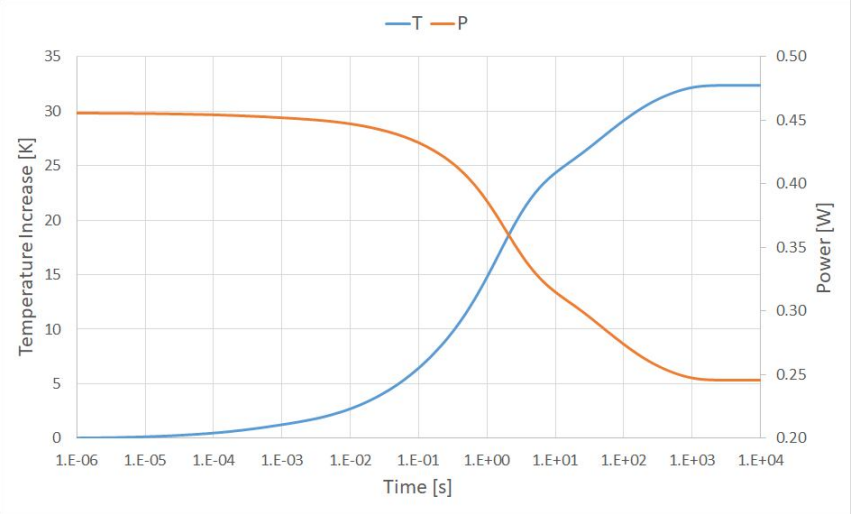

Figure 6.24: Simulation of the system with MOSFET M_3 in ON-state and $V_{GG} = 2.30$ V and $V_{DD} = 3.00$ V.

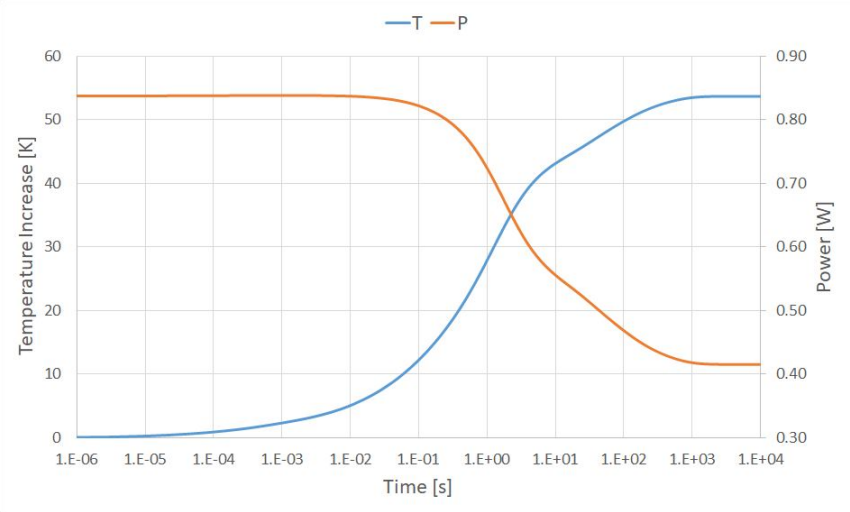

Figure 6.25: Simulation of the system with MOSFET M_3 in ON-state and $V_{GG} = 2.30$ V and $V_{DD} = 4.00$ V.

6.7 Results Discussion

The approach proposed has shown good results. The model developed through MLP demonstrated a good agreement with measurements and it can provide a valid alternative to more complex models. In fact, the use of an MLP allows an easy SPICE implementation. On the other hand, a behavioral model based on this approach could represent the behavior of a large variety of electronic devices.

Through the methodology presented in the previous chapter, a non-linear thermal network has been created; the target is to develop a consistent electro-thermal model. Tests have been developed that could demonstrate the electro-thermal effectiveness, so that the results of the simulations could be validated.

To conclude, this chapter has presented a methodological approach for the development of NN-based models. Even if this process does not insert completely new elements, it supplies an extremely new approach to electro-thermal models. In fact, no work combining the use of neural networks and thermal networks is present in literature; moreover, non-linear thermal networks identification allows to obtain models

which are extremely simple to simulate, as it was demonstrated. It is worth considering that the time-variant electro-thermal simulation realized through the suggested methodology requires few seconds; concerning this, it is necessary to remember that FEM simulations of the same system in thermal physics under non-stationary thermal conditions require several hours.

Chapter 7

Conclusions

I am not now, nor have I ever been,
a member of the demigodic party.

– Dennis MacAlistair Ritchie

The main object of this work has been to provide computational light-weight simulation methodologies in order to allow the study of complex power electronic systems for industrial and automotive applications. In fact, such systems present different reliability challenges, and one of them is linked to the thermal behavior. This work proposes novel simulation methodologies, which have the aim to be an alternative to FEM simulations and to be an easy and reliable tool during device design phases.
First of all, a review on power electronic systems employed in automotive industry and power MOSFET modeling has been done; after that, an overview on the study of simulations reliability has been made.
Thermal modeling state of the art has been exposed by suggesting a systemic approach to the construction of FE and LE models.
Finally, three innovative methodologies have been proposed, which allow the development of fast simulation models:

- the first one is given by the fusion of FEM and LEM for thermal simulations;

- the second one is a non-linear multi-source heat model based on LEM for thermal simulations;

- the third one is a non-linear LEM-based model for electro-thermal simulations.

The first introductive chapter of the thesis was addressed to contextualize the role of power electronic systems in the automotive field and to provide a basic knowledge about power electronics and reliability. It was explored, on one hand, the main use of power MOSFETs, and on the other hand the state of the art about SPICE power MOSFETs models.
The second introductive chapter explains the concepts about thermal modeling of power devices. In fact, besides to provide an overview about the literature on thermal modeling, it explains the FEM process in order to develop thermal simulations (stationary and non-stationary conditions) and thermal networks extraction and analysis. As already mentioned, this work provides three original novel methodologies.
The first methodology is focused on power device thermal behavior and it allows to take into account the effects of the PCB and the environment in FEM simulations with a great DoFs reduction. The reduction of DoFs is done through the use of LEM based strategy. In fact, the unnecessary part of the model (PCB) is modeled through LEM, while the model part of interest (device with pins) is kept unchanged in FEM studies. On the other hand, the unnecessary part cannot be eliminated as such important on the complete system behavior. The proposed procedure extracts the Foster thermal network of the system portion between the pin and the environment, by removing the less significant system parts. The Foster network is converted in a Cauer network and, after that, in a 3D geometry composed by fictitious material, and inserted in the FEM model. The main advantage of the described procedure is the capability to simplify FEM model (with computational advantages) without loosing details on the part of interest. The built model is useful in long pulses and short pulses simulations and to compute electro-thermal and thermo-mechanical simulations.
The non-linear multi-source thermal model is built through another LEM based procedure in order to extract the necessary Foster newtorks. In this second procedure the FEM is used only to generate data and partially used to validate the approach. The

model developed via an ad-hoc procedure is based on multi-variable systems theory and it has the advantage to reproduce the thermal behavior of a system composed by several heat sources and affected by non-linearities. Non-linearities in a power electronic system are generally due to material thermal properties and natural air-convection; in such systems, the thermal conductance or the convective coefficient are non-linearly temperature dependent. The model extracted with the proposed procedure is able to reproduce, with the help of a SPICE simulator, the thermal interactions between power devices in a complex system. Although the proposed procedure, unlike other literature LEM approaches that implement non-linearities, does not use variable thermal capacitances in the model, but only variable thermal resistances. This result is important in order to obtain non-stationary reliable SPICE simulations and it is a key element of the complete algorithm composed by two main steps: the first one dedicated to fit the thermal impedance, while the second one dedicated to extract all the thermal impedances at different power steps. The whole methodology is supported by measurements, in fact the FEM model used to extract data is validated by thermal characterization.

Finally, the last developed modeling method is based on ANN and it merges the non-linear thermal LEM with an electrical description based on MLP. In fact a real system is used to develope an electrical model with the use of AI. The electrical model obtained with the proposed procedure is extremely accurate and it has the advantage to reproduce the electrical characteristics of a device without a deep knowledge of the device structure. The MLP based electrical model is inserted in a SPICE behavioral model with the purpose to couple the electrical model with the non-linear thermal model. The result is an electro-thermal model fully coupled of a power device. The methodology could be easily extended to the case of multiple heat sources without difficulties but with a great computational advantage. Thus, the methodology is an alternative to simulations based on FEM, since it allows to obtain extremely accurate electro-thermal simulations in non-stationary conditions. The model extracted with the presented procedure was validated via measurements.

To conclude, all the methodologies presented could be completely automated, provide a fast computation alternative to FEM studies of power electronic systems, and

then can be easily used for a reliability conscious power system design.

Appendix A

List of publications

A1 D. Chiozzi, M.Bernardoni, P. Cova and N. Delmonte, "Efficient thermal FEM modeling - Compact boundary conditions for electro-thermal problems", PhD Performance Catalogue of Infineon Villach Innoday 2015, Villach, Austria, 05 May 2015, pp. 36-36.

A2 P. Cova, N. Delmonte and D. Chiozzi, "Numerical analysis and experimental tests for solder joints power cycling optimization", Microelectronics Reliability, vol. 55, no. 9-10, pp. 2036-2040, Aug.-Sep. 2015.

A3 D. Chiozzi, M. Bernardoni, N. Delmonte and P. Cova, "A simple 1-D finite elements approach to model the effect of PCB in electronic assemblies", Microelectronics Reliability, vol. 58, no. 1, pp. 126-132, 2016.

A4 D. Chiozzi, P. Cova and N. Delmonte, "Numerical and experimental optimization of solder joint power cycling parameters", Book of Abstracts of the 48th Annual meeting of Associazione Gruppo Italiano di Elettronica (GE), Brescia, Italy, 22-24 Jun. 2016, pp. 67-68.

A5 N. Delmonte, D. Chiozzi, M. Caselli, P. Cova, G. Chiorboli, A. M. Aliyu, A. Castellazzi and P. Laserre, "Development aspects of a modular integrated 1200V-35A SiC MOSFET bi-directional switch", Book of Abstracts of the 49th Annual Meeting of the Società Italiana di Elettronica (SIE), Palermo, Italy, 21-23 Jun. 2017, pp. 132-133.

A6 P. Cova, A. M. Aliyu, A. Castellazzi, D. Chiozzi, N. Delmonte, P. Lasserre and N. Pignoloni, "Thermal design and characterization of a modular integrated liquid cooled 1200V-35A SiC MOSFET bi-directional switch", Microelectronics Reliability, vol. 76–77, no. 1, pp. 277–281, 2017.

A7 M. Bernardoni, N. Delmonte, D. Chiozzi and P. Cova, "Non-linear thermal simulation at system level: compact modeling and experimental validation", submitted to Microelectronics Reliability.

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