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DC-DC POWER CONVERTERS FEATURING
WIDE-BANDGAP DEVICES

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Alla mia famiglia

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Introduction

Modern society is strongly dependent upon electrical appliances for all the aspects of people's life, from economy to transportation, communication and health care. In this scenario, reducing energy consumption is critical to meet the world's growing demand for energy, sustainably. Wide Band Gap (WBG) materials, such as Silicon Carbide (SiC) and Gallium Nitride (GaN), can play a crucial role to improve the efficiency in the generation-distribution-utilization cycle of the electric energy. This is because most of the generated electric energy is consumed after undergoing several transformations carried out by power electronic converters and the largest portion of the losses occurs in their semiconductor devices.

This thesis concerns the design of high-efficient DC-DC converters based on WBG power devices. The first objective of the presented work is the development of an isolated bidirectional converter for the distribution network of future electrical aircrafts. The second project belongs to the field of photovoltaic systems and aims to develop a three-port converter with multiple power elements interfacing capability.

The dissertation is organized as follows.

- **Chapter 1** provides a quick overview of the main wide-bandgap semiconductors and outlines their appealing features for power electronic applications.

- **Chapter 2** explains the working principle of the Dual-Active-Bridge (DAB) and the Triple-Active-Bridge (TAB) converters, by means of simplified equivalent models. This includes a control-oriented small-signal model, which allows for basic analytical investigations and facilitates both the elaboration of appro-

priate modulation strategies and their calibration. In the end, design considerations to achieve desirable zero-voltage-switching behavior are also presented.

- **Chapter 3** traces a brief outline of current work towards More Electric Aircraft (MEA) and details the SiC-based DAB converter that provides the interface between the high and low voltage buses in the proposed energy distribution network. Both the hardware and the firmware design of the power module are extensively discussed, including the synthesis of the controlling strategies into the FPGA. The major contributions regard the design and implementation of the feed-forward compensation, the soft-start procedure and the paralleling methods.

- **Chapter 4** covers the design of a single-phase TAB converter featuring GaN devices, as fundamental module of a novel architecture proposed for photovoltaic inverters. The scheme of the centralized energy management system, that handles the power flow between the solar input source, the user load, and the energy storage device, is presented. Finally, details of the hardware implementation are also described and the main building blocks of the 1kW converter prototype are built, according to Appendices B and C.

Chapter 1

Wide Band Gap (WBG) semiconductor devices

1.1 Introduction

Silicon (Si) is by far the most widely used semiconductor material for electronic power devices. However, wide bandgap materials exhibit superior electric characteristics compared to silicon and it is now worldwide accepted that a real breakthrough in power electronics mainly comes from WBG semiconductor devices [1].

At present, Silicon Carbide and Gallium Nitride are the most promising candidates to replace Si for power switching applications, due to their attractive performance such as high switching frequency, high blocking voltage and high operating temperature.

Some basic information about these materials will be given in this chapter. In

particular, it will be pointed out why their physical properties are of industrial interest for manufacturing power devices and how they can have a favorable impact in the power conversion market.

1.2   Wide Band Gap semiconductors

Wide-bandgap semiconductors in general refer to any semiconductor materials with a bonding energy of the atoms in the crystal much greater than conventional semiconductors such as Silicon and Gallium Arsenide (GaAs). They are typically compound semiconductors such as Gallium Nitride, Aluminum Gallium Nitride (AlGaN), Indium Gallium Nitride (InGaN), or Silicon Carbide. Specifically, 4H-SiC and 6H-SiC are the dominant polytypes in SiC research since large wafers can be made in these materials. These semiconductors usually have a bandgap greater than 3 electron volts, compared with 1.12 eV for Si and 1.43 eV for GaAs.

Table 1.1: Physical characteristics of Si and main wide bandgap semiconductors [2].

Property		Si	4H-SiC	6H-SiC	GaN	
Energy Bandgap	E_g	1.1	3.2	3.0	3.4	eV
Dielectric constant[1]	ε_r	11.9	10.1	9.66	9.0	
Electric Breakdown Field	E_c	300	2200	2500	3300	kV/cm
Electron Mobility	μ_n	1500	1000	500	1250	$cm^2/V \cdot s$
Hole Mobility	μ_h	600	115	101	850	$cm^2/V \cdot s$
Saturated Electron Drift Velocity	v_{sat}	1	2	2	2.2	$\times 10^7 cm/s$
Thermal Conductivity	λ	1.5	4.9	4.9	1.3	$W/cm \cdot K$

[1] $\varepsilon = \varepsilon_r \cdot \varepsilon_0$ where $\varepsilon_0 = 8.85 \times 10^{-12} F/m$

Among the others, GaN and SiC devices have gained a prominent status regarding base material availability and maturity of their technological processes, and today they offer the best trade-off between theoretical performance and commercial readiness level for utility applications. Their main properties are listed (with respect to silicon features) in Tab. 1.1.

A detailed analysis based on the measured peak electric field strength at avalanche breakdown was disclosed in [2]. The purpose of that investigation was to critically examine elemental and compound semiconductors (including emerging WBG materials) in terms of on-state resistance, power losses, heat conduction, and radiation hardness. Further comparisons about different semi-conducting materials were discussed in [3], which evaluated some commonly known figures of merit for a more immediate evaluation of the performance capabilities of these materials for high-power electronic applications. Those papers show that the above mentioned WBG materials could provide substantial improvements in the power-handling capability, heat conduction, thermal runaway problems, high-temperature, and high-frequency operations. These potential benefits at both device and system level in power electronic applications are outlined in the next sections.

1.3 Device performance

An ideal power semiconductor switch is expected to have zero conduction and switching losses, zero leakage current in off-state, infinite voltage blocking capability and zero power consumptions when the control signal is applied. Other desired characteristics include high switching speed, good thermal stability, and high-temperature operation capability. Even if these idealistic characteristics are unachievable, there is a growing need for semiconductor technologies to meet the requirements of advanced high-power and high-efficient electronic systems. The driving force for the use of WBG in that application is the potential benefit to realize low loss and very fast unipolar switches with blocking voltages up to several kV.

According to these considerations, the wide-bandgap inherent properties and the corresponding advantages as power device are sketched in Fig. 1.1.
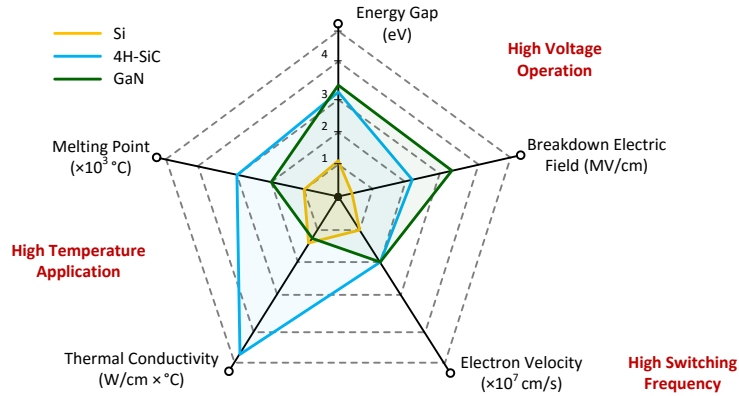
Figure 1.1: Radar chart of the main properties of semiconductor materials.

As it can be observed in Tab. 1.1 and Fig. 1.1, the wide band gap energy results in several compelling attributes for power electronics devices. The most remarkable characteristic is the higher critical electrical field (around 8 times higher than that of Si for SiC and 10 times higher for GaN), which brings to greater device breakdown voltage (for the same drift layer thickness). Otherwise, it means that the width of the drift region could be reduced for the same breakdown voltage, resulting in thinner devices at the same voltage rating. With a higher electric breakdown field, more doping can also be applied to the material, further increasing the maximum electrical field and reducing the depletion area. Moreover, the on-resistance of the drift region is lower since the conductance per unit area increases with the critical electrical field value. Lower R_{on} means less conduction losses, leading to higher overall converter efficiency.

In WBG materials the drift velocity is more than twice the electron drift velocity in Si. Therefore, GaN and SiC devices could be switched at higher frequency than silicon counterparts. Based on this advantage, power converters switching around or above 1 MHz could become popular, and their sizes could be shrinked drastically.

From the thermal point of view, a wider energy gap (combined to high melting point) implies higher admissible temperatures at which the power device can still operate well. In particular, SiC has also a thermal conductivity about 3 times higher

than that of silicon, so this material can better transfer heat to its surroundings. This means that the dissipation of the losses occurs with a much lower temperature drop across the device, or, in other words, that more power can be extracted from the semiconductor through the same temperature gradient.

Finally, higher energy gaps cause significantly lower junction leakage currents.

1.4 Potential impacts

As mentioned above, switching devices based on wide bandgap materials offer a significant performance improvement on the switch level compared with Si devices. These materials are capable of higher switching frequencies (hundreds of kHz) and blocking voltages (upward of tens to hundreds of kV), while providing for lower switching losses, better thermal conductivities, and the ability to withstand higher operating temperatures. The corresponding value proposition for WBG devices at system level can be summarized in the following points.

- Reduced energy costs: because WBG semiconductors are inherently more efficient than silicon, less energy is expended as heat, resulting in smaller system sizes and material costs for the same delivered power.

- High power density: due to smaller size of the power electronic devices (greater voltage and current handling capability), reduced volume of passive components (higher switching frequencies), and less critical heat sink requirements (higher operational temperature).

- Lower system cost: even if the WBG devices are generally more expensive, their use could enable overall cost reductions by decreasing the size/weight of other components such as passive inductive and capacitive circuit elements, filters, cooling system and so on.

Other possible advantages include improved transient characteristics, faster switching speed, and reduced electrical noise (due to smaller package and better reverse recovery characteristics).

However, a number of barriers and challenges still exist in utilizing wide-bandgap semiconductor devices to their full potential, and various research works investigate the actual impact of these devices on the system-level performance. For example, the influence of SiC devices on industrial inverter drives and DC-DC converters is analyzed in [4], while [5] evaluates prospective efficiency improvements and size reduction of bidirectional converter suited for hybrid or electric vehicle, when SiC power devices are utilized instead of Si switches. Similar analysis are carried out for GaN-based solutions in PV module integrated converters [6] and high-frequency resonant converters [7]. In both cases, the selected power devices increase the conversion efficiency thanks to their outstanding material properties.

1.5 Applications and perspectives

With further development, WBG semiconductors have the opportunity to meet demanding power converter requirements and to penetrate in the market, today dominated by silicon-based devices. In particular, gallium nitride and have the potential to displace silicon in power conversion. GaN and SiC devices will compete with Si counterparts for different segments of the market. GaN will take over consumer low voltage (up to 600 V) applications such as telecom power supply units, Power-over-Ethernet (PoE) equipment, and laptop adapters, while SiC will be most prominent in industrial applications that require higher voltages/currents such as traction, renewable energy or automotive inverters, and motor drives.

1.5.1 SiC

The SiC electronic journey began in the early 1990's when SiC-based single-crystal wafers became commercially available for the first time. Since the market release of 600V and 1.2kV SiC power semiconductors in early 2000's, plenty of new products based on these devices have been developed. SiC transistors are finding success especially in high voltage applications primarily due to their size advantage. Today a SiC device rated at 1.2 kV (or above) can be an order of magnitude smaller than its direct Si competitor (IGBT). This size advantage makes a significant difference

wherever there is a need for a compact, light weight, high power density converter. Furthermore, SiC is an appropriate material for robust power electronics in harsh environments. Electric and Hybrid Electric Vehicles (EV/HEV), Uninterruptible Power Supplies (UPS), and Power Factor Correction controllers (PFC) are some of the industrial applications belonging to these categories that can benefit from SiC introduction. Other appropriate market segments include High Voltage DC-DC (HVDC) transmission, railway applications, string solar and fuel cell inverters, and gride-tied power distribution systems. SiC devices have also made inroads in avionic applications since they show ten times less switching losses in comparison to Si devices for given operating conditions [8].

1.5.2   GaN

The GaN appearance in power electronic is even more recent. Applications of gallium nitride were mainly focused on opto-electronics and radio frequency uses because of its direct bandgap and high frequency performance, respectively. The GaN HEMT is an intrinsically normally-on device, which means that a negative gate bias is required to switch the device off. Nevertheless, this is not acceptable to the power electronics industry and several approaches have been developed for converting the GaN HEMTs from the conventional normally-on mode to preferred normally-off behavior. In 2009 Efficient Power Conversion Corporation (EPC) introduced the first enhancement GaN (eGaN) FET designed specifically as power MOSFET replacement. Then other companies such as GaN Systems and Panasonic has developed normally-off low-voltage GaN devices for high-efficient applications. Taking advantage of its unique material properties, these companies offer gallium nitride transistors with an on-resistance lower than attainable with silicon and exceptional carrier mobility, in smaller package. Together with negligible charge storage and low output capacitance, these features enable the design of high switching circuits with tremendous power savings. Typical applications for these devices include switch mode power supplies and small solar inverters (up to 5 kW), PC power adapters, lithium battery controllers and smart-grid systems. Finally, as explored in [9], GaN devices could also be the best solution to achieve the needs of Integrated Modular Motor Drives (IMMD) for

low power industrial motors.

Chapter 2

Bidirectional converters based on full-bridge topologies

2.1 Introduction

The task of a power converter is to supply electrical devices, by providing voltages and currents in a form that is optimally suited for them. Traditionally, a power converter regulates the flow of electric energy from the source to the user loads. However, many modern power distribution systems (energy networks for hybrid vehicle, renewable resource applications, etc.) require a bidirectional energy transfer capability as a key element of their operating functions. Preferably, this behavior should be achieved using a single electronic module to reduce size, weight and cost of the system, while still maintaining a high operating efficiency irrespective of the direction of energy flow. Dual Active Bridge structure, where two DC-AC converters are coupled back-

to-back through an AC inductor/transformer (Fig. 2.1), is the prominent proposed topology for isolated high-power density applications, due to its soft-switching properties, low number of components, and well established control techniques.
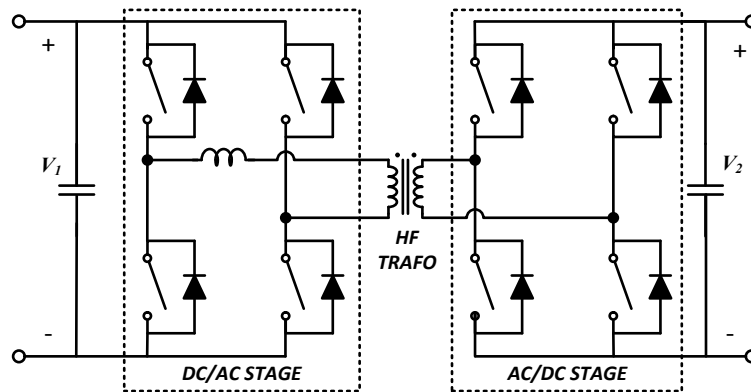
Figure 2.1: Schematic of the single-phase Dual Active Bridge converter.

In a world of growing need for efficient energy conversion and distributed generation, future power systems need to be interfaced with alternative energy sources such as fuel cells, photovoltaic, along with energy storage devices such as batteries and super capacitors, in order to achieve higher overall performance. Nowadays, most of the power electronics interfaces is realized by connecting individual DC-DC converters. In this framework, integrated power converters that are capable of combining and controlling several energy sources concurrently are a topic that has recently attracted increasing research interest. By utilizing only a single power module, a multiport converter promises a cost-effective, flexible, and more efficient energy processing compared to the conventional approach that exploits multiple converters. An emerging generation of power converters that has been proposed by researchers for the integration of distributed generation and storage is the family of isolated multiport DC-DC converters based on H-bridge cells, which has been derived from the DAB topology (Fig. 2.2). A three-port bidirectional converter has been proposed in [10] for a fuel cell and battery system to improve its transient response and also ensure

constant power output from fuel cell source. A similar topology was found in [11] for UPS application. A further extension with four ports, the so-called Quad Active Bridge (QAB), has been presented in [12] and [13] for the development of Solid State Transformers (SST).
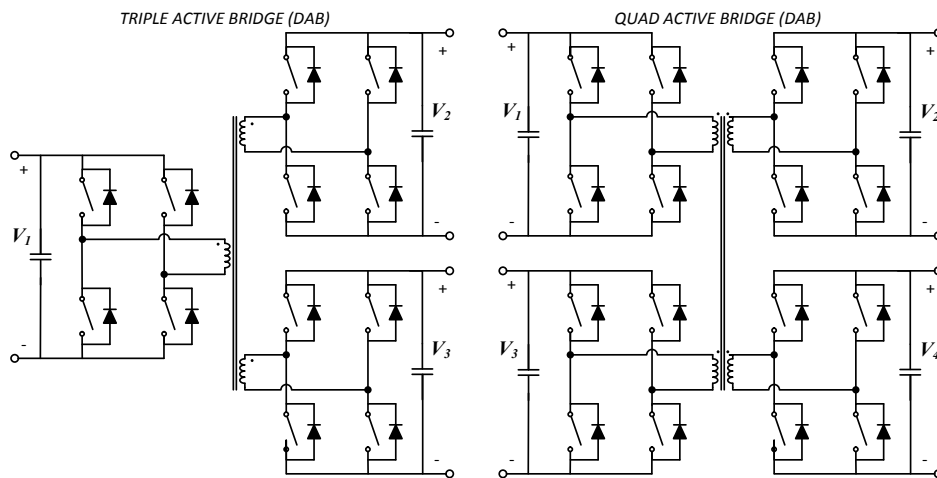
Figure 2.2: Three and four port converter for multi-source systems. The full-bridge modules are coupled by means of a multi-winding transformer, eventually with the addition of external inductors.

Isolation between multi-source systems is a mandatory requirement of many standards. In these multiport architectures, galvanic isolation is readily achieved by means of the intermediate transformer, which can be quite small and efficient if a high switching frequency is adopted. The full-bridge represents a favorable choice for realizing the basic switch cell since it ensures four-quadrant operation, enables soft-switching techniques, and has half the rms current compared to a half-bridge.

This chapter is devoted to investigate the working principle of DAB and TAB DC-DC converters, that employ phase-shift modulation. After a brief overview of the single-phase full-bridge operation modes, the equivalent circuits and the expressions to calculate the rated power for any multi-active-bridge are derived. Thereafter, the average and small signal model are developed for control purpose, referring to the

modulation strategy. Some relevant considerations are also given to identify the zero-voltage-switching region.

Since it is the most widespread solutions, the whole analysis is carried out assuming the phase-shift control strategy. In it basic form, each full-bridge operates at fixed switching frequency and 50% duty-cycle (neglecting the small dead time) to provide nearly square wave voltage across transformer terminals. The angle delay between these AC voltages determines the direction and the amount of power transfer between the input ports.

2.2 Full-Bridge converter

The full-bridge (or H-Bridge) inverter is a well-known power circuit that has been studied comprehensively in literature. Four main switches (including freewheeling diodes) are electrically connected as shown in Fig. 2.3.
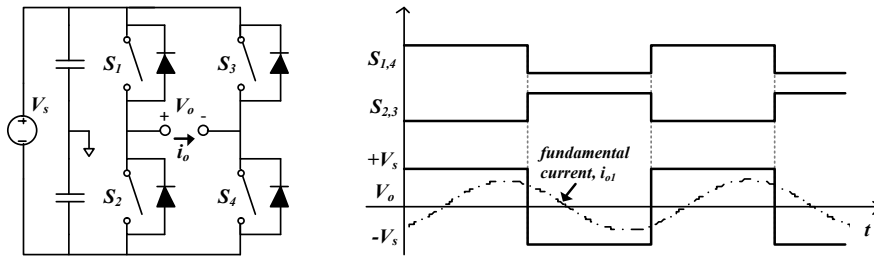
Figure 2.3: Single-phase full-bridge: electric circuit, driving signals and output waveforms in case of a generic inductive load.

According to their states combination (where '1' and '0' levels correspond to on and off conditions respectively), three output voltage levels can be synthesized:

$$V_o = \begin{cases} +V_s & \text{when } (S_{1,4} = 1 \ ; S_{2,3} = 0) \\ 0 & \text{when } (S_{1,2} = 1 \ ; S_{3,4} = 0) \text{ or } (S_{1,2} = 0 \ ; S_{3,4} = 1) \\ -V_s & \text{when } (S_{1,4} = 0 \ ; S_{2,3} = 1) \end{cases} \qquad (2.1)$$

When all switches are turned off, the current flows through the freewheeling diodes and the voltage level ($\pm V_s$) depends on the current direction. A negative output current means that energy is sent back to the generator. Two switching patterns exist for zero-voltage state. Nevertheless, assuming phase-shift control strategy, the diagonal switching pairs (i.e S_1-S_4 and S_2-S_3) in each converter are turned on simultaneously. Devices on the same leg are switched complimentary, with a needed blanking time to complete the turn-off process.

Device losses and soft-switching commutations

Broadly, three losses mechanisms affect switching converters: conduction losses, switching losses and gate driver losses. Modern applications exhibit a growing need for high efficiency combined with high power density. This combination definitely represents one of the most challenging issues for power converter design. The simplest way to reduce the size (especially magnetic components), indeed, is to increase the working frequency, but this involves an increment of switching losses, and so worse efficiency. One strategy to improve this trade-off relation is to use soft-switching topologies, that minimize the losses during the devices transitions. In brief, when a MOSFET commutates, there are losses due to voltage and current overlaps (Fig. 2.4), and the charge or discharge of stored energy in its C_{oss} capacitor[1]. Soft-switching techniques encompass Zero-Voltage-Switching (ZVS) and Zero-Current-Switching (ZCS) methodologies, that can be applied to ensure non-dissipative turn-on (ZVS)and turn-off (ZCS).
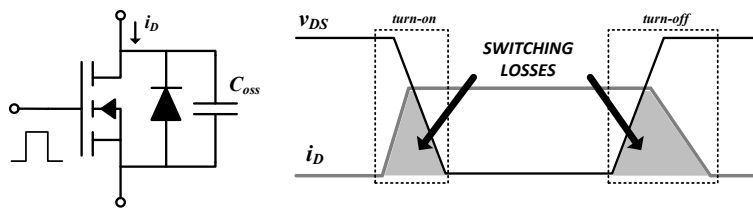
Figure 2.4: Switching losses of a power MOSFET.

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[1] $C_{oss} = C_{ds} + C_{gd}$. C_{gs} only affects the time taken to charge the input capacitance of the device before drain current conduction can start

Both foresee the use of controlled resonance phenomena and are a powerful solution for improving efficiency, reducing the electro-thermal stress and the electromagnetic radiations. In particular, ZVS technique consists of discharging the parasitic capacitor prior to turning on the MOSFET. The body diode goes into conduction during this transition, but it is not subjected to hard commutation. However, its reverse recovery must be considered: if the diode has not regained its voltage blocking capability, the bridge may incur in a shoot-through condition, that in turn might lead to failure. This problem increases dramatically with the voltage rating of the device.

2.3   Dual Active Bridge (DAB)

The dual active bridge architecture for dc-dc conversion has been popular among researchers over the past two decades since it was firstly introduced in [14] due to its high performance, high efficiency, galvanic isolation, and inherent soft-switching property. In recent years, the use of DAB converter is being investigated in renewable energy systems, transportation and hybrid vehicles. The topology has been extensively analyzed and several research papers have been published on its performance accompanied by a comprehensive analysis. In this section, the circuit principle of operation is discussed and mathematical models are derived for an accurate design of the control system.

2.3.1   Circuit description and working principle

As shown by the schematic in 2.1, the DAB converter contains two voltage sourced full-bridges connected through the transformer leakage inductance (and eventually an additional series inductor), that acts as the main current transfer element. The coupling transformer also provides the match between the input and output sides voltages, by means of winding turns ratio n. Along with small number of components, this topology includes the following favorable characteristic: low device stresses, buck-boost working modes, small filter requirements and parallel operation possible as result of phase-shift dependent current source behavior. The converter switching cycle can be split in four main intervals (not accounting for transitions). In every state,

two MOSFETs of each bridge conduct, while during the transitions between them, certain capacitors and diodes are also involved in the path of the flowing current. In order to illustrate the logic behind the basic operation, diagrams and representative waveforms are plotted in Fig. 2.5.
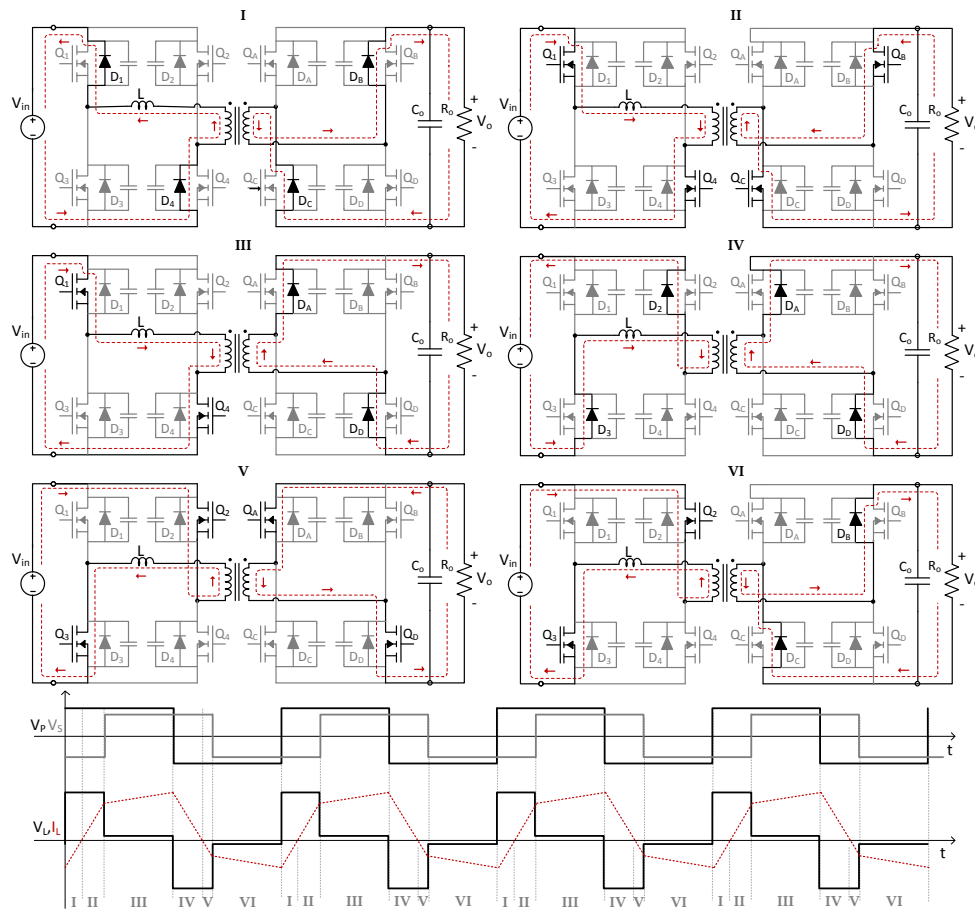
Figure 2.5: DAB converter equivalent circuits and steady-state waveforms under phase-shift control (for forward power flow). The remaining states when the output side bridge is the leading module (reverse power flow), follow the same trend.

According to Fig. 2.5, the switching sequence starts by assuming that the voltage across the inductor is positive and its current is flowing in the negative direction, i.e. through the body diodes D_1, D_4, D_B and D_C (I). At certain instant, the parent MOSFETs are actively turned on and the current eventually reverses to positive direction (II). In the third phase, Q_B and Q_C are turned off and the current starts flowing through D_A and D_D until power devices are activated and the current is softly commutated to their channels (III). In the next phase, Q_1 and Q_4 are turned off and the derivative of the current becomes negative (IV). The sequence repeats similarly in the second half-cycle. During the last steps, the power MOSFETs (Q_2, Q_3, Q_A and Q_D) are turned on while the voltage across the switches is almost zero and conduct until the modulation changes the AC voltage again. In this description, the charge and discharge process of the parasitic capacitor is not taken into considerations, hence the electrical diagrams are incomplete. Fig. 2.6 outlines the primary equivalent circuits during the omitted transient states.
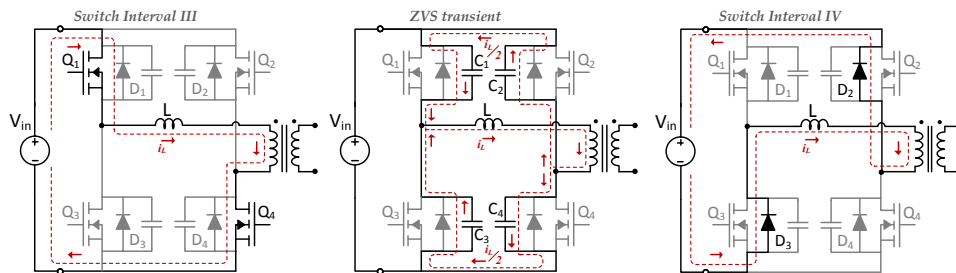
Figure 2.6: Zero Voltage Switching transient.

A proper dead-time is inserted between the commutation of each leg switch pair to enable resonant-transition of the converter. The ZVS commutations involve three steps. After the turn-off of the switch which is previously in conduction, a resonance naturally takes place among the device parasitic capacitance and the coupling inductance. The current flowing through the intrinsic capacitor discharges it and finally forces the body-diode to be forward-biased. Once its anti-parallel diode is put into conduction, the MOSFET is turned on with (almost) zero voltage across it, and the load current flows through the channel. In this process, the body-diode conduction

time should be minimized in order to reduce additional losses. A description of the design strategy to ensure ZVS operation is given in section 2.3.4.

2.3.2 Fundamental model

The steady-state analysis of the DAB is based on the equivalent lossless model outlined in Fig. 2.7 and the related operating waveforms depicted in Fig. 2.8 (a detailed DAB model, including losses, is beyond our goals and can be find in [15]).
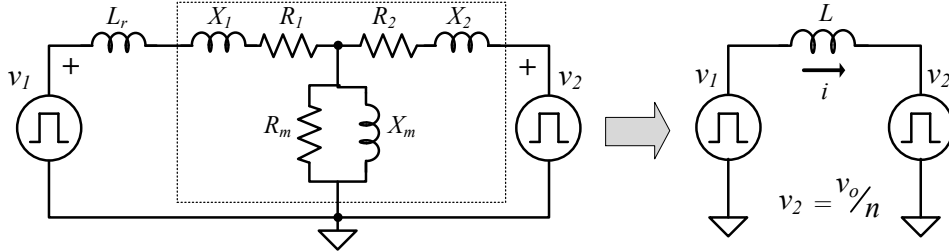
Figure 2.7: DAB equivalent circuit and ideal model. For the simplest representation all the losses are neglected, the transformer magnetizing inductance and coupling capacitances are ignored, and all the quantities are referred to the primary side.

The current generated by the equivalent voltage across the inductor is a function of $\vartheta = \omega_s t$, where ω_s is the switching angular frequency, as:

$$i(\vartheta) = i(0) + \frac{1}{L} \int_{\vartheta} v_L(\vartheta) dt = i(0) + \frac{1}{L} \int_{\vartheta} (v_1(\vartheta) - v_2(\vartheta)) d\vartheta \qquad (2.2)$$

where v_1, v_2 are input and primary referred output voltages. Thus, assuming constant supply voltages, the inductor current in the two modes of operation (i.e. when the two voltage waves have same or opposite polarity) can be expressed as:

$$i(\vartheta) = \begin{cases} \frac{V_1 + V_2}{\omega_s L} \cdot \vartheta + i(0) & \text{when } 0 \leq \vartheta \leq \delta \\ \frac{V_1 - V_2}{\omega_s L} \cdot (\vartheta - \delta) + i(\delta) & \text{when } \delta \leq \vartheta \leq \pi \end{cases} \qquad (2.3)$$

The voltages and inductor current repeat every half period with reversed signs.
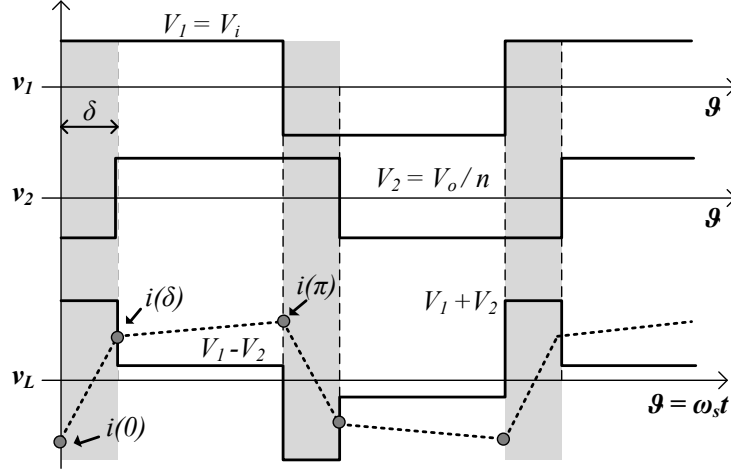
Figure 2.8: Idealized operating waveforms of the single-phase dual active bridge (for $V_1 > V_2$, $\delta > 0$). The DC components of the square voltages is zero, in order to avoid the saturation of the high frequency transformer (or the external series inductor).

At the end of the half cycle $i(0) = -i(\pi)$. Taking this condition into account yields:

$$i(\delta) = \frac{2V_1 \cdot \delta + (V_2 - V_1) \cdot \pi}{2\omega_s L} \tag{2.4}$$

$$i(\pi) = \frac{2V_2 \cdot \delta + (V_1 - V_2) \cdot \pi}{2\omega_s L} \tag{2.5}$$

Due to symmetry conditions, the average power over one switching period, can be calculated considering only the first half cycle. On the assumption of positive phase-shift ($0 \leq \delta \leq \pi$), the key expression can be derived as follows:

$$P = V_1 \cdot \overline{i(\vartheta)} = \frac{V_1}{\pi} \left(\int_0^\delta i(\vartheta) d\vartheta + \int_\delta^\pi i(\vartheta) d\vartheta \right) = \frac{V_1 V_2}{\omega_s L} \cdot \frac{\delta(\delta - \pi)}{\pi} \tag{2.6}$$

Since the converter has a unified operation principle, the direction of power flow can be changed seamlessly and a similar conclusion is obtained for negative values

$(-\pi \leq \delta \leq 0)$. By extending these outcomes to the full phase-shift range, the general equation of the transferred power results:

$$P = \frac{V_i \cdot V_o}{n\omega_s L} \cdot \delta \left(1 - \frac{|\delta|}{\pi}\right) = \frac{V_i \cdot V_o}{2nf_s L} \cdot \phi \left(1 - |\phi|\right) \tag{2.7}$$

where $\phi = \delta/n$ is the normalized phase-shift. A positive value denotes a power transfer from primary to secondary sides (forward mode), while a negative one refers to a power transfer from the secondary to the primary port (reverse mode). Regardless of the direction, power always flows from the bridge generating the leading square wave to the other one and four controllable parameters are available to adjust the power level: the phase-shift δ, the switching frequency f_s, and the duty-cycles of the square voltages. In the single phase-shift (SPS) modulation, the amount (and the direction) of power transferred is controlled only by the delay angle between the input and output H-bridges. Fig. 2.9 shows the power transfer characteristic for SPS modulation with respect to Eq. 2.7.
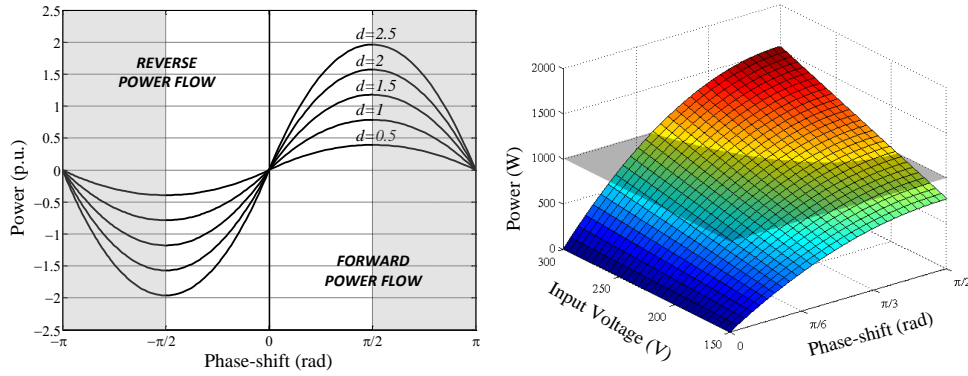
Figure 2.9: Family of output power (normalized to $P_n = V_i^2/(\omega_s L)$) versus phase-shift, with $d = V_o/(nV_i)$ as a parameter (on the left). Delivered power (case study: $L = 65$ μH, $f_s = 100$ kHz, $V_o = 28$ V, $n = 19/2$) as a function of phase-shift for a variable input voltage (on the right).

The total inductance ($\omega_s L$) defines the energy deliverable through the circuit: the maximum available power can be achieved for a phase-shift angle equal to $\pm\pi/2$,

minimum power for $\phi = 0$. However, it is important to note that minimum power (or zero output power) does not imply zero current. The current is still circulating through the devices causing losses. Consequently, zero active power does not correspond to zero reactive power. If the duty ratio is kept constant, it is not possible to achieve zero reactive power if the output power is zero. Furthermore, at constant switching frequency, a lower RMS value of the transformer current could be only achieved with a proper selection of n and L, since it is not possible to modify the shape of the transformer current. These disadvantages of phase-shift control strategy gave reason to investigate alternative modulation methods [16].

2.3.3 State Space Average (SSA) model

Modeling and simulation of electrical systems are crucial steps that enable design of power converters and verification of numerous aspects related to their performance. With an accurate small-signal model, the controller synthesis is quite direct, and stability problems can be easily foreseen with pole plots. In particular, the state space averaging has been demonstrated to be an effective method for analysis and control design in pulse-width-modulated switching power converters. In this section, dynamic phasor approach and first harmonic approximation are exploited to obtain the functional representation of dual active bridge.

Dynamic phasor

The dynamic phasor modeling technique (also referred to as the general averaging model [17]) is essentially a frequency-domain analysis method based on the Fourier series expansion of a generic waveform $x(t)$, that is given by:

$$x(t) = \sum_k X_k(t)e^{jk\omega_s t} \tag{2.8}$$

where $\omega_s = 2\pi/T$, T is the window length (usually the fundamental period), and $X_k(t)$ are the complex Fourier coefficients (or dynamic phasors):

$$X_k(t) = \frac{1}{T} \int_{t-T}^{t} x(\tau)e^{-jk\omega_s \tau}d\tau = \langle x \rangle_k(t) \tag{2.9}$$

In contrast to the traditional Fourier representation, these coefficients are time-varying as the integration interval slides with time. For electric power systems, this approach provides a middle ground between sinusoidal quasi-steady-state analysis and time-domain representation. Two key factors in developing dynamic phasor equivalent models starting from their time-domain equations, are the derivative and the convolution properties (Eq. 2.10) of the k-th Fourier coefficient:

$$
\begin{aligned}
\left\langle \frac{dx}{dt} \right\rangle_k &= \frac{d\langle x\rangle_k}{dt} + jk\omega_s \langle x\rangle_k \\
\langle xy\rangle_k &= \sum_i \langle x\rangle_{k-1} \langle y\rangle_i
\end{aligned}
\tag{2.10}
$$

By employing these definitions, the dynamic phasor models of main electrical components can be achieved conveniently. For instance, the transformation of the time-domain voltage dynamic equations of a resistor and an inductor can be calculated as follows:

$$
v(t) = Ri(t) \quad \rightarrow \quad \langle v\rangle_k = \langle Ri\rangle_k = R\langle i\rangle_k
\tag{2.11}
$$

$$
v(t) = L\frac{di(t)}{dt} \quad \rightarrow \quad \langle v\rangle_k = \left\langle L\frac{di}{dt} \right\rangle_k = L\frac{d\langle i\rangle_k}{dt} + j\omega_s L\langle i\rangle_k
$$

Small-signal model

As explained in the previous section, the dual active bridge power circuit can be conceptually viewed as an inductor driven at either end by a controlled square wave voltage source. The power transfer mechanism is dominated by interaction between the fundamental components of voltages and currents at the switching frequency. Hence, under the assumption that all the higher harmonics have a negligible impact on the converter operation, the square wave voltage sources can be replaced by their fundamental components (Fig. 2.10) and a single frequency (f_s) phasor analysis can be carried out. Since all circuit quantities are sinusoidal the real (P) and reactive (Q) power of the AC equivalent system are given by:

$$
P = \frac{V_1 V_2}{\omega_s L} \cdot sin(\delta) \qquad\qquad Q = \frac{(V_1 V_2) \cdot cos(\delta) - V_2^2}{\omega_s L}
\tag{2.12}
$$

As pointed out in [18], these equations reveal that the real power transfer is primarily determined by the phasor angle between the two source voltages, while the reactive power is determined by their magnitude difference.
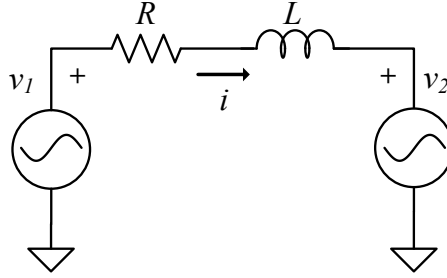
Figure 2.10: First Harmonic Approximation (FHA) model of DAB converter.

In order to derive desired transfer functions, the dynamic phasor has been considered to transform the system into the complex domain. According to the equivalent circuit in Fig. 2.10, the dynamic behavior of the DAB converter is expressed by Eq. 2.13 and its phasorial transformation can be derived as Eq. 2.14.

$$v_1(t) - v_2(t) = Ri(t) + L\frac{di(t)}{dt} \tag{2.13}$$

$$\frac{d\langle i \rangle}{dt} = \frac{1}{L}[\langle v_1 \rangle - \langle v_2 \rangle - (R + j\omega_s L)\langle i \rangle] \tag{2.14}$$

Based on the procedure detailed in Appendix A, splitting real and imaginary components of the quantities involved, a non-linear system can be achieved with a DC operating point where linearization can take place. An additional differential equation imposing the power balance on the output capacitor, allows to include also the secondary side voltage ($v_o = nv_2$) as a state of this model. Finally, the resulting state space representation can be linearized around the steady-state operating point for the phase-shift δ_0, output voltage V_o and for the real and imaginary components of the

inductor current phasor (I_{c0}, I_{s0}). The linearized state space model is given by:

$$
\begin{bmatrix} \hat{i}_c \\ \hat{i}_s \\ \hat{v}_o \end{bmatrix} = \underbrace{\begin{bmatrix} -\frac{R}{L} & \omega_s & \frac{2\sqrt{2}}{nL\pi}sin\delta_0 \\ -\omega_s & -\frac{R}{L} & \frac{2\sqrt{2}}{nL\pi}cos\delta_0 \\ -\frac{2\sqrt{2}}{nC_o\pi}sin\delta_0 & -\frac{2\sqrt{2}}{nC_o\pi}cos\delta_0 & -\frac{P_o}{C_o v_o{}^2} \end{bmatrix}}_{F} \begin{bmatrix} i_c \\ i_s \\ v_o \end{bmatrix} +
$$

$$
\underbrace{\begin{bmatrix} \frac{2\sqrt{2}}{nL\pi}V_o cos\delta_0 & 0 \\ -\frac{2\sqrt{2}}{nL\pi}V_o sin\delta_0 & 0 \\ -\frac{1}{C_o}\frac{2\sqrt{2}}{n\pi}\left(cos\delta_0 I_{c0} - sin\delta_0 I_{s0}\right) & \frac{1}{C_o} \end{bmatrix}}_{G} \begin{bmatrix} \hat{\delta} \\ \hat{i}_o \end{bmatrix}
$$

(2.15)

The 3x2 matrix M of all the linearized transfer functions linking the two inputs (δ, i_o) to the three state variables (i_c, i_s, v_o) can be extracted using:

$$
M(s) = (sI - F)^{-1} \cdot G \tag{2.16}
$$

With reference to an application where the primary objective of the DAB converter is to generate a stable DC output voltage, the most relevant statement is the transfer function linking the control variable (phase-shift, δ) to the output voltage (and eventually to the inductor current) of the converter.

$$
M_{(3,1)} = \frac{v_o(s)}{\delta(s)} = G_{DAB}(s) \tag{2.17}
$$

The analytical model has been validated by means of time-based simulation of the circuit using Matlab toolboxes. The routine for the measurement of the small signal model from the full Simulink-PLECS scheme of the converter starts defining a set of frequencies where the transfer function has to be tested. For the various operating conditions to be investigated, the proper phase delay between the two bridges is determined by Eq. 2.7 and circuit simulations are performed. At the end of each simulation, a FFT (Fast Fourier Transform) is used to get magnitude and phase of the signals and derive the transfer function from phase-shift to output voltage. The

simulated frequency response and the theoretical expectation from the state space model are plotted in Fig. 2.11. The Bode diagrams exhibit a good agreement up to one decade down from the nominal switching frequency (100 kHz in this case study). Only at this point some divergences in magnitude and phase emerge.
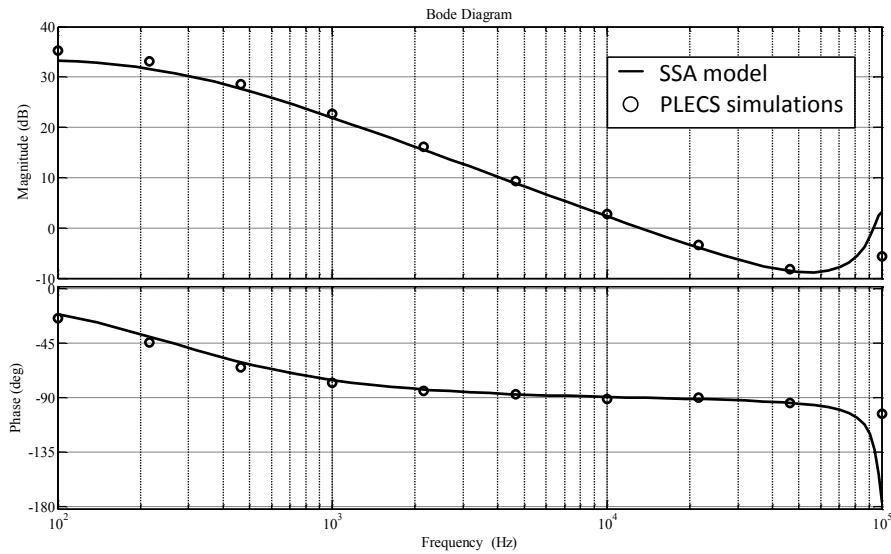
Figure 2.11: Bode diagrams comparing the analytical transfer function with the simulated values.

2.3.4   Design for ZVS

One of the major advantages of the DAB is soft-switching commutation of all the devices at nominal conditions, that improves efficiency, reduces switching-related EMI, and eliminates the need for snubbers. This behavior relies on the ZVS principle. Thereby it must be ensured that turn-on of a switch only takes place when its anti-parallel diode is conducting. If this condition is fulfilled, the drain to source voltage of the switch is quasi zero at turn-on, almost completely eliminating the switching losses. The values of the inductor current whenever the driving square wave voltages change their polarity are especially relevant. In particular, considering the first half-

period, $i(\delta)$ and $i(\pi)$ must be greater than zero, in order to ensure that the current flow through the parasitic body diode of the transistor that must be turned on:

$$i(\delta) \geq 0 \quad \text{and} \quad i(\pi) \geq 0 \tag{2.18}$$

Solving for δ the equations 2.4 and 2.5 yields the phase-shift for the necessary conditions to achieve ZVS in the leading and lagging full-bridges, respectively:

$$\begin{aligned} \delta \geq \frac{\pi}{2}\left(\frac{V_2 - V_1}{V_1}\right) = \frac{\pi}{2}(d-1) \\ \delta \geq \frac{\pi}{2}\left(\frac{V_1 - V_2}{V_2}\right) = \frac{\pi}{2d}(1-d) \end{aligned} \qquad \text{where } d = \frac{V_2}{V_1} \tag{2.19}$$

These boundary constraints and the soft-switching region are represented in the normalized power plane (Fig. 2.12).
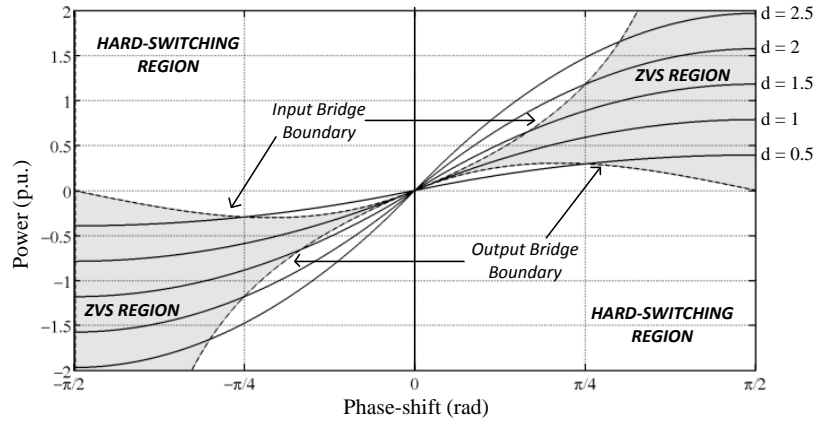
Figure 2.12: Family of normalized output power versus phase-shift characteristics, highlighting the soft-switching limits.

Full control range in the soft-switching mode is achievable only when the converter voltage ratio is equal to one ($d = 1$). When $d \neq 1$, the soft-switching region is limited to a smaller area near the maximum output current. Since the slope of the current depends on d, when the voltage ratio changes, the time needed by the current

to reach zero change as well. Furthermore, the available time to invert the current is proportional to δ, hence for low phase-shift, this period is also reduced. As a consequence, the soft-switching could not be obtained for the entire power range. In particular, for high phase-shift values (which imply high current and hence higher power) ZVS is achieved even for values of d quite different from 1, while for low δ, this is only achieved when d is really close to the unit.

The aforementioned constraints must be satisfied to achieve ZVS, although the limits expressed by Eq. 2.19 do not ensure soft-switching, even in case of $d = 1$. The sufficient conditions to obtain ZVS include the influence of the parasitic capacitances of the transistors. Normally, the device output capacitance is of low value, however if the energy stored in the junction capacitors cannot be ignored, a minimal current in the series inductance is required to complete the ZVS commutation [19]. In the absence of a snubber capacitor across the device, during turn-off, resonance would naturally occur between the intrinsic capacitance (C_{oss}) and the coupling inductance (L). Thus, the sufficient condition to achieve ZVS is that the energy stored in the resonant inductance must be greater than the energy required to charge and discharge the MOSFET output capacitances of the leg in transition within the blanking time. This condition is represented via the following equation:

$$E_L \geq E_{C_{eq}} \quad \rightarrow \quad \frac{1}{2}LI_x^2 \geq 4 \cdot \left(\frac{1}{2}C_{oss}V_x^2 \right) \tag{2.20}$$

where I_x is the current through the coupling inductor when the leading and lagging full-bridges are switched ($i(\delta)$ and $i(\pi)$, respectively), and V_x is the input or output voltage, depending on the evaluated condition. The sufficient boundaries can be estimated by solving the expression of the minimum required currents as follows:

$$i(\delta) \geq 2V_2 \cdot \sqrt{\frac{L}{C_{oss_o}}} \quad \rightarrow \quad \delta \geq \frac{\pi}{2}(1-d) + 2\omega_s d \sqrt{LC_{oss_o}}$$

$$i(\pi) \geq 2V_1 \cdot \sqrt{\frac{L}{C_{oss_i}}} \quad \rightarrow \quad \delta \geq \frac{\pi}{2}\frac{d-1}{d} + \frac{2\omega_s}{d}\sqrt{LC_{oss_i}} \tag{2.21}$$

where C_{oss_i} and C_{oss_o} are the output capacitance of the power devices utilized in the primary and the secondary full-bridges, respectively.

The impact of the intrinsic capacitance of the power devices on the ZVS limits can be easily appreciated in Fig. 2.13: when the power handled by the DAB is reduced, soft-switching property can be lost. The ZVS commutations can be kept down to a minimum value of the delivered output power, after which the current in the inductor becomes too small to yield a full charge/discharge of the resonating capacitors.
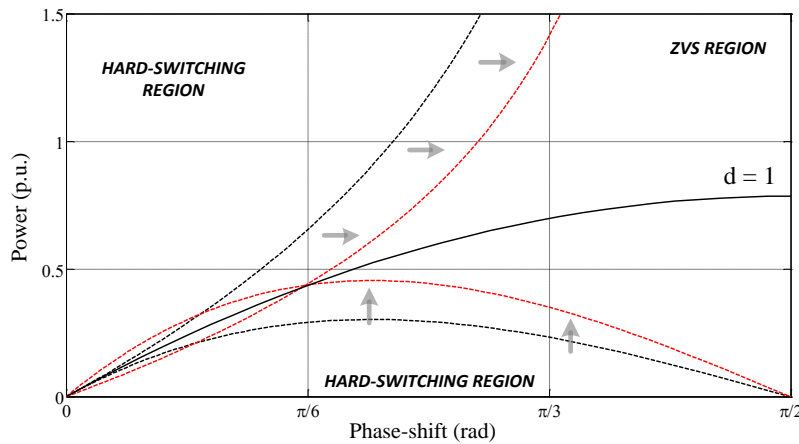
Figure 2.13: Necessary conditions to achieve ZVS operation, taking into account the effect of charging/discharging parasitic capacitances during device commutations.

As previously described, maintaining ZVS over a wide power range is an interesting design goal, especially for HV applications, in which hard-switching operation is usually avoided. For that reason, control strategies for DAB DC-DC converters has been proposed, aiming at complete ZVS over the whole operating range. [20] proposes Dual-Phase-Shift (DPS) modulation to maintain soft-switching from nominal power down to light load. In [21] a pulse-width-modulation is added in one of the converter bridges, to introduce a new degree of freedom that allows controlling the current waveform and extend the soft-switching operating mode region. In [22] the AC-link reactance variation, by means of variable switching frequency and/or adaptable inductance is used to extend the ZVS region to cover almost the whole operating area. Finally, it should be noted that ZVS eliminates only turn on losses; switching losses during turn-off, due to overlap and capacitance charging, will still be incurred.

2.4   Triple Active Bridge (TAB)

The three-port extension of DAB configuration is depicted in 2.2. This topology is particularly relevant to multiple voltage electrical systems in hybrid electric vehicles and renewable energy generation plants [23]. Three active bridges are connected through a three-winding transformer and a network of inductors. The transformer provides electrical isolation between buses, its leakage inductances are employed to transfer energy between the sources, and different voltages can be matched by the suitable turns ratios. The implementation with full-bridge cells enables bidirectional power flow capability for each port of converter. In the simplest control strategy, every H-bridge generates a PWM voltage (at the same frequency) and the power flow among the three ports is regulated by the reciprocal phase-shift between them (usually with the primary side set as reference).

Conceptually, the power circuit can be viewed as a grid of inductors driven by controlled square wave voltage sources, as shown in Fig. 2.14, where $L_{1,2}$, L_{23}, and L_{13} represent the primary referred transformer leakage and optional external inductor, and v_2, v_3 are the equivalent voltages referred to the primary side. The relative displacements (δ) of these voltages enforce the power flow among the sources and shape the inductor currents, as shown by the idealized main waveforms illustrated in Fig. 2.15.
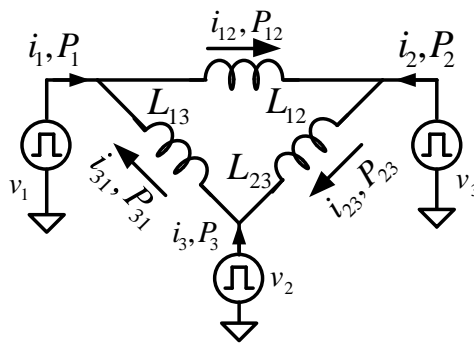
Figure 2.14: Δ-equivalent model of phase-shifted TAB converter.
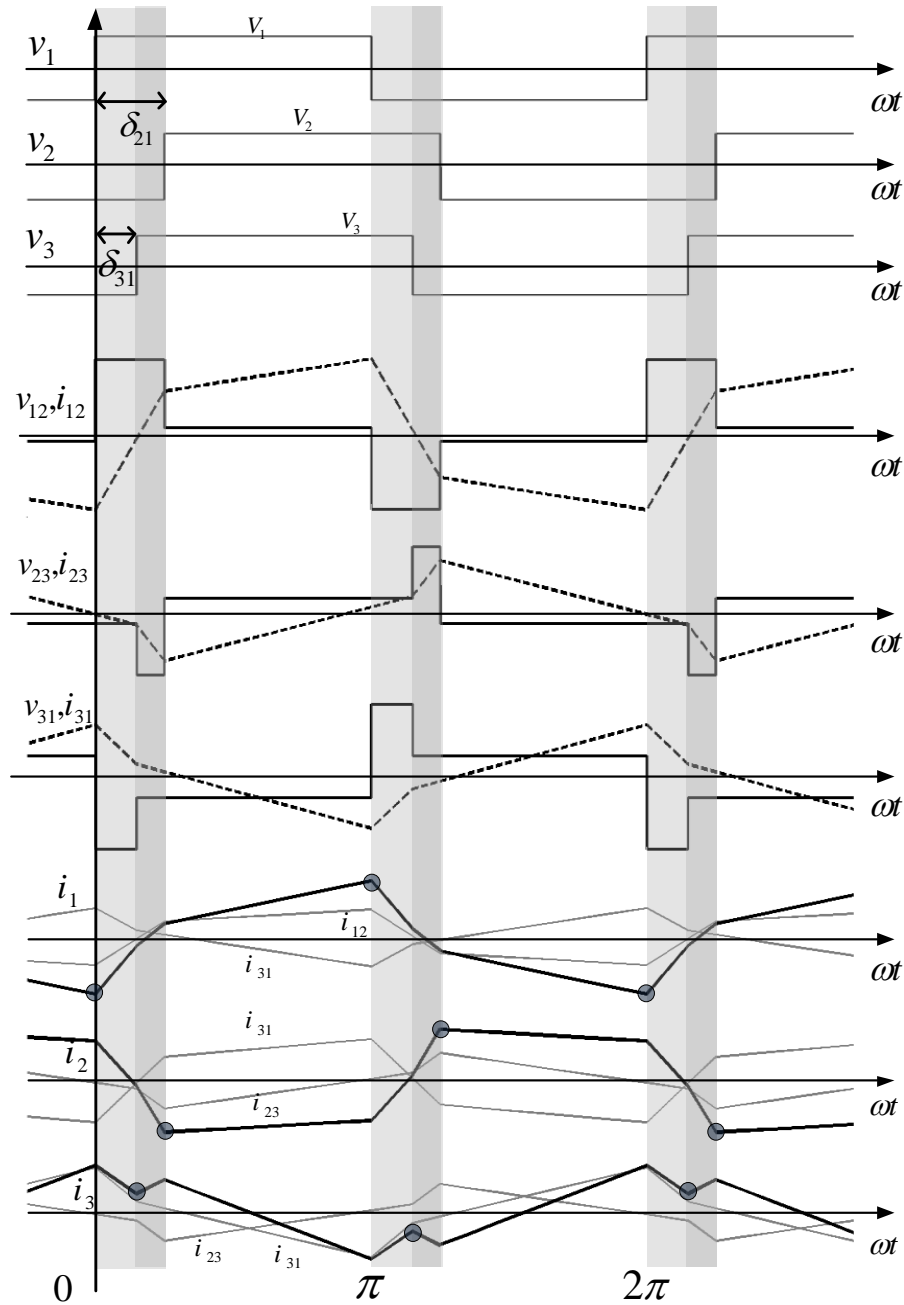
Figure 2.15: TAB characteristic waveforms for $V_1 > V_2 > V_3$ and $\delta_{31} > \delta_{21} > 0$.

According to this schematic representation, the amounts of power and the currents flowing into the circuit can be written as a linear combination of three two-port models [10]:

$$
\begin{aligned}
P_1 &= P_{12} - P_{31} &&; & i_1 &= i_{12} - i_{31} \\
P_2 &= P_{23} - P_{12} &&; & i_2 &= i_{23} - i_{12} \\
P_3 &= P_{31} - P_{23} &&; & i_3 &= i_{31} - i_{23}
\end{aligned}
\tag{2.22}
$$

where the key equations can be derived using the formulas developed for the DAB converter.

$$
P_{\alpha\beta} = \frac{V_\alpha V_\beta}{\omega L_{\alpha\beta}} \delta_{\alpha\beta} \left(1 - \frac{|\delta_{\alpha\beta}|}{\pi} \right)
$$

$$
i_{\alpha\beta}(\omega t) =
\begin{cases}
\frac{V_\alpha + V_\beta}{\omega L_{\alpha\beta}} + i_{\alpha\beta}(0) & \text{when} \quad 0 < \omega t < \delta_{\alpha\beta} \\
\frac{V_\alpha - V_\beta}{\omega L_{\alpha\beta}} + i_{\alpha\beta}(\delta_{\alpha\beta}) & \text{when} \quad \delta_{\alpha\beta} < \omega t < \pi
\end{cases}
\tag{2.23}
$$

The direction of the power flow is determined by the sign of the phase-shift angle (where a positive value indicates that the corresponding port acts as a source, and a negative one marks that the power is sunk by the associated port). The converter has the favorable capability of directly supplying power from an input to an output (without charging/discharging the third element), by using a proper selection of the phase-shifts.

The commutation mechanism is similar to the dual active bridge bidirectional converter. Extending the analysis carried out in the previous section, the necessary ZVS conditions imply:

$$
\begin{aligned}
i_1(0) \, , \, i_2(\delta_{12}) \, , \, i_3(\delta_{23}) &\leq 0 \\
i_1(\pi) \, , \, i_2(\delta_{12} + \pi) \, , \, i_3(\delta_{23} + \pi) &\geq 0
\end{aligned}
\tag{2.24}
$$

The soft-switching condition becomes more complicated due to the interactions between the multiple input stages, however, in the three-port TAB converter, ZVS conditions can always be achieved to reduce switching losses. An effective method

is proposed by [24] and [25] to obtain this behavior. The so-called "duty-cycle control"consists in continuously adjusting the duty-cycle on the storage side H-bridge according to the voltage level, in order to extend the ZVS region over the entire working range.

2.5   Conclusion

In this chapter the operation principle of multiport full-bridge converter using phase-shift modulation has been investigated. The steady-state analysis of the dual active bridge has been performed adopting the fundamental model, and the representative mathematical expressions have been derived on symmetry assumption. In particular, the equation to calculate power transfer as function of the controllable phase-shift has been studied. The converter dynamics have been presented by using a state-space averaging technique based on first harmonic approximation. The results were used to develop a control-oriented small signal model and Bode plot of the relevant transfer function is given. These theoretical and analytical considerations have been verified by digital simulation based on circuit schematic. The proposed model was proven to be reasonably accurate for performance characterization and design of the control loops. Additionally, the principle of zero-voltage-switching was discussed and ZVS operation limits have been derived, taking into account the presence of devices parasitic capacitance. Finally, a brief overview of the three-port active bridge converter was given.

Chapter 3

SiC-based converter for avionic application

3.1 Introduction

The market demand for more energy efficient aircraft has grown tremendously during the last few decades and is driven by many stakeholders including airline operators, legislators, and public opinion. In many aspects the motivations for this research are similar to those for vehicles and include goals to reduce emissions and decrease fuel consumption [26].

3.1.1 Power distribution on a conventional aircraft

On a traditional aircraft, all the power needed is extracted from the jet engines that exploit the energy stored in fuel. Most of this power is expended as propulsive thrust

to keep the airplane flying. The remaining is transmitted to the primary and secondary subsystems on board, such as flight surface actuators, de-icing loads, avionic controls, passenger entertainment, cabin air conditioning, and engine start [27].

In a conventional architecture, the power required for those subsystems is typically derived from a combination of:

- Mechanical power, which is transferred by means of gearboxes from the engines to the central hydraulic pumps, fuel pumps, and electrical generators.

- Hydraulic power, generated from the main pump that feed the actuation systems for flight control actuators, aircraft braking, landing gear, door closure and numerous ancillary systems.

- Pneumatic power, obtained by bleeding the compressor to drive turbine motors for the engines' starter subsystem, and Wing Ice Protection System (WIPS) and Environmental Control Systems (ECS).

- Electrical power, employed for cabin and aircraft lighting, galleys, and other commercial loads (such as passenger comfort or entertainment systems).

All energy types have different drawbacks, including the sacrifice of total engine efficiency in the process of harvesting a particular form, as with hydraulic and pneumatic systems [26]. Moreover, in modern aircraft each system has become more complex, and interactions between different pieces of equipment reduce the performance of the whole apparatus. Therefore, even if firmly established and well understood, these traditional technologies do not realize the most convenient structure to generate, distribute, and consume energy in an effective and efficient manner.

In order to address this issue and driven by the demand to decrease operating and maintenance costs, the aerospace industry is pushing towards all electrical aircraft, which means that all power take-offs from the engine are electric in nature [28]. The first steps in that direction involve the replacement of mechanical and hydraulic components by their electrical counterparts, and the use of electric power for driving all non-thrust subsystems.

3.1.2 More Electrical Aircraft (MEA)

The concept of More Electrical Aircraft (MEA) provides for the utilization of electric power for all non-propulsive equipment that are usually driven by a combination of different secondary power sources such as hydraulic, pneumatic, mechanical and electrical [29]. Although electrical actuation needs electric motors, power converters and controllers, it has many potential advantages in terms of fuel burn saving, increased reliability, reduced maintenance cost and emissions. A detailed description of these expected benefits can be found in [30].

Specifically, removal of hydraulic systems, which are costly, labor-intensive, and susceptible to leakage and contamination problems, improves the aircraft reliability and reduces complexity, weight, installation and running cost. The same applies to the replacement of the engine-bleed system by electric motor-driven pumps. Another key enabler is the electrification of the ECS, as it is the biggest steady state power consumer during aircraft cruise. Finally, additional advantages that the move to MEA brings are the modular nature of the system and the flexibility to generate and distribute power near to where it is being consumed.

A basic schematic comparison between traditional aircraft and a MEA power distribution architecture is shown in Fig. 3.1. The salient differences are the transition to electromechanical, electro-hydrostatic or pure electrical actuators, and the increasing level of electrical power extracted via the engine-mounted generators (different ways are discussed in [31]). Conceptually, electrical power for a MEA would be produced by a starter/generator directly driven by the main engine. Once power has been transferred out of the engine and distributed into the electrical network then it is available to supply the aircraft services.

The variety of load types on board requires power supply voltages that are different from those provided by the main generators. As the trend continues to replace the non-propulsive systems, that aspect is going to be even more demanding. Thus, power electronics has become a key element essential for any future platform, since it should provide the matches between loads and generator, and allow loads to be controlled. From the previous statements, it is clear that advances in power conversion are essential to achieve the MEA goals and potential. The all electrical aircraft is not a
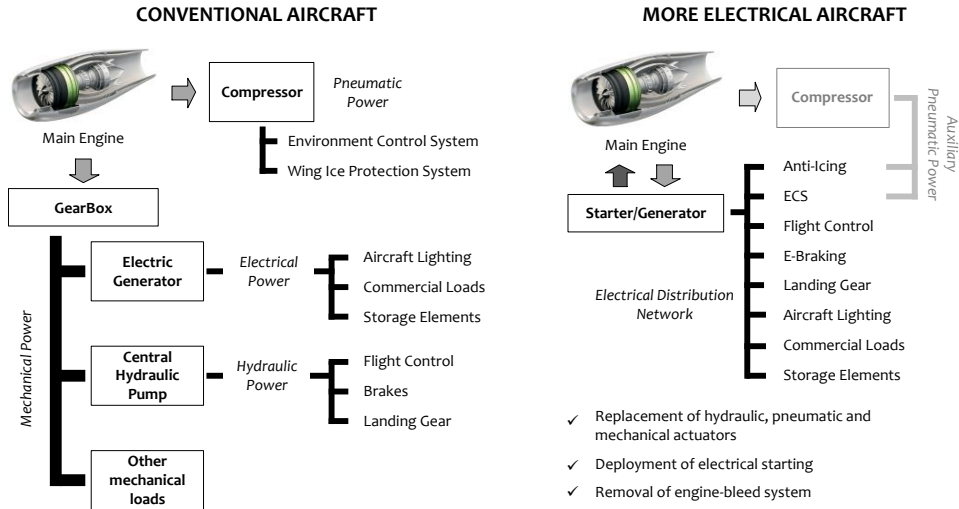
Figure 3.1: Schematic comparison between conventional aircraft and MEA power distribution network.

novel concept indeed, but the lack of electric power generation capabilities has made this idea prohibitive until recently. Over the last few decades, power electronics has made tremendous breakthroughs creating a viable path to efficiently drive the majority of aircraft subsystems by means of high power-density electrical components. Nowadays the potential exists to make the MEA approach completely feasible for the next generation aircrafts.

As mentioned above, increasing use of electric power to drive aircraft subsystems is the opportunity to significantly improve the aircraft power system performance, reliability, and maintainability. While offering great opportunities, more electric approach also poses significant technical and business challenges to the industry, both in the amount of the required power and the processing and management of this energy. Some of these challenges to met and key technologies to be acquired, before a much more electric aircraft becomes commonplace are highlighted in [30]. Also the overall system integration must not be underestimated. Different options for power generation topology are investigated in [32].

In conclusion, the design of power distribution network implies a complex effort and the development of new electric architecture concepts is mandatory in order to meet tomorrow's aircraft power requirements.

3.1.3 The REGENESYS project

Given that the aerospace industry is highly regulated, before any concept turns into a product for a commercially operated aircraft, significant validation and verification effort has to be directed into demonstration and test activities. In order to boost this process, the European Union is founding ambitious research programmes through the Clean Sky JTI (Joint Technology Initiative) to significantly improve the air transport.

The Regenerative Multi-Source Power Conversion System (REGENESYS) forms part of the overall Cleansky Green Rotorcraft ITD (Integrated Technology Demonstrator). The main purpose of this project is to develop a flexible power conversion system embedding multiple energy sources, as well as energy recovery and storage capability, which could be implemented onto a suitable rotorcraft platform and would contribute to an overall efficiency gain in the operation of Electric Power Generation Distribution System (EPGDS). That could cut the carbon footprint of the aircraft leading to reduced mass, maintenance, emissions and noise pollution. The power distribution network has been primarily designed to be installed on a helicopter, but it can be further developed toward a future aircraft power architecture.

Generally, electrical power generation on an aircraft is based on the use of 115V 400Hz AC and 28V DC power systems, with the AC power being utilized for high power loads, such as blade de-icing and DC being used for flight deck avionics and lighting loads. The REGENESYS technology demonstrator (Fig.3.2) is developed for the use with this typical high voltage bus and includes:

- Bidirectional power converters, which interface the nominal 270V DC power bus to the loads with additional regenerative capability and energy storage functions.

- Storage element(s), based upon commercially available lithium-titanate batteries, that allow safe high current charge and discharge, and can directly support

the requirements of the regenerative energy profile from a rotocraft rotor.

- A variety of avionic loads and regenerative sources.

- A sophisticated Converter Controller Unit (CCU), and its associated software, which implements the digital loop closure for power elements and may intelligently manage the overall system providing a stable, flexible power distribution. In addition, the system also includes a Micro-Controller Module (MCM) to interfaces the converters to the communication data bus.
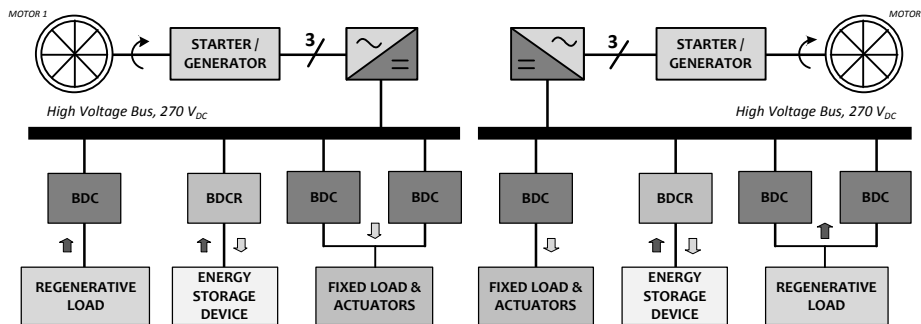
Figure 3.2: Basic schematic of the proposed EPGDS.

A critical component of this architecture is the high-efficiency DC-DC power converter. The proposed distribution network employs two different types of Bi-Directional Converters (BDCs). One (Regenative Bi-Directional Converter, BDCR) is designed to handle the fast regenerative energy from the rotor brake following a landing. It works between 270 V and the storage sub-system voltages (185 V). The second one (BDC) distributes power supply to low voltage (28 V) loads, that could be regenerative sources or otherwise. Both can be adapted to meet changing aircraft requirements, such as future 540V DC bus.

The development of the power converters for this application brings various challenges, such as high power density or high temperature capability that must deal with volume and weight constraints. the following sections explain the design details of the BDC unit, including some considerations about the thermal management.

3.2   Bidirectional DC-DC converter

3.2.1   BDC requirements

The system is aimed at the power distribution of a small helicopter. The converter specifications are derived taking also into account further enhancements, so that such a system can be applied to a generic future aircraft (whether aircraft or rotorcraft). As anticipated, the REGENESYS power network requires an optimized DC-DC converter working between 270V DC and 28V DC bus. It should achieve 1.2 kW maximum power and operate with efficiency greater than 90% within all the operation range. Since it is intended to connect either avionic loads and regenerative sources, the converter must be also able to manage bidirectional power flow.

High switching frequency (50-100 kHz) is required. Typically, by increasing the frequency, the size of the magnetic components and the capacitive filters can be reduced. This is expected to have a lot of influence on the overall converter size, helping to match the target volume and weight, that are 1 liter and 1.5 kg, respectively. Higher-frequency operation also endows the switching regulator with greater bandwidth, boosting the converter transient response.

As motivated in the previous section, for this application a distributed structure of power supplies is preferred in order to ensure modularity and robustness. The ease of paralleling is another desirable feature to improve the flexibility of the system, so that these converters may potentially work together to deliver the requisite power of some specific loads with higher power demand.

Finally, the system shall be capable of uninterrupted operation over the temperature range -55°Cto +80°C, with no need of any separate forced cooling.

3.2.2   Topology comparison

Theoretically, many different topologies are able to satisfy the above discussed specifications. The range of investigation is further restricted by including other attractive characteristics beyond the mandatory requirements, such as: fixed frequency operation (for predictable EMI performance and easier control), resonant-transition soft-

switching capability (for losses reduction and circuit simplicity), and low-order dynamics (for ease of implementation).

For a comparative study among relevant DC/DC converters, the following isolated high step down architectures have been considered (Fig. 3.3):

- Two-Stage Isolated (TSI) converter [33];

- Cyclo-Converter Based (CCB) converter [34];

- Dual Active Bridge converter, in two implementation options: Full-Bridge (FB) at both sides and Center-Tapped (CT) secondary winding.
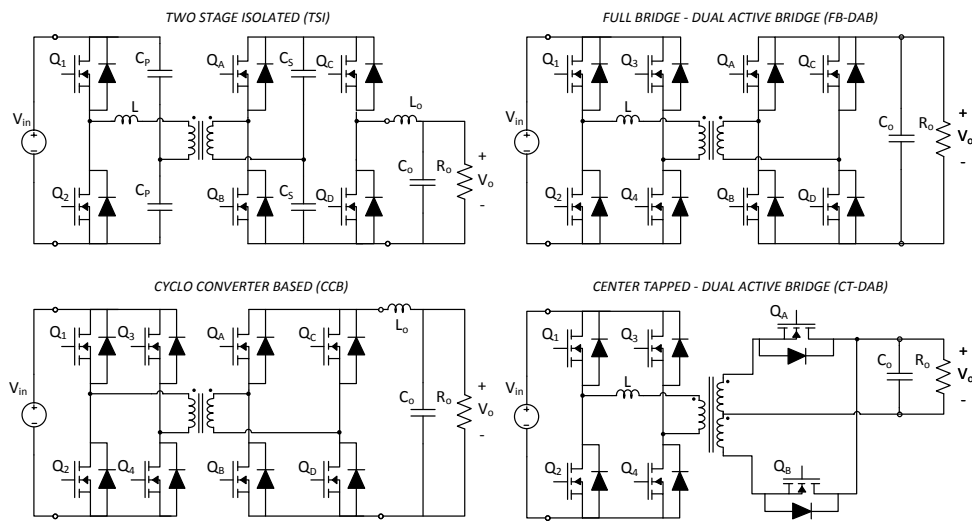
Figure 3.3: Preselected DC-DC power converter topologies for comparative study.

A detailed investigation has been carried out in [35], based on extensive circuit simulations that employ realistic physics-based compact models of the semiconductor devices. The benchmark criteria are semiconductors losses, size (volume of capacitors and magnetic components), and filtering requirements. Some results are briefly reported in Fig. 3.4, and Table 3.1 summarizes the selection outcomes.

None of the candidates is superior to all others in every respect. TSI requires the lowest number of power switches, DAB is expected to have the highest efficiency, CCB the smallest input filter size, and each achievement likely comes with trade-offs in the design. However, in view of the overall scenario, FB-DAB is shaping out to be the best performing solution for the specific application amongst all the ones assessed. It features high power density, high efficiency, bidirectional power flow capability, inherent soft switching, galvanic isolation and low number of passive components. Moreover, from a control perspective, the DAB acts as a controlled current generator enabling ease of paralleling units for higher power demands. fontssymbols
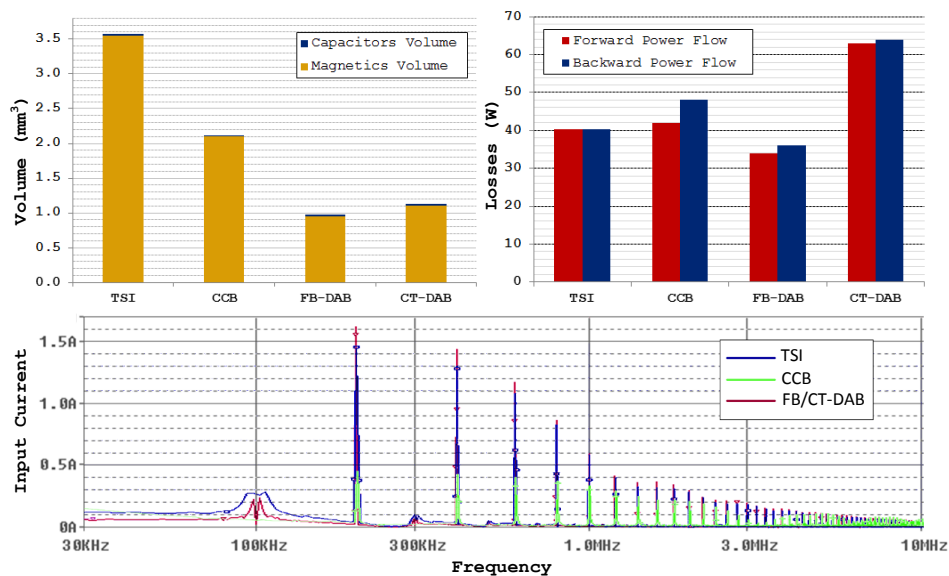
Figure 3.4: Comparison among the various power converter structures analyzed: estimated volume, simulated semiconductor losses (considering transformer leakage inductances) and input current harmonics content, at nominal power.

Table 3.1: Summary of the comparison across the suitable topologies (Fig. 3.3).

Feature	Topology			
	TSI	**CCB**	**FB-DAB**	**CT-DAB**
Number of power devices	6	8	8	6
Volume of passive components	××	×	✓✓	✓
Semiconductor losses (forward)	✓	✓	✓✓	×
Semiconductor losses (backward)	✓	×	✓✓	×
Input filter requirements	×	✓✓	×	×
Control	×	×	✓✓	✓✓

3.2.3 Components selection

The magnetics are core components of the converter: the transformer, provides galvanic isolation and voltage matching; the series inductor determines the maximum achievable power and the current waveforms flowing through the circuit. In principle, it could be embedded as leakage inductance of the transformer in the forms of integrated magnetics to enhance a compact design. However, since its value directly affects the converter control and dynamic characteristics, the two elements are kept separate at this development stage. That also enables an optimization of the transformer efficiency and thermal management. Hence, as the transformer provides a leakage inductance of 7 μH, additional 48 μH inductor is required to achieve the desired total value of 55 μH. In view of the turns ratio (19:2), a planar implementation is employed to deliver a solution with contained overall volume and weight. In order to further optimize the thermal behavior and the converter shape, the magnetic devices are enclosed in a dedicated heat sink. Fig. 3.5 shows a photograph of the transformer designed for two different working frequencies (50 and 100 kHz). As expected, by increasing the converter switching frequency the size of the magnetic components is reduced. The same applies to the capacitive filters. However, this potential benefit in

terms of mass and size is achieved at the expense of increased switching losses and the associated cooling requirements, unless proper expedients are adopted (such as soft-switching technique or better switching performance). Silicon carbide technology is a promising candidate to replace the silicon counterpart in this aspect.
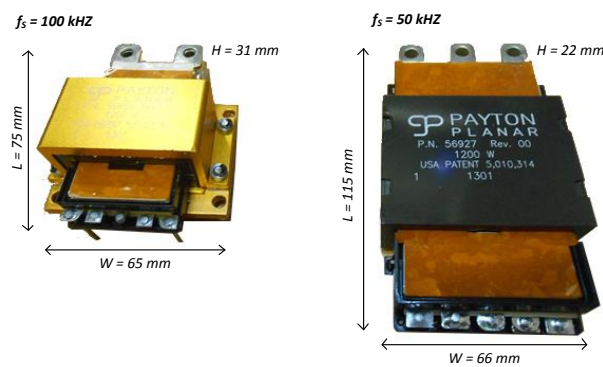
Figure 3.5: 1.2kW planar transformer with incorporated heat-sink.

Indeed, recent advancements in power device technology, in particular the availability of wide-band-gap (SiC) power MOSFETs, make possible to overcome this issue. Due to the inherently lower conduction and switching losses, higher switching power converters featuring SiC active rectifiers are feasible with significantly better efficiency. Additionally, the high temperature capability of the SiC is another advantage. As SiC MOSFETs can operate at high temperature without degradation of performance, heat sink size can be reduced. A side by side comparison between Si and SiC suitable power devices is summary reported in Table 3.2

The benchmark of several semiconductor devices shows that the best efficiency for the present application can be achieved by means of SiC MOSFETs (Rohm) at primary side and Opti-MOS3 (Infineon) at secondary side [1]. Thus, SCT2120AFC and IPA032N06N3G are respectively used, as indicated in Fig. 3.9. Both transistor types enable for the use of the body-diode as a freewheeling element for the current

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[1]Although the converter is intended for fully bidirectional operation, in this dissertation we refer to the 270V-side as the primary (input) side and to the 28V-side as the secondary (output) side.

Table 3.2: Characteristics of discrete commercial N-channel power MOSFETs .

Parameter		Q1	Q2	Q3	Unit
Drain voltage	V_{DS}	650	600	600	V
Drain-Source on resistance	$R_{DS(on)}$	120	190	290	$m\Omega$
Drain current (at 100°C)	I_D	20	13	13	A
Output capacitance	C_{oss}	90	1170	500	pF
Turn-on time	t_{on}	53	145	37	ns
Turn-off time	t_{off}	79	160	30	ns
Reverse recovery time	t_{rr}	33	610	240	ns
Maximum junction temperature	T_j	175	150	150	°C

Q1: SCT2120AFC (SiC), Q2: SPW20N60S5 (Si), Q3: STW20NM60FD (Si)

in the resonant tank, without the need for additional anti-parallel diodes. Moreover, both transistor types are avalanche rugged, capable of easily withstanding the dissipation of the typical energy levels stored in parasitic inductances prior to commutation and thus allow for reliable fully snubberless design of the converter. The simulations carried out at various loading conditions (for both forward and backward power directions) are presented in [35], and confirm that the losses in SiC devices are quite small compared to total semiconductor losses.

On the low-voltage/high-current secondary side, very large capacitance value is required to get proper voltage smoothing without the need for additional LC filters. The capacitance is implemented by paralleling a number of electrolytic and ceramic capacitors to achieve an optimum trade-off between volume/cost and performance.

3.2.4   Prototype

A 1.2kW 270V/28V bidirectional converter has been designed and realized. The BDC unit is composed of three main boards (Fig. 3.6):

- the Power Cell (PC), that incorporates all the power components of the dual active bridge converter, including the gate driver circuits and the sensors.

- the MicroController Module [2] (MCM), that manages external communications for the set up and the supervision of the BDC.

- the Converter Loop Controller (CLC), a fully FPGA-based control platform that receives commands from the MCM and drives the power board.
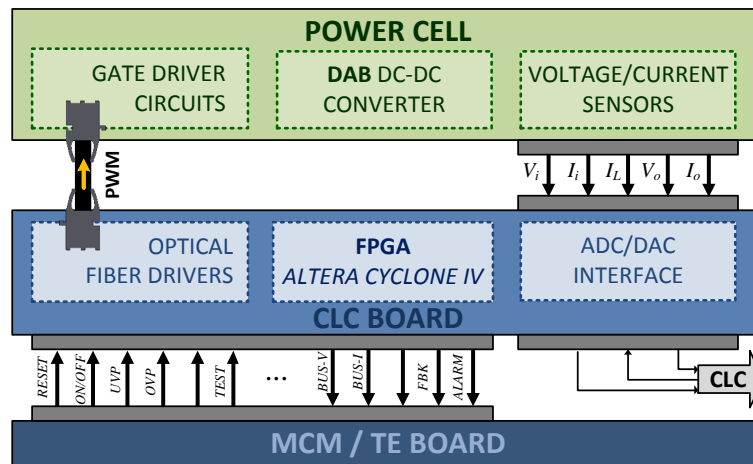
Figure 3.6: Block diagram of the BDC unit, with interconnections between boards.

The MCM (or TE) provides the high-level instructions (start/stop, reset, external fault, etc.) to regulate the converter behavior. The measured quantities on the power board are sent to the controller as electrical signals through a standard DSUB25 connector. Hence, a voltage and current transducers with current output (LV 25-P and

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[2]In order to reduce the system complexity, a Test Equipment (TE) board replaces it, during the preliminary characterization trials and for the control strategy assessment.

LA 55-P respectively) are opted for. Once these analogue feedbacks are acquired and elaborated by the CLC, the output command signals are transmitted to the power circuit via optical fibers in order to guarantee gate driver isolation and minimize EMC/EMI related problems. The controller board also sends back status data, and alarms or error messages in the event of failures.

Power cell

The power circuit is the fundamental part of the DC-DC converter. In addition to the power and voltage rating, the other design details and operating conditions are summarily listed in Table 3.3.

Table 3.3: Details of the DAB power circuit.

Attribute		Value	
Power rating	P_n	1.2	kW
Input Voltage	V_i	270	V
Output Voltage	V_o	28	V
Switching frequency	f_s	100	kHz
Trafo turns ratio	n	19:2	
Trafo leakage inductance	L_{lk}	7	μH
Series inductor	L_r	48	μH
Input Capacitor	C_i	540	μF
Output Capacitor	C_o	850	μF

Due to the complexity of the design and the number of components involved, and in order to ensure the maximum flexibility during the development stage, several boards were employed in the first realization. As illustrated in Fig. 3.7, the primary and secondary side power cells (i.e. the 270V and 28V full-bridges), are implemented on separate PCBs interconnected through the high-frequency transformer and the
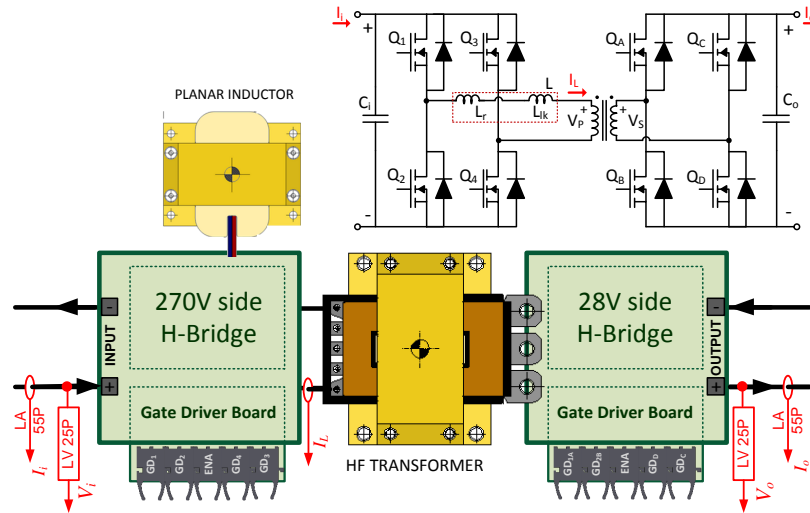
Figure 3.7: Schematic and assembly representation of the preliminary power board.

series inductor. In both PCBs, two semiconductor devices (one leg of each H-bridge) share a common heat sink, and no supplementary clamp or snubber circuit is added. Two gate driver boards, design on purpose for the device types (SiC MOSFET, Opti-MOS), acquire the command signals from the optical receivers and convert them into appropriate voltage levels to trigger the power devices (schematics in Fig. 3.8).
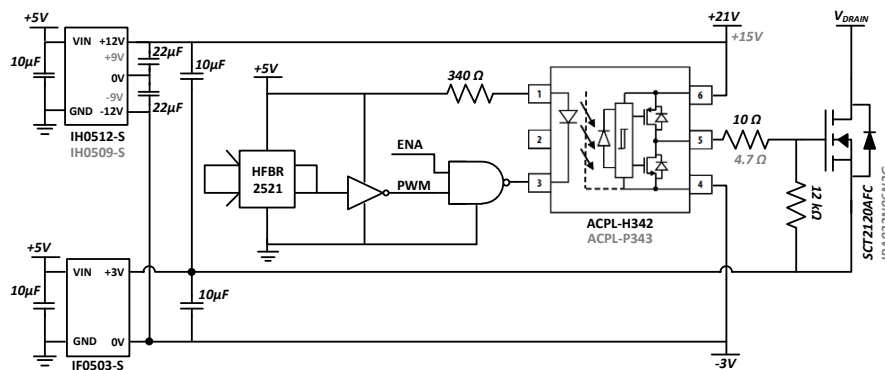
Figure 3.8: Gate driver circuits of primary (black) and secondary (gray) power cells.

In order to limit the stray inductance they are directly connected below the primary and secondary cells. In total, eight isolated gate driver circuits are used for the experimental prototype. An additional enable signal for each H-bridge allows to completely turn-off the full-bridge. All the sensors used for control strategy and protection aims are mounted on independent boards. Fig. 3.9 shows a photograph of the lab-prototype.
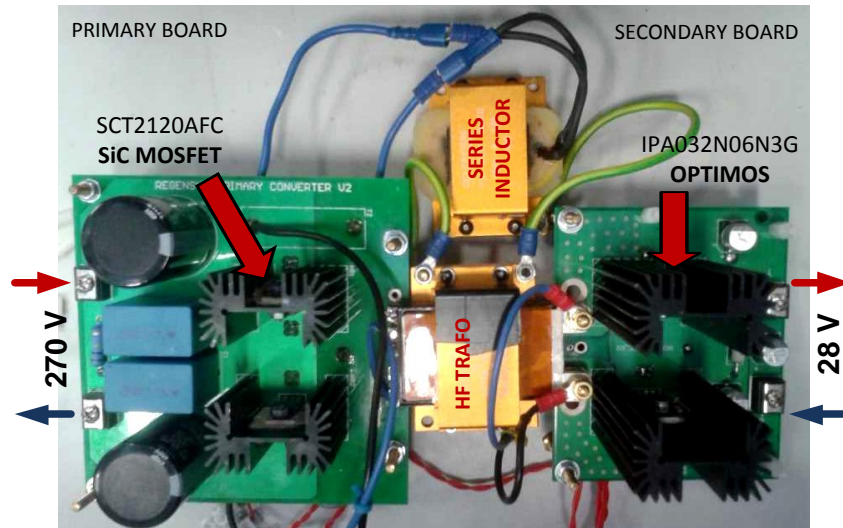
Figure 3.9: Preliminary prototype of the DC-DC power converter.

On the basis of the positive performance obtained in the characterization process, this converter has been re-engineered to a TRL 6 level, taking into consideration also safety and HW/SW certification factors. The final implementation is shown in Fig. 3.10. Beyond the optimized layout, the enclosing of the sensors, and the generation of the required power supplies on board, the major difference is found on the low-voltage side, where two devices are paralleled to better handle the high output current.
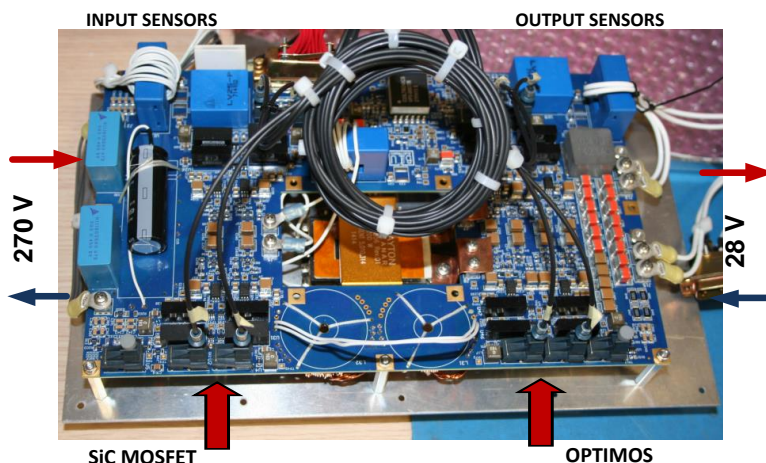
Figure 3.10: Final design of the power board (courtesy of BLU Electronic).

CLC board

The control board interfaces the MCM and the power module. It interprets the commands received and closes the control loop to ensure proper operation of the converter at its defined working point. It also provides data to monitor converter functional status and, in the event of an alarm, takes appropriate autonomous action to safeguard the system (e.g. power limit, shutdown, disconnect). The CLC platform is designed around the Altera CYCLONE IV (EP4CE40F23) FPGA, and embeds all the acquisition, conditioning, and elaboration circuits required.

On the basis of its functional tasks, the board might be divided into the following active blocks, as highlighted in Fig. 3.11:

- Control logic, that includes the FPGA and its supporting circuitries (power supply, JTAG FPGA/Flash programmer, internal reference).

- Power interface, that incorporates the Analog-to-Digital Converters (ADCs) with the associated conditioning circuits and the components to drive the optical transmitters with the PWM signals that control the MOSFET switching. In particular, six ADC ICs are mounted on the CLC, so that each sensor sig-

nal from the power board has a dedicated conversion chain and simultaneous sampling is feasible.

- MCM communication manager, that allows to receive configuration information and operating instructions from the external controller, and to give status data back. Since those signals could have analogue or digital nature, this portion of the PCB is equipped also with Digital-to-Analogue converters (DACs).

- CLC interface, to connect the board with another CLC card for paralleled units control purposes. As before, ADCs and DACs are employed to send/receive the key parameters (converters output current) for the operating activities regulation.
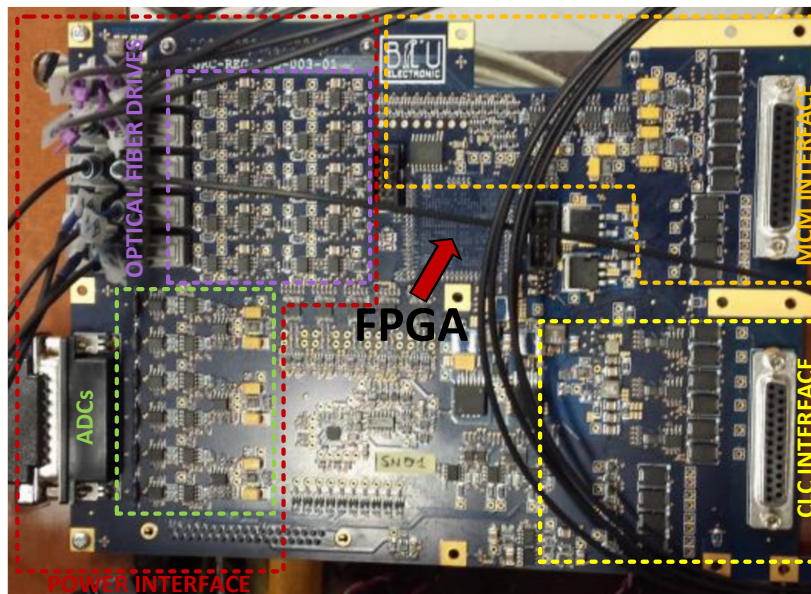
Figure 3.11: Converter Loop Controller (CLC), with the different section for power cell, and MCM/CLC interfaces in evidence (courtesy of BLU Electronic).

3.2.5 Experimental results

To practically assess the converter design, experimental results were obtained at different power transfer applying dc voltage at the input with a variable resistive load connected on the low-voltage output. Preliminary testings of the prototype were performed in open-loop configuration for both forward (from 270V to 28V) and backward (from 28V to 270V) power flow, by setting manually the proper phase-shift in the designated square-wave operating mode of DAB. The main waveforms displayed in Fig. 3.12 show the circuit working as expected by the simplified model in Sec. 2.3.
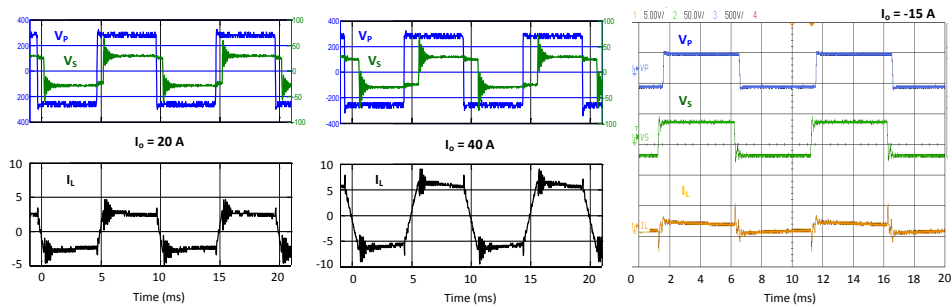
Figure 3.12: Phase-shifted voltages generated by the full-bridges and corresponding current through the transformer windings at different operating points.

Efficiency

Beyond the full functionality of the DC/DC converter, the efficiency is one of the most important attributes to check at the development stage. Poor efficiency translates into higher power dissipation which has to be managed on the circuit board. That is an critical issue, especially in demanding environments as avionic applications.

The experimental measured efficiency within the operating range is shown in Fig. 3.13. The converter operates above 90% efficiency for most of the operating conditions, with a peak of 95% at 300 W. This performance is quite invariant with the direction of power flow.
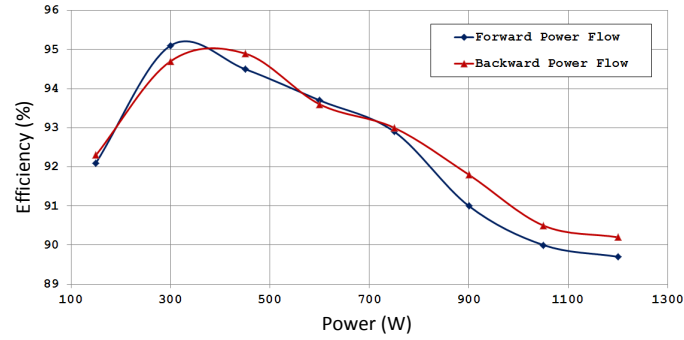
Figure 3.13: Measured efficiency of the prototype all over the operating range.

The behavior under different load conditions (at nominal input voltage $V_{in} = 270V$) or for variable input voltages (at half load) are briefly reported in Table 3.4.

Table 3.4: Measured efficiency on the laboratory prototype.

Load[1]	Efficiency	V_{in}	Efficiency
12.5%	92.1	235	91.4
25.0%	95.1	240	92.0
37.5%	94.5	250	92.6
50.0%	93.7	260	93.3
62.5%	92.9	270	94.0
75.0%	91.0	280	94.4
87.5%	90.2	290	94.7
100%	89.9		*(at 600 W)*

[1] Normalized to 1.2 kW nominal power

The efficiency obtained in the final realization of the converter is typically around 94% with still some margins for improvement in a future design iteration.

ZVS turn-on

The DAB converter is designed to operate within the soft-switching range, in a fully snubberless arrangement. For the present application, ZVS technique is exploited. The natural resonance phenomenon that allows to achieve non-dissipative turn-on of the power MOSFETs, involves the transformer leakage inductance and the intrinsic capacitance of the power devices. Fig. 3.14 shows the measured drain-source and gate-source voltage waveforms at the primary and secondary side devices, that demonstrate the desired soft transition. During the commutation event, the diode conduction occurs before the transistor is switched on.
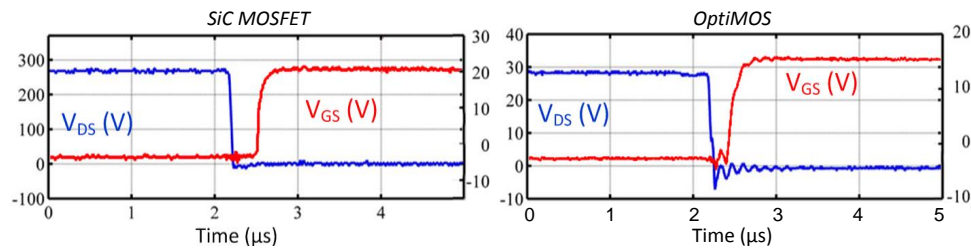
Figure 3.14: Experimental results of the DAB converter: turn-on transient waveforms of primary and secondary power devices. The switch voltage is actually brought to zero before gate pulse is applied.

3.3   Control design

The objective of the bidirectional converter is to satisfy the power demands of generic loads and actuators in the forward power flow mode, and effectively transfer the power extracted from the regenerative sources to the high-voltage bus in the backward configuration. In both situations, the BDCR unit takes care of the high-voltage DC bus regulation to maintain the desired reference (270 V), while the BDC unit is responsible of keeping the low-voltage constant at the nominal value (28 V), regardless of the output conditions and load variations.

Since DAB converters have been widely employed in high-power architectures,

several switching methods to control the operating modes have been proposed and discussed in literature. Triangular modulation (TRM) and Trapezoidal modulation (TZM) [36] focuses on minimizing the current at turn-off instant of switching devices to reduce the switching loss. [37] show how circulating currents and transformer RMS current during normal operation can be reduced, by choosing an optimal modulation scheme. Other works regard the extension of the ZVS range [38], [39] or the improvement of the poor light-load efficiency [40], [41], and so on. Among those different strategies, the phase-shift modulation allows for the highest power transfer and has been preferred for the specific application.

The control scheme is outlined in Fig. 3.15. The measured output voltage (V_o) is compared with the reference value and the difference applied to the PI voltage controller that adjusts the phase-shift between primary and secondary square voltages to reduce the error. The result is fed as an input to the PWM modulator, that in turn produces the proper switching pulses to control the full-bridges semiconductor devices and closes the loop. A supplementary feed-forward compensation based on analytic evaluation is added up to improve the system response. This method both applies to forward and backward power flow.
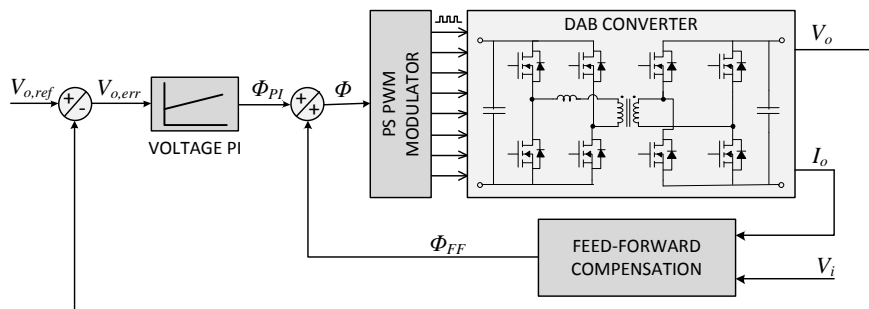
Figure 3.15: Block scheme of the phase-shift PI based voltage control for the dual active bridge converter, with feed-forward correction.

To effectively design the closed-loop control and predict its performance before practical implementation, the whole system (including power circuits and discrete-

time controller) has been broadly simulated using PLECS toolbox in Matlab/Simulink environment, as shown by the subsequent sections.

Voltage PI controller

According to the model derived in Sec. 2.3.3 and Appendix A, the converter behavior depends on the load conditions as expressed by the mathematical representation of the relation between the output voltage and the phase-shift variable. Fig. 3.16 shows the transfer function of the plant $G_{DAB}(s)$ at different current loadings.
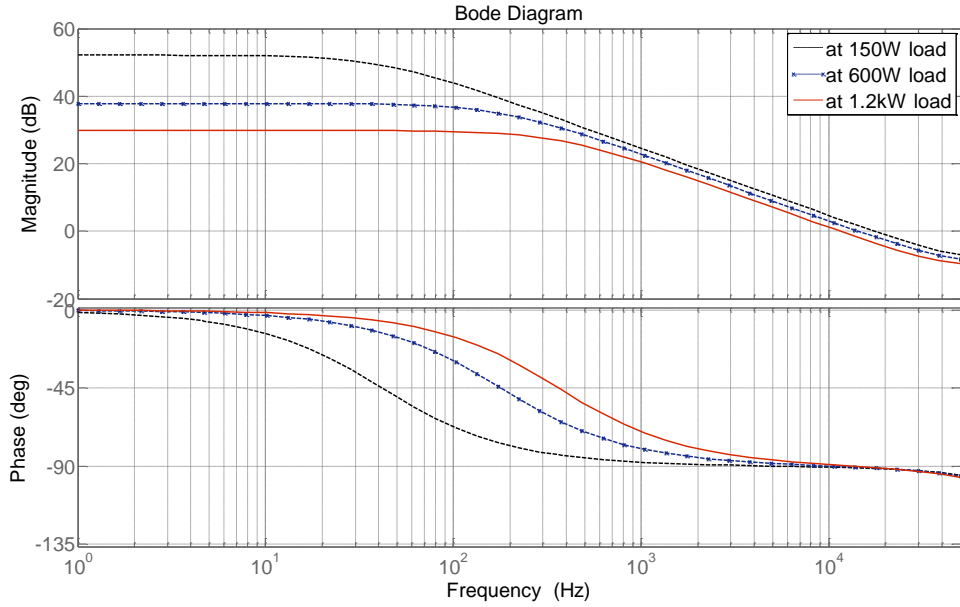
Figure 3.16: Bode plots of the plant at various resistive loadings.

The voltage loop with the PI regulator is sketched in Fig. 3.17, where $G_{PI}(s) = K_P + K_I/s$. In principle, the proportional and integral parameters can be straight derived to obtain the desired system bandwidth (ω_c) and phase-margin (ϕ_M), as outlined below:

$$\begin{cases} K_P = \frac{1}{|G_{DAB}(j\omega_c)|} \cdot \cos(\vartheta) \\ K_I = -\frac{\omega_c}{|G_{DAB}(j\omega_c)|} \cdot sin(\vartheta) \end{cases} \quad \text{where } \vartheta = -180 + \phi_M - \langle G_{DAB}(j\omega_c) \rangle \qquad (3.1)$$

However, once those values are defined, the bandwidth of the converter remains no longer unique for a variable output condition. To overcome this problem and keep the bandwidth constant the proportional gain might be tuned with the variation of load current and input voltage [42]. Nevertheless, a conventional PI controller with fixed gains is still preferred to avoid additional control efforts and stability issues. A different strategy is exploited to limit the overshoot and improve the transient response under variable loadings, as explained in the next section.
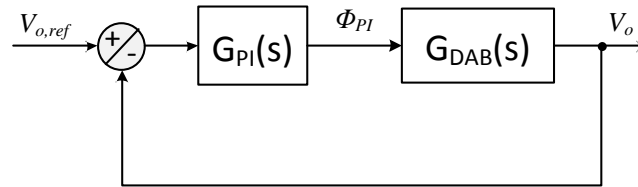
Figure 3.17: Simplified block diagram of the feedback voltage loop.

Three likely design examples of the PI regulator are summarized in Table 3.5, while Fig. 3.18 illustrates the Bode diagram of the closed-loop system at various power ratings with the proportional and integral gains as in the second column.
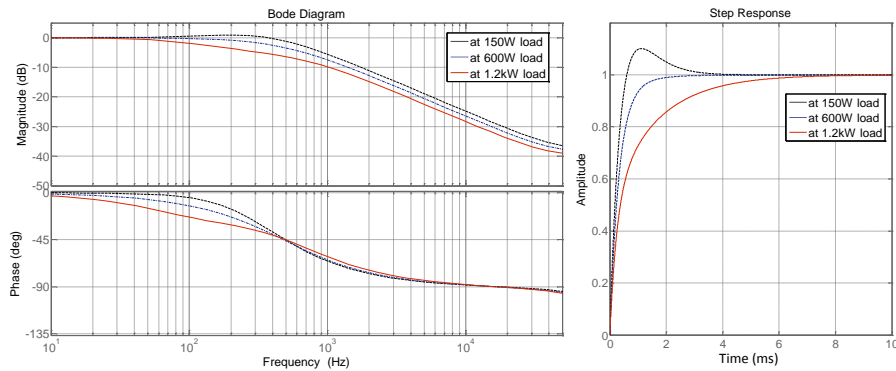
Figure 3.18: Bode plot of the voltage loop and system step response at different power ratings ($K_P = 0.033$, $K_I = 34.9$).

Table 3.5: Voltage loop performance for different PI controller design.

P (W)	BW (Hz)	PM	BW (Hz)	PM	BW (Hz)	PM
0	112	77.2°	588	78.2°	1192	90.5°
240	68	102°	527	84.8°	1078	94.5°
480	35	104°	456	92.5°	958	99.3°
720	22	101°	374	101°	840	105°
960	15	99.1°	290	109°	737	112°
1200	12	97.6°	225	114°	677	118°
	$K_P : 0.006$	$K_I : 2.74$	$K_P : 0.033$	$K_I : 34.9$	$K_P : 0.07$	$K_I : 12.5$

BW:BandWidth, PM:Phase-Margin

The approach of using step-load responses has been used to verify the proper design of the feedback compensation. Fig. 3.20 and 3.19 show the converter experimental response to abrupt output current steps, adopting the same PI parameters. Fluctuations on the output voltage can be observed in correspondence of the instantaneous current variations, but the controller exhibits the expected behavior in terms of time reaction and stability.
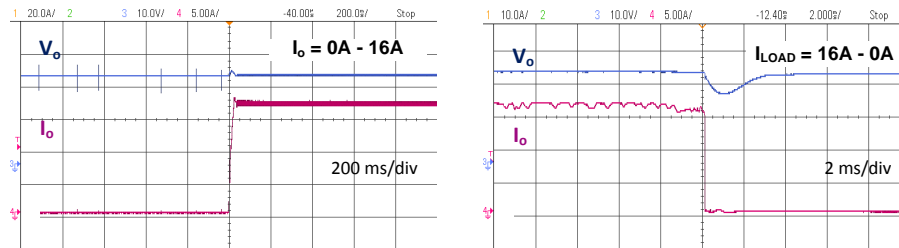
Figure 3.19: Converter transient response in regenerative configuration, when current changes from 0 A to 16 A, and vice versa.
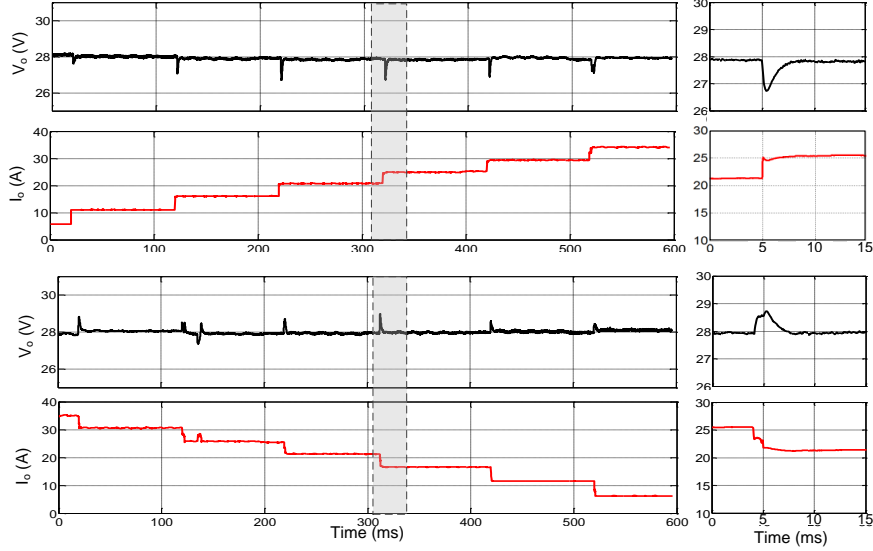
Figure 3.20: Experimental results of converter transient response, increasing or reducing the delivered power by ± 5 A current steps.

Feed-forward compensation

In order to reduce the sensitivity of the system to the load variations and mitigate the drawbacks of PI regulator, a feed-forward compensation term is included in the control loop. The sensed electrical quantities (input voltage and output current of the converter) are employed to evaluate the disturbances and to account for them before they have time to affect the system. The value of this estimated phase-shift ratio for each operating point can be arithmetically derived from Eq. 2.7, as follows:

$$\phi_{FF} = \frac{1}{2} \cdot \left(1 - \sqrt{1 - \frac{8nf_s LV_o}{V_i R_o}} \right) = \frac{1}{2} \cdot \left(1 - \sqrt{1 - \frac{8nf_s LI_o}{V_i}} \right) \qquad (3.2)$$

If all the parameters involved are known, the PI controller behaves only as auxiliary modulator and balances the difference between the compensation factor (ϕ_{FF}) and the required phase-shift (ϕ) to drop the voltage steady-state error to zero. Although its contribute is limited, the presence of the PI is mandatory. The feed-forward

value, indeed, has an intrinsic inaccuracy due to the model simplifications and the error inherent in discretization. Moreover, the unavoidable sampling delay affects the time for the system to react. Fig. 3.21 shows the effect of the load current feed-forward. As expected, the inclusion of this correction term improves the transient response, ensuring faster reactions to load or input voltage variations. Through this strategy, the output ripples during load current changes are small compared to those in case of only voltage loop, even in case of a transition from regenerative to forward power flow (Fig. 3.22). The same smoothing effect can be observed for variations of the high voltage bus. That limits the overshoots and avoids overcoming the safety thresholds during normal operation.
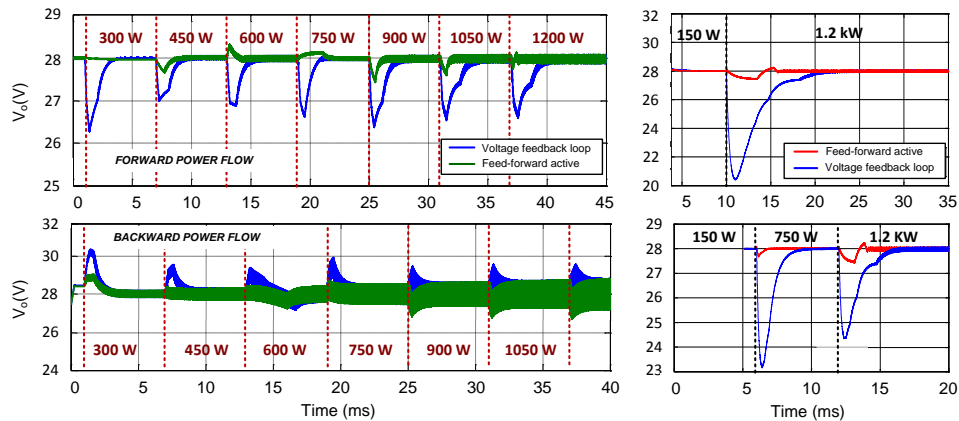
Figure 3.21: Simulations of converter step response with or without feed-forward compensation. On the right, transitions for different output current variations.

Some examples of experimental measure are plotted in Fig. 3.23. Tests on lab-prototype confirm the foreseen benefits with consistent performance for both directions of power flow. In conclusion, the presence of this additional element is profitable and enables the converter to promptly manage large and rapid changes of power demand without unacceptable rising or falling of the voltage on the 28V bus.
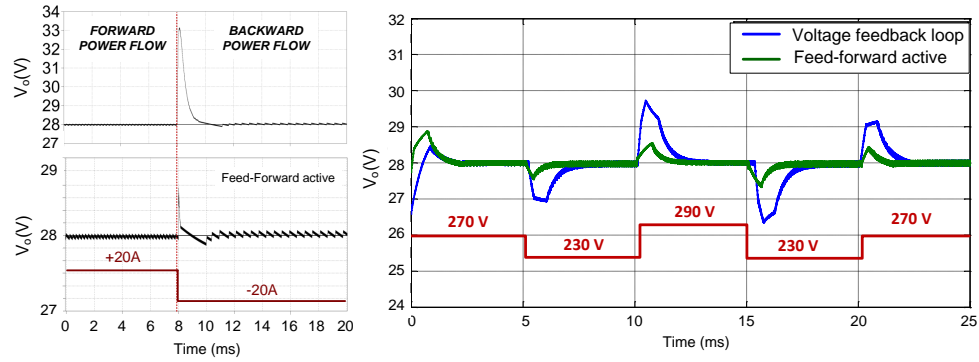
Figure 3.22: Simulations of converter behavior: rapid transitions from regenerative condition to forward power flow and response to oscillations of input voltage.
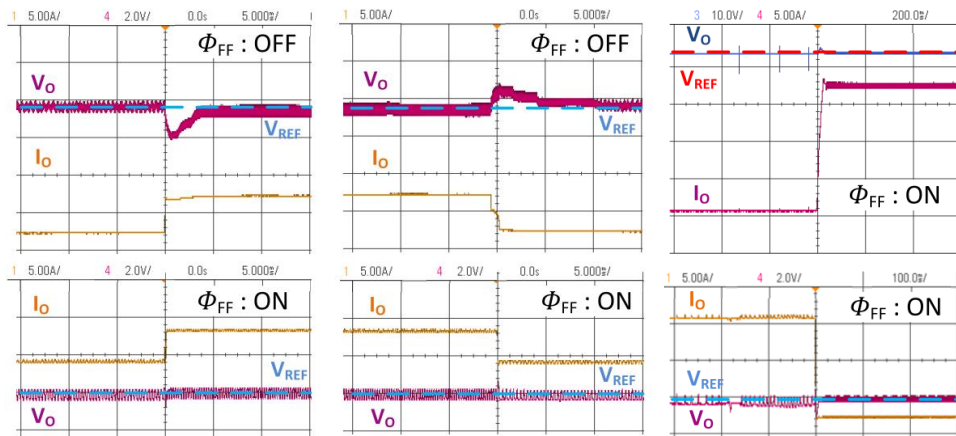
Figure 3.23: Scope acquisitions of closed loop control for abrupt steps of $\pm 5A$, and converter response to $\pm 15A$ load current changes when feed-forward term is enabled.

3.3.1 Soft-starting procedure

A downside of the DAB topology is the starting issue. When the converter is firstly switched on, the uncharged capacitors act as virtual short circuits allowing the current to rapidly escalate. At the initial stage, the circulating current is not determined

by the controllable phase-shift, but only by the peripheral circuit and its peak value is directly proportional to the equivalent input voltage. Therefore, in high-voltage and high-power applications, the starting process with rated input voltage and zero initial output voltage is not feasible unless additional circuits [43] or advanced control algorithms are integrated [44], to mitigate the effect of the inrush current at turn-on.
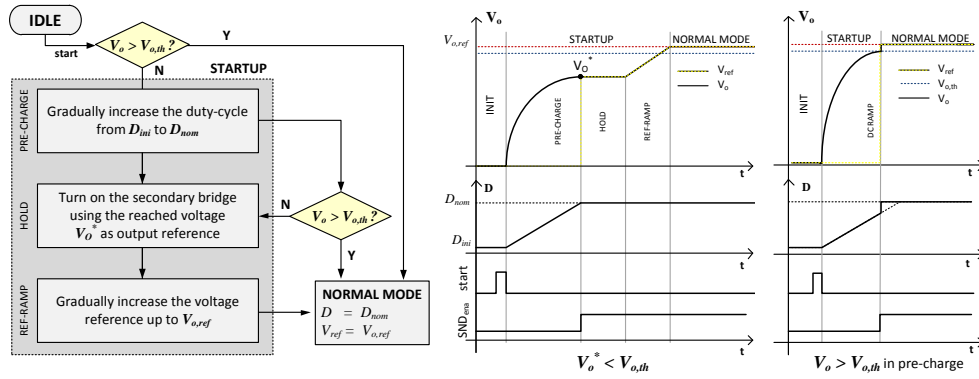
Figure 3.24: Flowchart of the start-up procedure and main associated waveforms.

The implemented method is based on Dual Phase-Shift (DPS) control [45]. A detailed description is given in [46]. The operations sequence is briefly depicted in Fig.3.24 and can be divided in three intervals. At the beginning (*PRE-CHARGE*), the secondary bridge is kept off and the output capacitors are charged, gradually increasing the phase-shift applied between the legs of the high-voltage bridge. In particular, the duty-cycle on primary side slowly rises from a relatively small quantity (D_{ini}) to its rated value (D_{nom}), as defined in (3.3), where T_{su} is the time that let the duty ratio increase up to the nominal value.

$$D = D_{ini} + \frac{D_{nom} - D_{ini}}{T_{su}} \cdot t \tag{3.3}$$

During this pre-charge event, the output voltage is built up only by the secondary side body diodes, and the established value (V_o^*) depends merely on the load. Then (*HOLD*), the secondary switches are turned on and the closed loop control is activated to keep the output voltage at the reference value, which is, initially, the attained output voltage. If the feed-forward correction is working, the transition goes smoothly:

no large voltage drop occurs (Fig. 3.25). Finally (*REF-RAMP*), the set-point is incremented till the rated value ($V_{o,ref}$), as formulated in (3.4), where T_{ref} is the imposed ramp time.

$$V_{ref} = V_o^* + \frac{V_{o,ref} - V_o^*}{T_{ref}} \cdot t \qquad (3.4)$$

In the event of exceeding a safety threshold ($V_{o,th}$), the system is suddenly forced to the normal mode, where both the duty-cycle and the voltage reference are set at the nominal values.
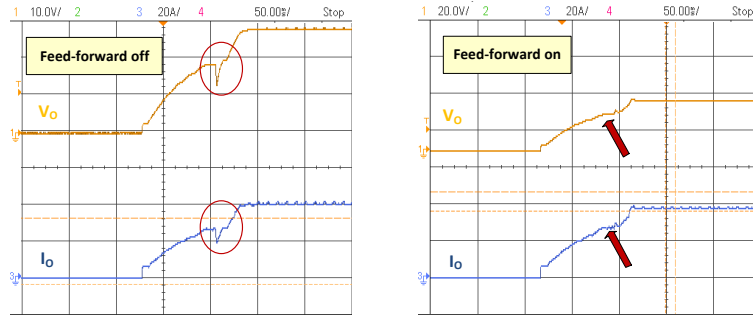
Figure 3.25: Experimental turn-on of the converter through the proposed strategy (at 1.2 kW). With the feed-forward term on, the transition when the closed-loop control is suddenly activated does not affect the low-voltage bus.

Simulations are shown in Fig.3.26, while the primary and the secondary bridge equivalent circuits at different startup instants are depicted in Fig.3.28. The proposed strategy for the safe turning on of the DAB converter is feasible under all the load conditions (ranging from 0 to the maximum power), as proven by the empirical results in Fig.3.27. At last, it is worth to be noted that this method is implemented entirely by digital control, so no additional circuitry is required.
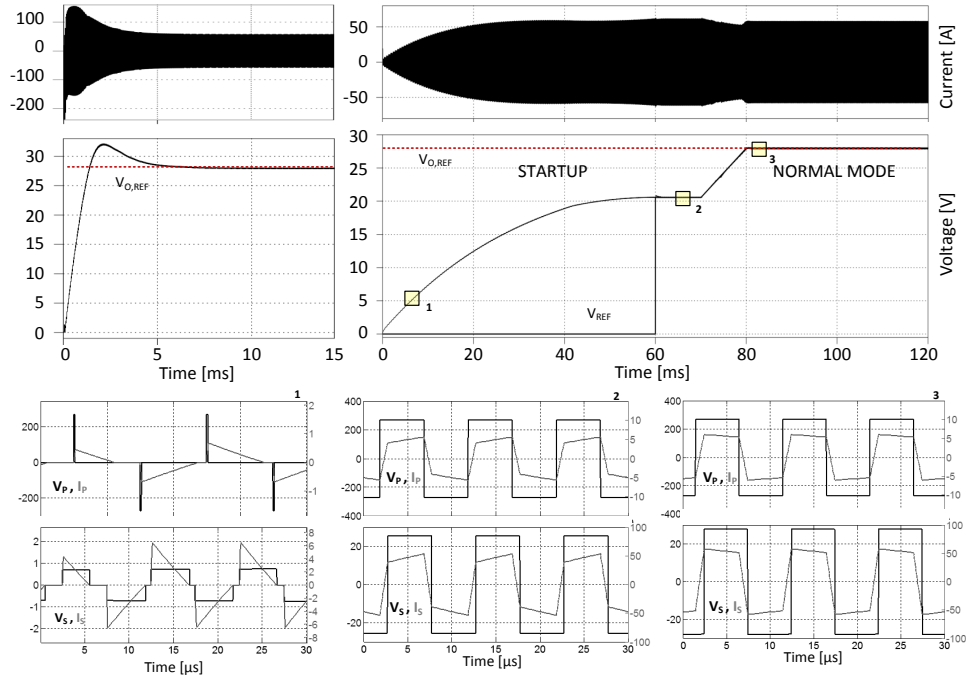
Figure 3.26: Converter turn-on under heavy-load condition (1.2 kW) and transformer waveforms in each phase of the soft-starting process. By using this procedure, the critical inrush current is significantly reduced.
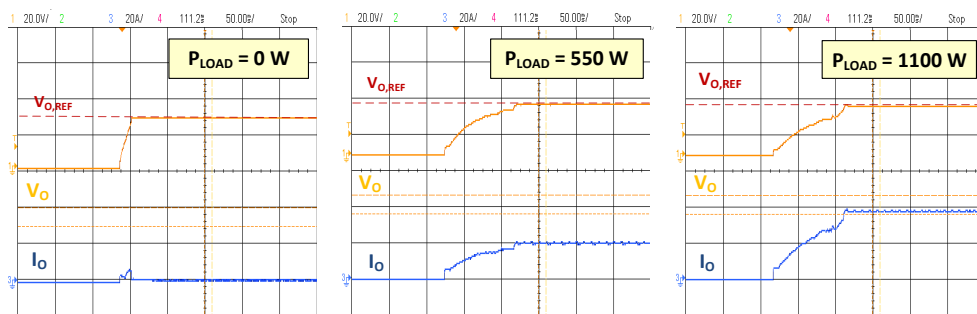
Figure 3.27: Soft-starting transient for different power ratings (at $V_{in} = 270V$).
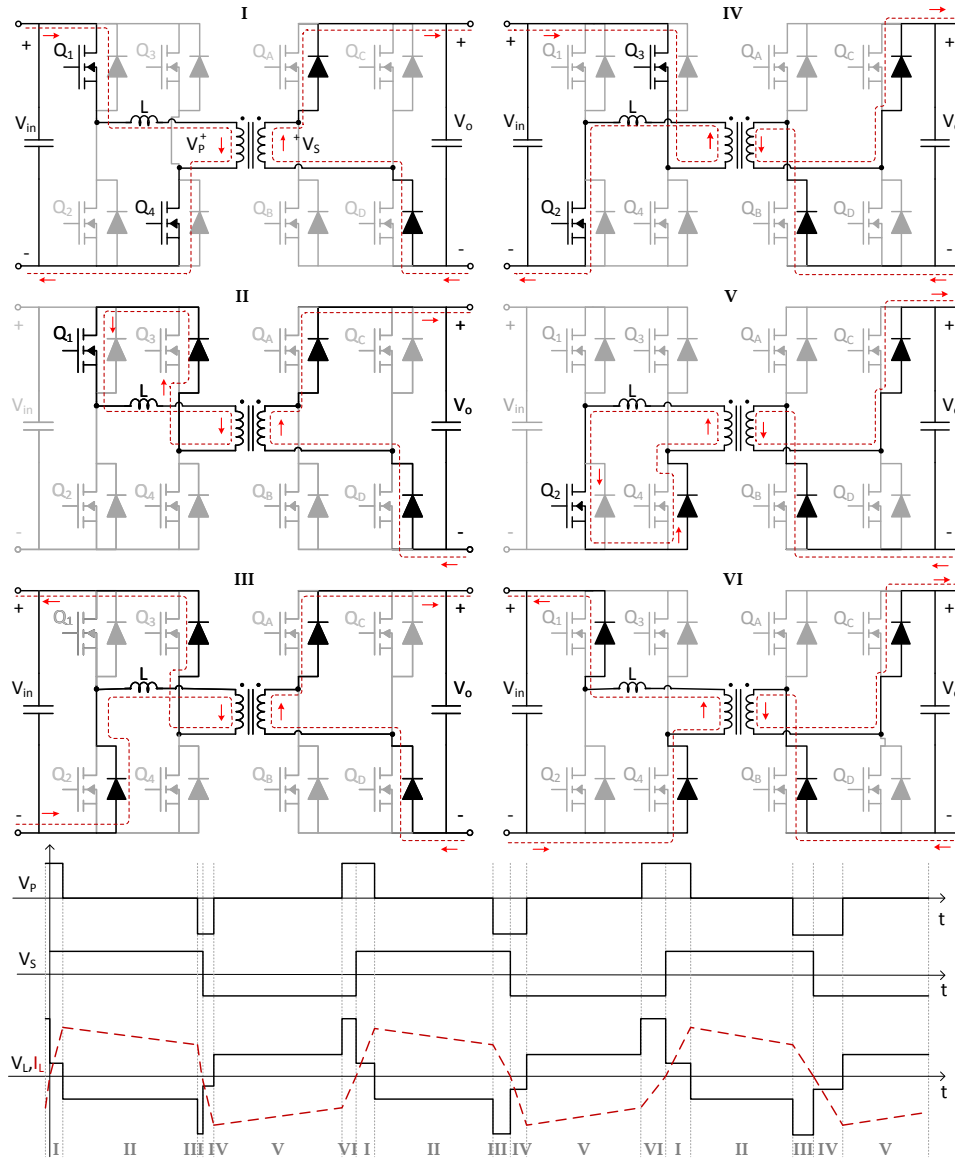
Figure 3.28: Equivalent circuits and idealized operating waveforms during the pre-charge stage. In this phase the secondary power devices are disabled and the output capacitors are charged only via the body-diodes.

3.4   Parallel operation

In order to achieve a flexible and modular power distribution architecture, the parallel operation of several converters should be taken into consideration with the aim of increasing the overall capability of delivering power. The parallel connection of two BDC units directly linked to the load (Fig. 3.29) is discussed in [47].
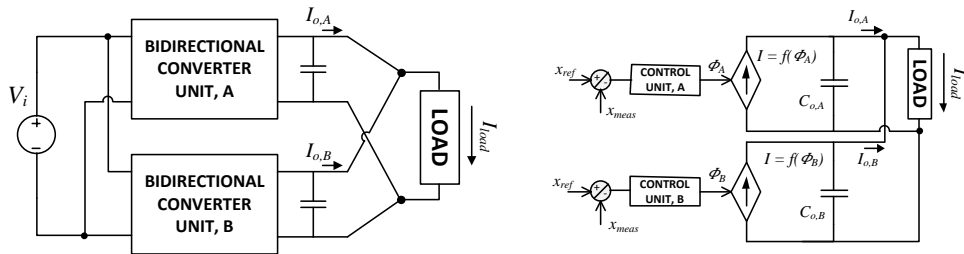
Figure 3.29: Parallel connection of two BDCs and simplified equivalent model.

In that configuration, the objective of the control is to maintain the low-voltage bus constant and actively share the power demand among the modules. The critical point of the control strategy, indeed, is to guarantee a balanced operation of the different power converters. Theoretically, BDC units are able to perform parallel operations without any further control, due to the DAB inherent gyrator characteristic [48]. The same phase-shift could be simply applied on both converters or each control loop could regulate the load output voltage in a concurrent manner. Simulations and laboratory trials with this settings are shown in Fig. 3.30 and 3.31, respectively. Assuming ideal conditions, the power is equally split between the units, but this process only occurs if the converters are identical and the boundary conditions exactly the same. In practice, as a small difference perturbs the system, there is no way to balance the converters efforts again. As it can be observed, undesirable issues related to the bidirectional nature of DAB topology could also arise if the operating working point is established with the converters running in opposite configurations (i.e. sinking or sourcing current). In this worst case scenario, the paralleling of two units is not only worthless but even potentially harmful. For those reasons, a technique is needed to

ensure converters work properly together. In this framework, two strategies to achieve uniform power distribution have been developed and assessed.
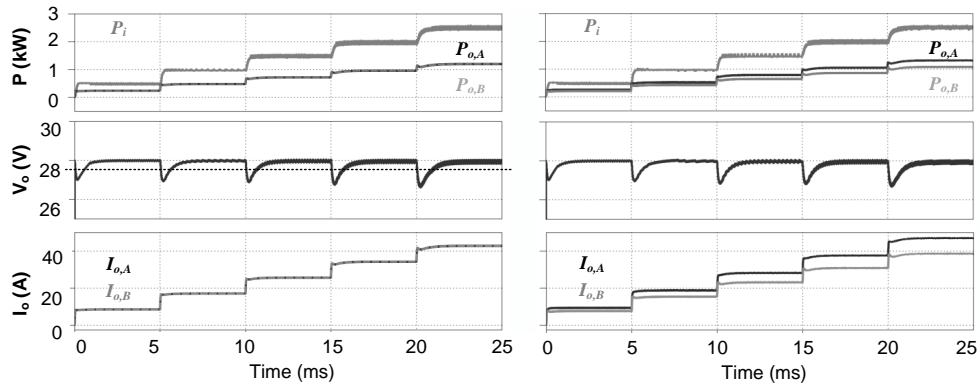
Figure 3.30: Simulations of BDC units in direct parallel configuration without any additional control. The power sharing is fully balanced only if the two converters and the boundary conditions are exactly alike (image on the left).
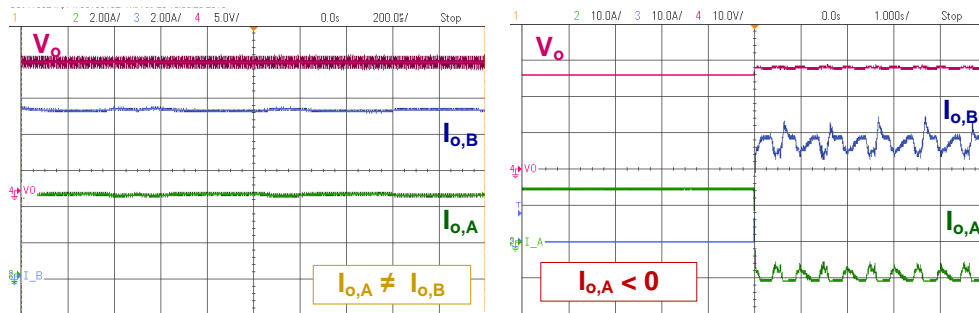
Figure 3.31: Experimental results of BDC units in direct parallel configuration without any additional control. The scope acquisitions point out two expected undesired behaviors: unbalanced output currents (on the left) and incoherent power flow directions (on the right).

3.4.1 Current sharing

The block diagram of the current sharing strategy is outlined in Fig. 3.32. The approach used in this scheme is based on decoupled control loops: one converter (*MAS-TER*) focuses on keeping the output voltage constant, employing the same method explained in the previous section, the other one (*SLAVE*) is responsible for the power division, working in current control mode. The voltage controller is disabled and the master output current is fed as the set-point of the slave feedback-loop to determine its phase-shift. The feed-forward additions could be provided similarly for both modules.
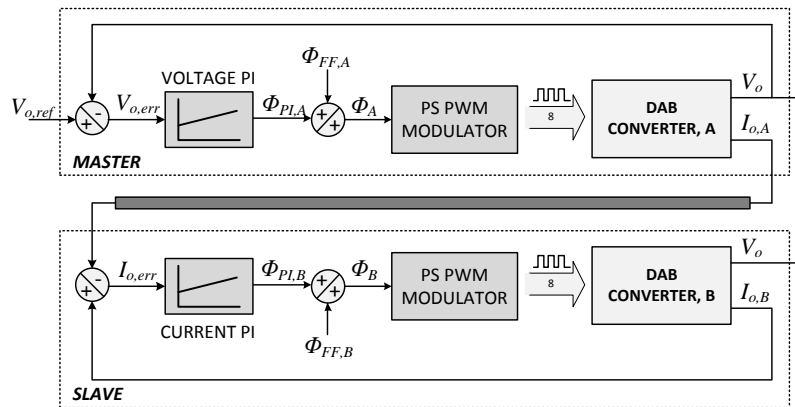
Figure 3.32: Output voltage control scheme of two BDC units in parallel, with current compensator. The output current of each converter is measured and a communication channel is employed to share this information.

The proposed method has been firstly validated by means of simulations. As shown in Fig. 3.33, the difference between the remote ($I_{o,mst}$) and the local ($I_{o,slv}$) output current is brought to zero and the system can accomplish the dynamically partitioning of the delivered power among the two units, under variable load currents.

Results acquired on the lab-prototype are presented in Fig. 3.34, for different power requests. The tests carried out are in close agreement with simulations: the energy distribution is realized as expected and the low-bus voltage is well regulated.
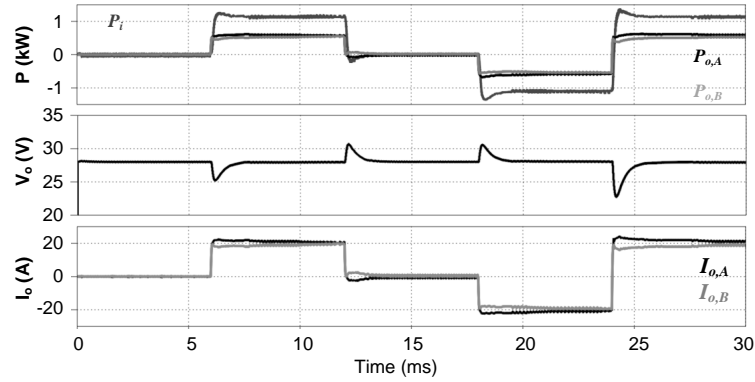
Figure 3.33: Simulations of paralleled units in current sharing configuration (delivered power, output voltage and currents).

The main benefit of this method are the fully controllable load sharing and the great accuracy obtained in a relatively simple manner. Despite of this, the need to exchange information between the power converters is the intrinsic limit of this strategy, especially if several modules are involved and a fast response is wished for. The loss of the communication link or a failure of the master block can shut down the whole system.
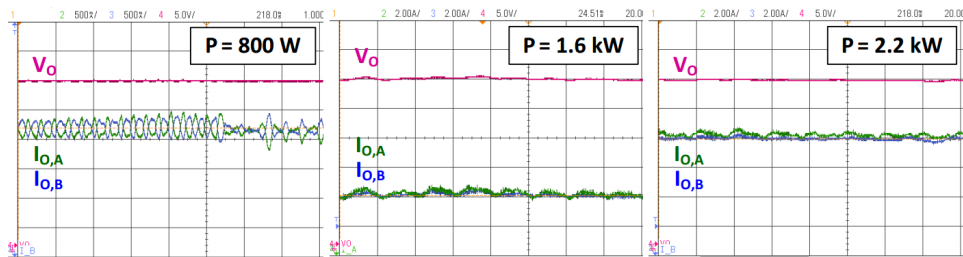
Figure 3.34: Experimental measurements acquired at different loadings, employing current sharing parallel method.

3.4.2 Droop control

The droop compensation feature could be another suitable solution to enable parallel connection and to allow actively power sharing among the DABs. This technique is a well-known practice commonly used for primary frequency control of grid-connected generators. The same logic can be applied to voltage control and can be easily implemented in this distribution network without any additional circuitry. The structure of the proposed strategy is illustrated in Fig.3.35.
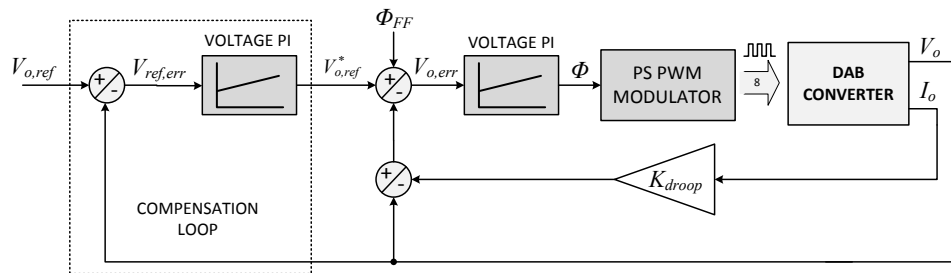
Figure 3.35: Overall block diagram of the voltage-droop control strategy, including the voltage reference compensator.

The concept is to add a virtual resistor (K_{droop}) into the feedback loop, which drops the internal voltage set-point ($V_{o,ref}$) as a linear function of the output current (I_o), $V^*_{o,ref} - K_{droop} \cdot I_o$. Thus, the voltage droop characteristic can be interpreted as a negative slope in the converter I-V plane: when supplied current decreases, the output voltage is allowed to increase to counteract the reduction in current, and vice versa.

In parallel configuration, this behavior promotes the power sharing between converters, without the need of a central control. Since the total current is imposed by the load, if one module drives a higher current, the other one output tends to decrease. The emulated impedance reflects this variation on a proportionally higher voltage set-point, that in turns produces a greater output current. At last, the units will settle at a steady-state where the contributes are balanced. Therefore, the droop control allows multiple generating units to share the load by automatically changing their op-

erating points. More important, each converter exhibits a self-balancing attitude by using only local information (i.e. output voltage and current), so it is not necessary for the single unit to be aware of the other elements in the system, and communication channels between modules could be abolished.

The voltage control operates as for the single module. A falling (rising) voltage indicates an increase (reduction) in loading and a request for more (less) delivered power. Parallel converters with the same droop controller respond to the fall (or rise) in voltage by increasing (or reducing) their output power simultaneously. An external PI-based loop is added to completely remove (or at least reduce) the undesired effect of a steady-state error on the regulated voltage. Simulation outputs for the proposed control strategy are shown in Fig. 3.36 (voltage compensation) and in Fig. 3.37 (power sharing). A low-pass filter is used to cut-off harmonic frequencies and fast oscillations of the sensed current.
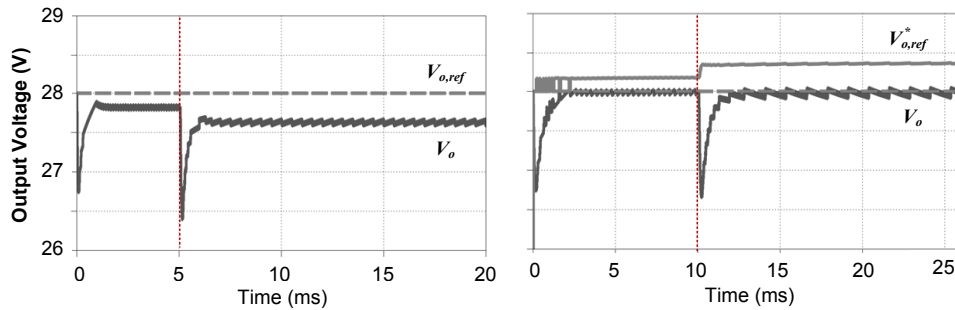
Figure 3.36: Effect of the reference feedback compensation on the output voltage.

Voltage droop-control have been employed on parallel BDC units with favorable outcomes (Fig. 3.38). Moreover, as the ratio of the droop coefficients is directly related to the amount of current flowing in each module, a dishomogeneous power distribution is also achieved, simply adopting different virtual resistors for each module.
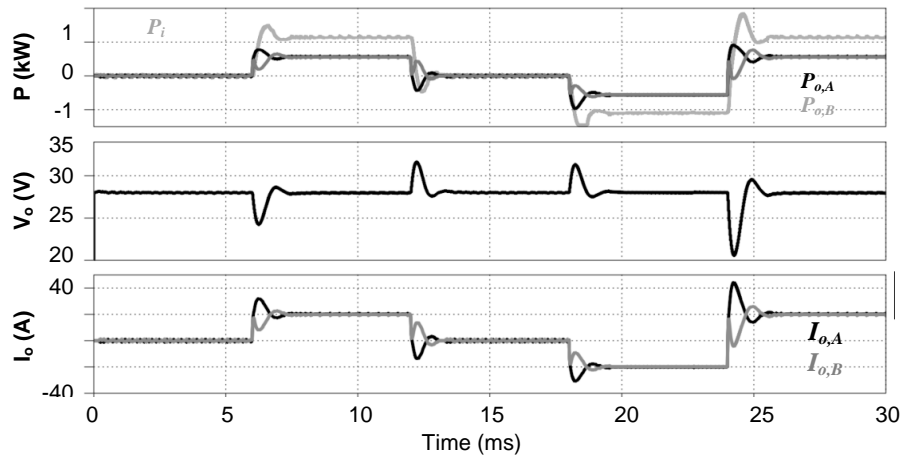
Figure 3.37: Simulations of BDC units working in parallel to supply a generic load. The proposed voltage droop method intrinsically equalizes the power flow between the two converters.
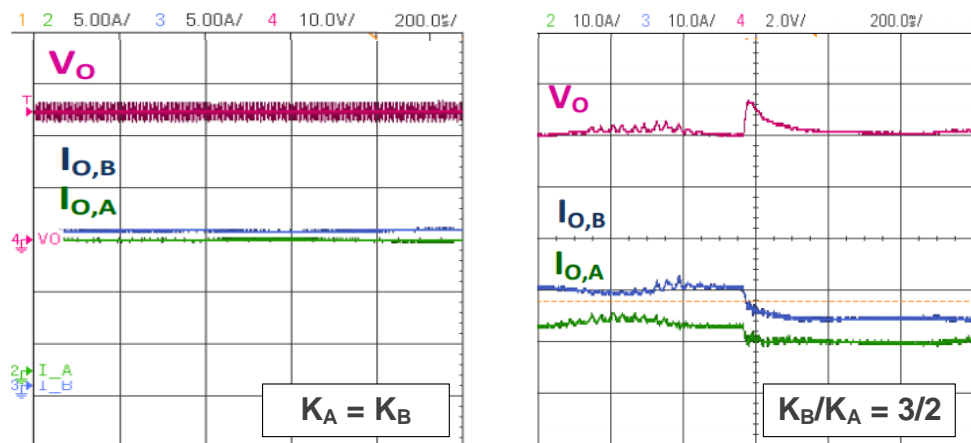
Figure 3.38: Experimental results of droop control strategy, adopting equal (on the left) or different (on the right) virtual resistors for the BDC units parallel connected.

3.5 FPGA implementation

The development of Field Programmable Gate Array (FPGA) over the last years provides a valid alternative for the implementation of digital control systems, previously dominated by the general purpose microprocessors. As mentioned above, in this application the whole firmware including the feedback loop and all the algorithms functional to the supervision objectives, the interface with external boards, and the safety tasks are embedded in a low-power consumption Altera Cyclone IV (EP4CE40F23) FPGA, clocked at 50 MHz. A fully FPGA-based control is preferred to other programmable platforms for reliability reasons (all the actions are embedded in physical logic circuits instead of being performed at software level) and higher processing speed (by their nature, FPGAs allow for true parallel processing, supporting multiple threads that execute in a concurrent manner). Moreover, FPGAs are not bound by the architecture (although logic cells are fixed, the functions they perform and the interconnections are determined by their code) hence, all the available resources and the hardware structure are completely programmable according to specific requirements. On the other hand, the most common peripherals for the control of high-switching frequency DC-DC converters, such as PWM modulators, ADCs circuits, standard communication protocols (I2C, SPI, etc.), are not integrated into the chip and they must be designed at hardware level from the ground up. This section describes how the main functional blocks are implemented into the FPGA architecture. Many possibilities exist to (hardware) realize these functionalities. The chosen methodology is to write all the entities needed using a generic abstract Hardware Description Language (HDL). This approach ensures flexible adaptation of each module to various control aims, and allows to replace the programmable platform without any additional issues. For design choice, all the variables involved in the closed-loop control are normalized and represented with 16-bit resolution in the signed Q15 common format.

3.5.1 System overview

A schematic description of the overall code at the highest abstraction level is given in Fig. 3.39. According to the functionality of each block, the firmware design may

be subdivided into the following active areas.
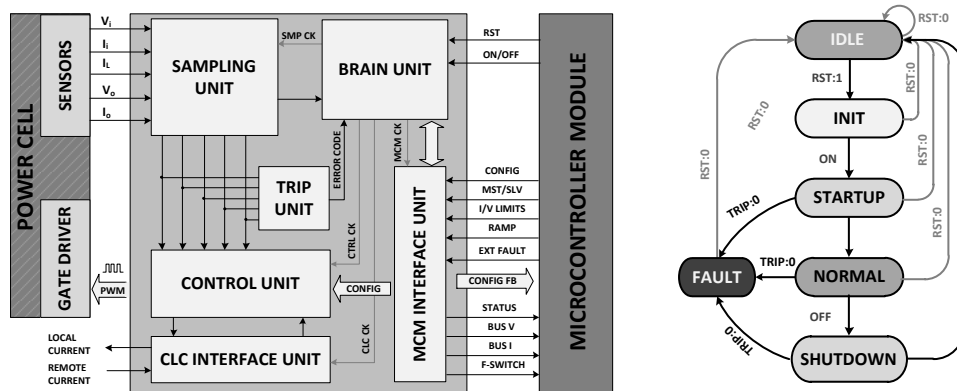
Figure 3.39: Firmware graphical representation with partition in functional sections and basic chart of the primary finite state machine.

The *Brain Unit* executes the main routine and manages all the interrupts services, by setting the priority assignment and providing the synchronization signals to all the major tasks. These different processes are carried out by independent threads in a concurrent manner, but every update of the output is globally synchronous with the PWM interrupt.

The *Sampling Unit* takes care of the acquisition of the analogue measures that come from the voltage and current hall sensors, which are located on the power board. These bidirectional ±50mA current signals are translated into positive voltage $(0 \div 3$ V$)$ by conditioning circuits and then converted into digital values through external ADC ICs (LTC1407). The entity provides the Serial-Protocol-Interface (SPI) required for the communication with those peripherals and employs versatile moving average filters to reduce the noise of the acquired signals. The measured quantities are finally normalized by proper scaling factors and then sent to other units.

At every acquisition, the *Trip Unit* compares the electrical measurements from the power cell with the guard thresholds to check if a malfunctioning or fault condition occurs. In this circumstance, the converter is turned-off to prevent inadvertent

damages on the system, and the supervision controller is made aware of the error detected.

The ***Control Unit*** runs the algorithms to close the feedback loop, and handles the optical fiber transmission of the PWM signals that drive the MOSFETs of the power converter. The digital output voltage signals (0/3.3V) coming from the FPGA are converted into the proper currents (0/40mA) needed by the fiber transmitters (HFBR-1531ETZ). The BDC unit is capable of working in two operating modes: stand-alone or parallel arrangement, with several configuration options. Hence, according to the setting parameters, the proper control strategy is selected.

A list of digital and analogue parameters to set-up the DC-DC converter, and commands to control its behavior are needed. All these directives are given by a higher-level host, i.e. the Central Controller Unit (CCU). The ***MCM Interface Unit*** is responsible for the communication with such device. It receives the setting parameters, interprets them, and transfers the relevant information to each controller unit. After checking the power converter configuration, the module sends the corresponding feedback signals to the MCM. The same applies for ongoing instructions that determine the actions to be taken. The unit also provides information to monitor the converter status, such as bus voltage/current, alarms and error messages.

The ***CLC Interface Unit*** performs a similar task for the communication with another BDC unit. Specifically, in parallel operating mode, it sends an analog signal related to its output current (if master) or receives the corresponding information from the other controller board (if slave). Both the MCM and CLC functional blocks control DAC ICs (AD5541) to transmit analogue response to the external host.

Given that all the logic on FPGA is purely combinational (if not specified otherwise) and all the external signals are asynchronous, by definition the exact time they are asserted and affect the system is unpredictable. In order to ensure a deterministic behavior of the firmware and avoid delay issues, all the elements are developed synchronously with the main clock. The only exception concerns the reset command (active low) to initialize the chip, that is driven by a global asynchronous signal throughout the implemented circuit. After the reset every state machine is in an idle state waiting for an input signal to change. During the initialization sequence

the controller writes appropriate bits to define BDC configuration and select the operating mode, depending on the data received. Then, at the power on, the startup procedure begins and the converters enters the normal operation mode. In this phase, all the routines (sampling, control, actuation) are executed repeatedly until the turn-off command is received, and the system returns into idle state. Program execution suddenly jumps to fault status (disabling all the PWM signals) if a trip condition occurs. In that case, a reset of the system is required.

3.5.2   Main components

PWM Modulator

In the PI-based phase-shift method, the controller dynamically adjust the delay between the voltage waveforms across the series inductor to achieve the desired power flow. This strategy requires a multiphase modulator that generates the gate signals with programmable delays to fire the forced-commutated devices. The Pulse Width Modulation (PWM) technique is employed to create the corresponding digital square waves.
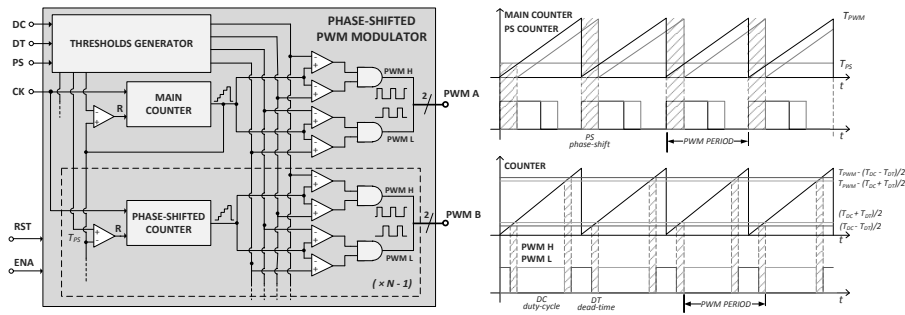
Figure 3.40: PWM generator block and phase-shifted modulation concept. Basically, for a N-legs (half-bridges) power converter, N counters and $2N$ comparators are employed to create the output square waves. Beyond the system signals (main clock, asynchronous reset and enable), the other input variables are the Phase-Shift (PS), the Duty-Cycle (DC) and the Dead-Time (DT) to avoid the short through condition on converter legs.

Fig. 3.40 displays the schematic representation of the module, and illustrates the building principle of the gate-driver signals. The approach is to implement a sawtooth carrier for every half-bridge in the converter. The ramps are shifted in time to correctly space the turn-on of each phases in a single switching period: 180 degrees for the two legs of the same full-bridge, and the input phase-shift for the angle between primary and secondary sides. The sawtooth carrier is generated by incrementing a clock counter, that is periodically reset. The comparison of its value with movable reference signals produce the other discrete ramps. Then, each carrier is compared with proper modulating boundaries to generate the complementary gate pulses for the high-side and low-side power devices. These thresholds values, that determine the rising and falling edges of the PWM signals, depend on the duty-cycle variable and programmable banking time.

The duty-cycle and the phase-shift values can only be varied in discrete steps, as a function of the counter resolution. So, even if the PWM generator does not require a specific input clock, the main clock is employed to achieve the maximum permitted resolution (i.e. 20 ns). Counters define the generated signal frequency. The upper limit is set to 500 cycles, resulting in 10 μs switching period, at 50 MHz clock frequency.

PI controller

The Proportional Integral (PI) regulator is the main element of the feedback control loop. The traditional analog PI equation is given as follows (Eq. 3.5). The adjustable parameters are K_P and K_I, while $u(t)$ is the control output, and $e(t)$ is the error signal between the set-point response level $r(t)$ and the measured quantity $x(t)$.

$$u(t) = K_P \cdot e(t) + K_I \cdot \int_0^t e(t)dt \qquad (3.5)$$

For the purpose of digital implementation, it is convenient to express the transfer function in incremental discrete sampled form. According to the Laplace transform and the Euler discretization method (backward differences), the equivalent expression

is given by:

$$u[k] = \overbrace{K_P \cdot e[k]}^{\text{proportional term, } P[k]} + \overbrace{K_I T_s \cdot e[k] \underbrace{-K_P \cdot e[k-1] + u[k-1]}_{I[k-1]}}^{\text{integral term, } I[k]} \tag{3.6}$$

Fig. 3.41 depicts the architecture of the discrete PI controller derived by Eq. 3.6, for a generic N-bit input. The hardware configuration is designed for integer numbers with parallel structure to get proportional $P[k]$ and integral $I[k]$ error simultaneously. In order to reduce the approximation error, all the calculations are performed using extended registers ($2N/(2N+M)$-bit) and for each algebraic sum, one extension bit is added to take care of possible overflows. The result is truncated only when the routine ends, and the most significant bits of the buffer register are copied into the N-bit output variable. Assuming a 16-bit input, 32-bit registers contain the results of multiplication operations. The integral temporary register includes also M extra guard bit. This allows to execute 2^M (at least) successive sums of the partial products before overhead of the accumulated error occurs and saturation must be applied. Through this strategy no information are lost on the previous integral errors $I[k-1]$ that feeds the final adder.
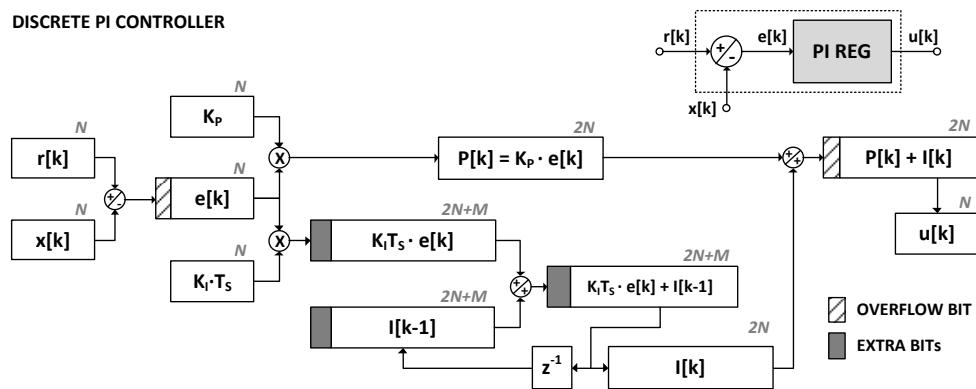
Figure 3.41: Basic scheme of the discrete PI controller.

Analog-to-Digital controller

The LTC1407 is a serial output ADC that contains two separate differential inputs which are sampled simultaneously on the rising edge of the conversion signal (*CONV*). These two sampled inputs are then converted at a rate of 1.5 MS/s per channel with 12-bit resolution (LSB = 610 μV), and the serial interface sends out the results in 32 clocks. The developed VHDL module provides the interface with the digital 3-wire SPI of the integrated circuit, as illustrated in Fig. 3.42.
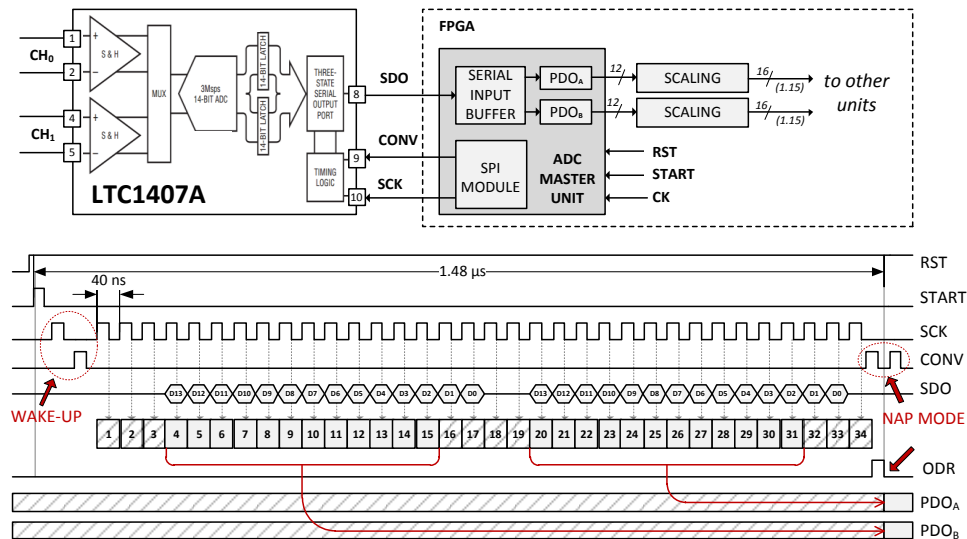
Figure 3.42: The ADC master module: graphical representation and timing diagrams.

The rising edge of serial clock (*SCK*) advances the conversion process and updates each bit in the three-state serial data output (*SDO*) data stream. The transmitted bit are collected in real time by the buffered serial port in the ADC master unit, using the falling edge of the clock to latch the data in a temporary register. When the process ends, output data ready (*ODR*) flag rises and the content of the buffer, that represent the pair of analog input channels in 2's complement format, is moved into the two 12-bit output words ($PDO_{A,B}$). The binary vectors are finally normalized with specific scaling factor and converted into the 16-bit format to be further processed by

the control routines. Two *CONV* pulses with *SCK* at fixed level put the system in nap mode. The *SDO* is automatically reset to the high impedance state and remains in this condition until a new conversion is started, in correspondence with the rising edge of *CONV*.

Digital-to-Analog controller

The AD5541 is a single 16-bit serial input voltage output DAC, that utilizes a versatile 3-wire interface. The DAC master module and the associated timing diagram is shown in Fig. 3.43. The communications require three channels consisting of a clock signal(*SCLK*), a data signal (*DIN*) and a chip select signal (*nCS*). The transmission of the 16-bit input word begins when high-to-low transition on *nCS* occurs. The data are latched on the rising edge of the serial clock. After all the bits have been loaded into the serial input register of the integrated circuit, a low-to-high transition on *nCS* transfers the contents from the buffer register to the DAC output that sets the equivalent analog voltage.
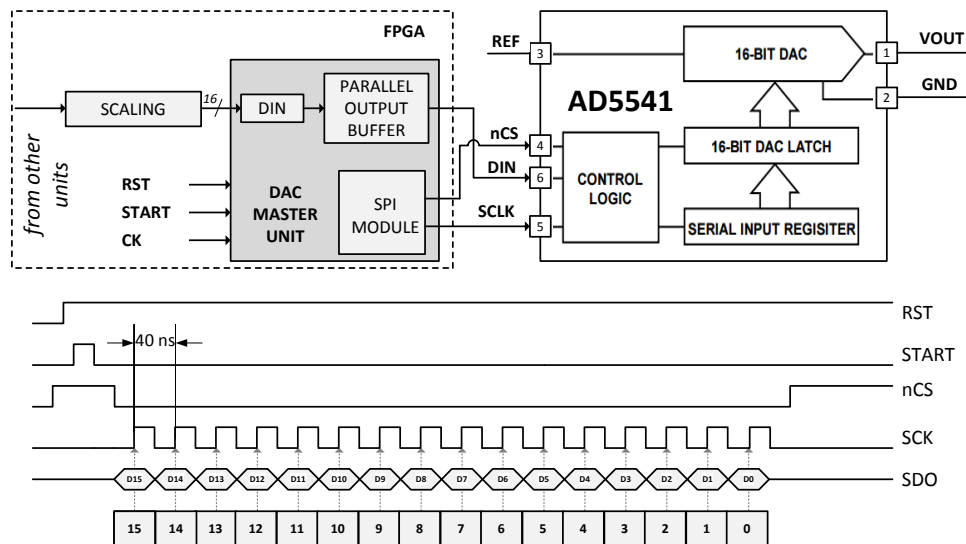
Figure 3.43: The DAC master module: graphical representation and timing diagrams.

Arithmetic operations

Within the firmware design all the numbers are represented using signed fixed-point format. Fixed-point arithmetic is essentially the same as integer arithmetic, so most of the operations follow the same rules and can be executed by means of the algorithms suitable for integer operations. That applies for example to addition, subtraction, and multiplication. Division and square-root are also a necessity for the control purpose (e.g. calculation of the feed-forward term), but the hardware implementation of these operations bring with them some issues because of their complexity. Several studies can be found in literature regarding this task (e.g [49], [50]). The full algorithms used to perform the division and the square-root calculation are illustrated in Fig. 3.44.
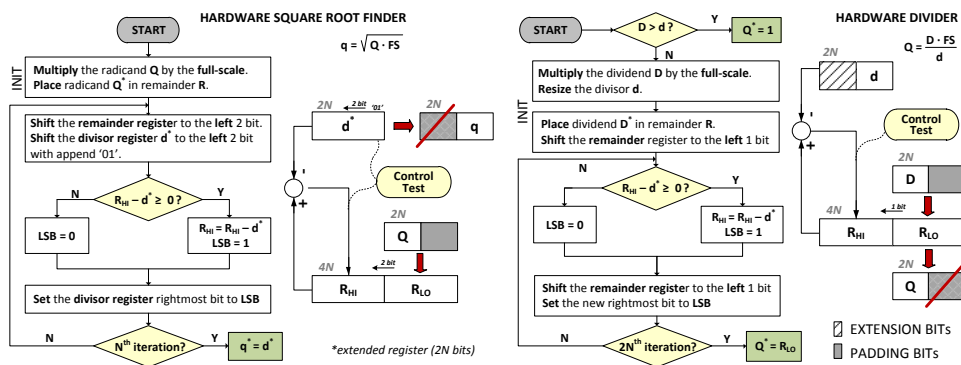
Figure 3.44: Conceptual scheme of the fixed-point square-root and division hardware implementation. Since a fractional interpretation is adopted, the input variables must be properly pre-scaled in order to perform the procedures (developed for integer numbers) without mistakes.

3.6 Thermal management

A significant issue in designing reliable converters is thermal management, with regard to both static and dynamic thermal stress, where static refers to operation at elevated temperatures, and dynamic is associated with heating and cooling cycles. Ex-

tracting heat from a power circuit can be dramatically enhanced by the right choice of materials, structure and layout. In order to assist the design, 3D Finite Element Modeling (FEM) could be an extremely useful tool, especially in complex systems with tight constraints when layout, volume, or weight must be optimized to meet the application requirements and it is difficult to take into consideration these aspects at the same time. Each significant component is modeled employing the simplification procedure described in [51], to reduce the computational complexity and simulate the whole system. Power losses are evaluated by electrical simulations or measurements, and act as heat sources of each element.
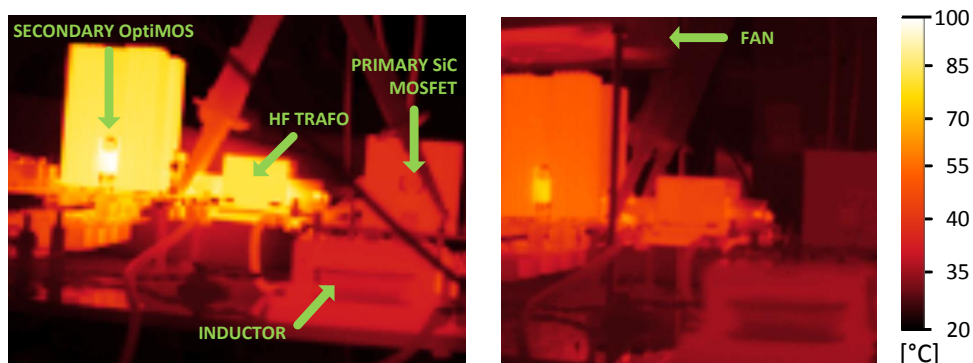
Figure 3.45: IR thermal maps of the converter at steady-state with natural and forced air cooling ($P_o = 600$W, $T_{amb} = 23°$C).

Comprehensive thermal characterization (in terms of infrared measurements) of the converter prototype has been performed throughout the development stages, in natural or forced air-cooling [3] at different power ratings. In particular, the focus was on the key components that contribute to losses: power switches and magnetics elements. Examples of acquired images are given in Fig. 3.45, and transient thermal performance are summarized in Table 3.6. The planar realization of transformer and inductor definitely enables easy and efficient cooling. The most critical components

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[3]From the application specifications, the converter could be fan cooled at the nominal operating conditions but it must be able to operate also in the event of fan failure, with 50% power derating.

are the OptimMOS at the secondary side, while on the primary side results indicate the possibility to significantly reduce the heatsink size. Hence, the target of the simulation study was to improve the heat transfer rate from these devices toward the ambient. Detailed description can be found in [52].

Table 3.6: Dynamic temperature measurements with natural convection (*nat*) or forced air cooling (*fan*), at different power loadings.

t(min)	SiC MOSFET			OptiMOS			Transformer			Inductor			
	T1	T2	T3	T1	T2	T3	T1	T2	T3	T1	T2	T3	
0	22	24	24	22	25	26	22	26	25	22	25	24	°C
5	28	28	33	38	48	87	35	35	41	24	28	33	°C
10	34	29	34	64	56	95	47	44	49	27	30	34	°C
15	39	30	35	79	58	102	60	47	55	31	31	40	°C
20	42	30	35	87	58	103	71	47	55	35	31	40	°C
25	44	30	34	92	58	102	77	48	58	37	31	42	°C
30	46	25	26	95	30	36	81	34	41	40	28	32	°C
40	39	24	24	60	26	25	71	26	25	37	25	25	°C

T1: $P_d = 600W$ (nat), T2: $P_d = 600W$ (fan) , T3:$P_d = 1.2kW$ (fan)

3.6.1   FE thermal model

The first step in this optimization process, was to develop a valid model of the device-heatsink assembly. All the material properties known from literature and components data-sheets were applied. Then, thermal contact resistances and convective heat exchange coefficient (in 20% maximum variation range), were exploited as fitting parameters to tune the FE model to the IR thermal measurements. COMSOL Multi-

physics software was used to set up and run the model. Fig. 3.46 and Fig. 3.47 show the static and dynamic performance of the derived model.
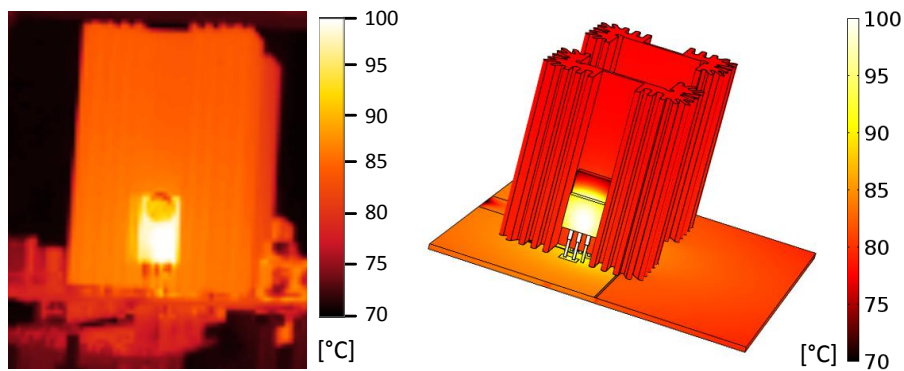
Figure 3.46: Steady-state temperature distribution on on the secondary MOSFETs with natural convection: infrared picture (on the left) and FE simulation (on the right).
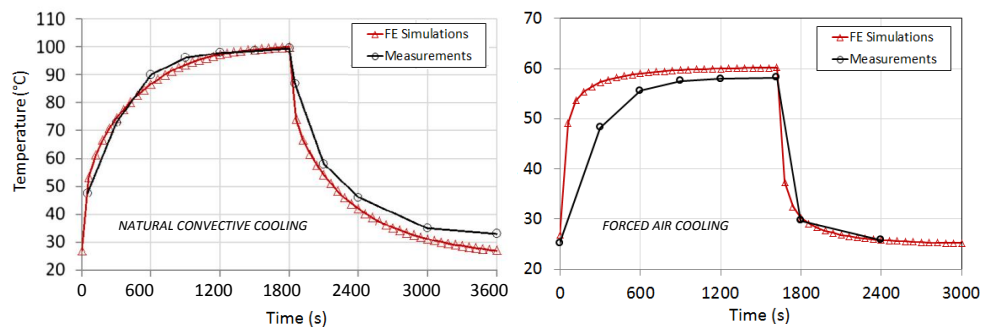
Figure 3.47: IR and simulated thermal transient on the secondary devices. The derived model exhibits a close agreement with the measurements for both natural and forced air cooling.

3.6.2 Heatsink design

Once obtained the model, a comparison study have been carried out. In particular the following possible solutions have been investigated, looking for the best trade-off between thermal resistance and capacitance. One project focuses on the heatsink design and proposes a new geometry which occupies the same volume with a reduced weight and a wider exchange surface. The other design suggests to replace the full plastic package of the device and to exploit the system chassis as heatsink, in order to decrease the thermal resistance to the ambient. This arrangement also implies a greater thermal capacitance that reduces the heating cycles amplitude.

The simulated thermal maps of these instances are depicted in Fig. 3.48. The corresponding thermal transients are reported in Fig. 3.49.
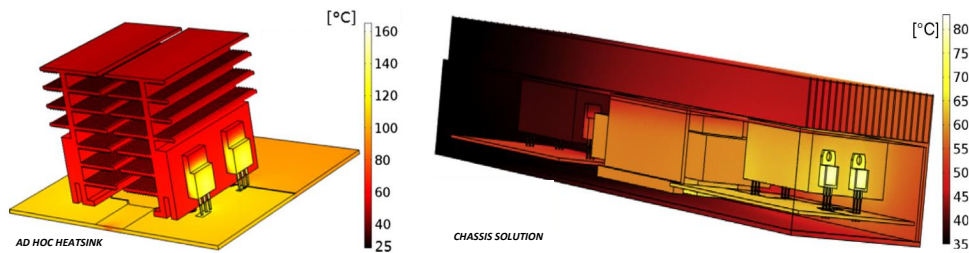
Figure 3.48: FE simulation of proposed solutions. In the full converter geometry all the main heating elements (i.e. primary/secondary power devices, transformer windings and core losses, and inductor losses) are also taken into account.

In the final realization, no separate forced cooling will be made available to the power converter. Therefore, a different layout has been opted for. Shared heatsink of power switches are removed, and a direct (electrical insulated) connection of the key components (SiC MOSFET, OptiMOS and transformer) to the external box is adopted. On the secondary side, two devices are paralleled to enhance the current rate and further improve the thermal handling capability.
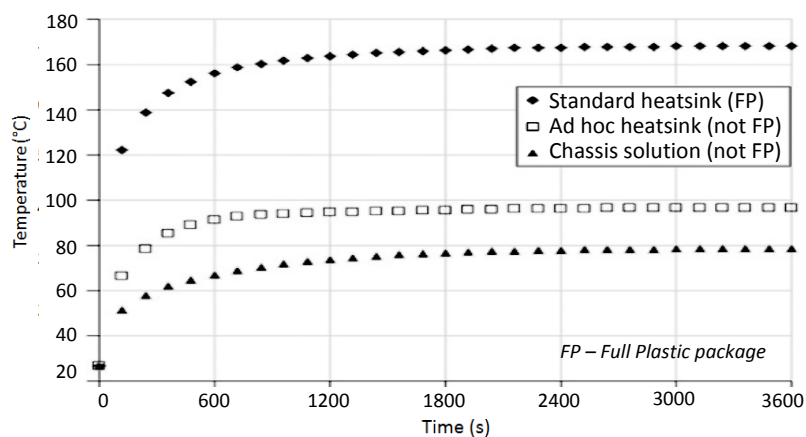
Figure 3.49: Comparison of the case temperature for the different arrangements analyzed (FE simulations).

3.7   Conclusion

The system has been integrated in a specifically designed test rig and subjected to performance and compliance trials, for demonstration purpose.

The selected design approach has proven to be more than adequate for the application. The converter readily achieves it maximum output power and with minor future modifications it will operate at 1.5 kW. It turns on without voltage overshoot or critical inrush current and it can be switched instantaneously from passive load to active regeneration. Feasible parallel connections of two power modules have also been assessed. The FPGA-based governor unit provides an effective digital control of the hardware over all the working conditions.

The prototype still needs some developments to reach the commercial standards for a product which could be installed on an aircraft. However, the BDC unit is already at a TRL6 level and, with further design iterations to improve electronics integration and overall packaging, it could rapidly arrive at a series production level.

Chapter 4

GaN-based DC-DC converter for photovoltaic systems

4.1 Introduction

In the last decades, the interest in renewable sources of energy has grown tremendously. They represent a potential path to mitigate environmental issues and reduce the dependence on traditional sources of energy for electrical generation. Among these, photovoltaics seems to be one of the most practical ways to generate electric power, and PV installations have increased so far in the last years that nowadays solar energy is the most important sustainable sources after hydro and wind power, in terms of globally installed capacity.

The intermittent (and hard to predict) output of a PV field - depending on the time of day, weather, and season - is the main disadvantage of this technology. Es-

pecially for stand-alone systems, where a suitable electric storage device must be provided to ensure the daytime energy requirements. Moreover, when the accumulators are fully charged, no more power can be extracted from the panels. Obviously, a grid-connected system does not suffer from these drawbacks, as the maximum power available from the field can be continuously transferred to/from the grid. For that reason, the majority of the systems is of the grid-connected kind. However, the presence of an intermediate energy storage device may be favorable also for these installations, since it enables self-consumption, that is now both favored and promoted by lawmakers.

In fact, as more solar and wind power comes on line, it becomes increasingly difficult and expensive to ensure stability of the grid. Hence, whereas in the past compensations for feeding-in solar energy were financially rewarding, now the decline in feed-in tariffs for injecting solar current into the grid gives full sense to self-consumption of harvested power. The aim is to satisfy the electricity needs of all electric devices in the household, minimizing the active power exchange between the PV inverter and the electrical grid. A system with energy storage backup is consequently becoming a key issue when discussing the profitability of solar power plants.

The voltage levels and the voltage-current characteristics of energy sources are normally different from those of storage devices and loads. In conventional integration schemes, energy management systems employ separate converters controlled independently to link these elements together. The need of technology for adapting the different voltage levels and carry out an adequate power flow control, has motivated the development of multi-port converters which utilize a single conversion stage for interfacing sources and storage devices. Recently, multi-port converters are gaining popularity because of the potential to reduce the complexity of the system and to achieve flexible, cost-effective, and more efficient integration.

This chapter covers the hardware and control design of a three-port DC-DC converter, as essential part of a novel modular inverter for residential photovoltaic applications. The concept is illustrated in Fig. 4.1 and will be discussed in the next sections.
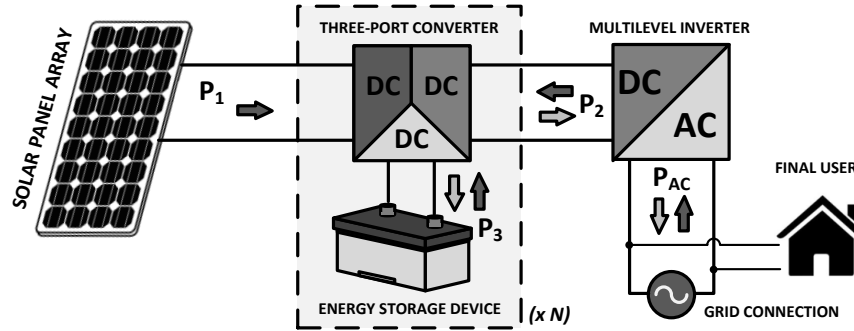
Figure 4.1: Architecture of the proposed modular photovoltaic inverter, for self-consumption use. A battery backup is included to compensate the mismatch between the supply profile and the demand pattern.

4.2 Modular photovoltaic inverter based on low-voltage FETs

The complete converter is a single-phase grid-connected photovoltaic inverter for residential applications, rated at a nominal power of 3 kW. This project idea was firstly presented and investigated in [53]. The power circuit is depicted in Fig. 4.2.
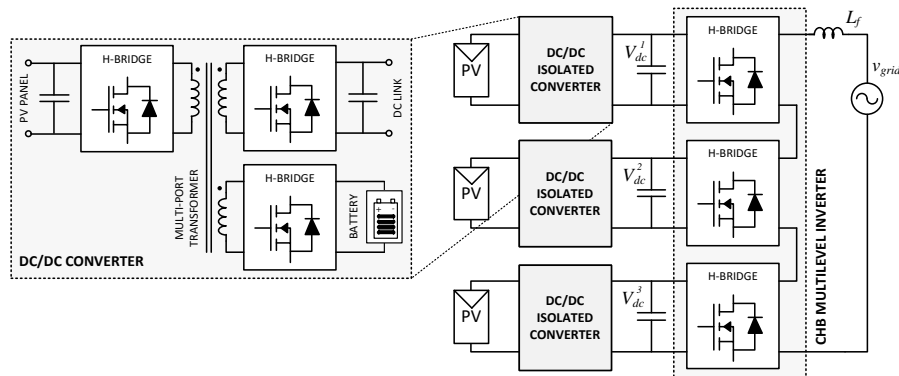
Figure 4.2: Schematic of the modular PV inverter. The storage device embedded in the DC/DC converter acts as an energy filter to smooth the power flow from the primary source (solar panel array) to the multilevel inverter bus.

The architecture is based on a 7-level Cascaded H-Bridge (CHB) inverter, connected to the grid (and to the local load) through an inductor filter, which is used to reduce the switching harmonics. The DC Link voltage is equally divided upon each full-bridge structure, so that devices with lower breakdown voltage requirement can be chosen. As a consequence, the output voltage can assume 7 different intermediate levels (0, $\pm V_{dc}$, $\pm 2V_{dc}$, $\pm 3V_{dc}$) given by the all possible combinations of the series connection and configuration of the full-bridges. Due to its high number of voltage levels, this multilevel topology ensures a better reconstruction of the output waveform (nearly sinusoidal), allows to reduce the size of output filters and increases the converter efficiency. Finally, its high flexibility fosters several control solutions. Here, the Distributed Commutation Modulation (DCM) [54] featuring an additional voltage balance algorithm is adopted.

The CHB inverter needs a separate power supply for each full-bridge section. Three DC/DC converters fed by separate photovoltaic strings are employed for this purpose. In the specific application, the use of Triple-Active-Bridge architecture (see Sec. 2.4) is considered to include an energy storage device into the system. Basically, two ports are utilized to proper interface the PV panels and the inverter DC Link, so that the spare terminals pair can be used to incorporate the battery backup directly into the converter. In this way, the multiple sources can be interconnected without the penalty of extra power processing stages or additional switches. Having two energy inputs available, the instantaneous power can be delivered in the system in a controlled manner, according to the demand of energy and the system operating conditions. When the production of solar panels is not enough, the battery injects the maximum available power and only the still missing energy is consumed from the grid. On the other hand, the PV inverter does not feed the redundant electricity into the utility grid until the battery is fully charged. Beside the capability of providing constant power to the multilevel inverter regardless of the solar irradiance, this solution also enables the implementation of Maximum Power Point Tracking (MPPT) technique for each source individually. This helps to reduce the impacts of power mismatch among the renewable sources and to maximize the output power of the system. Finally, the architecture modularity allows its application for different power

ratings, adapting the number of the conversion strings (PV panel + TAB + H-Bridge).

The use of a triple active bridge converter for the multi-port DC/DC conversion stage is justified by the inherent centralized control of power flow between the three ports, which allows for the implementation of the above mentioned strategy in an effective manner by phase shifting the square wave outputs of the three full-bridges. The TAB topology also shows a number of other attractive features for the application case. These include the ability to connect devices with different operating voltages (by proper winding turns and/or natural buck-boost capability), galvanic isolation, and bidirectional power flow for the all ports.

In order to achieve high efficiency, the choice of switches featuring low on-state resistance and gate charge is a critical design aspect. The EPC's eGaN FETs are a new generation of power switches promising to offer unsurpassed performance over silicon power MOSFETs in switching speed and conduction losses, with superior thermal characteristic. In particular, their switching figure of merit, $R_{ds,on} \times Q_g$, promises to offer a distinct advantage over any similarly voltage-rated silicon device. In addition, the smaller gate charge and device capacitance (hence the faster turn on/off), could allow for higher switching frequency, which results in transformer size reduction. Therefore, the 200V EPC2010C switches from Efficient Power Conversion Corporation (EPC) were selected for the converter prototype. In [55], the same gallium nitride devices have been used for an ultra-high efficient (about 99%) 1.7kW full-bridge isolated converter, to improve the overall efficiency of the power module.

4.2.1 GaN transistors overview

The basic structure of the EPC's enhancement mode gallium nitride power transistors is depicted in Fig. 4.3. The device is grown on silicon substrate with an Aluminum Nitride (AlN) isolation layer. AlGaN is grown on the top of GaN which creates a strain in the lattice that cause electrons density to increase at this interface. A two dimensional high mobility electron gas (2DEG) is formed to provide a channel to direct current from the drain to the source. Depletion area under the gate is added to develop a normally-off transistor, that behaves very similarly to a conventional, enhancement mode silicon power MOSFETs. A positive voltage higher than the threshold between

the gate and the source will turn the device on, and a voltage lower than the threshold will turn it off. Once on, the device can conduct current in either directions from drain to source and vice-versa.
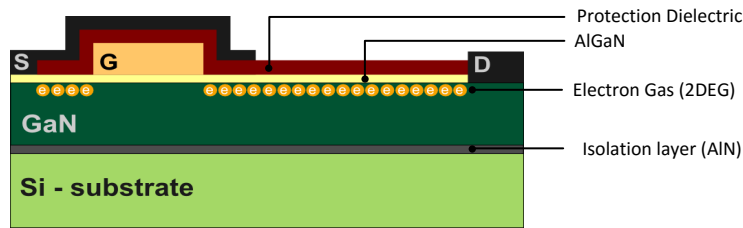
Figure 4.3: eGaN FET structure: when the gate is active.

Since it is a purely lateral device, there is no parasitic bipolar junction common to silicon MOSFETs. Even if the conduction mechanism is different, functionality similar to the body-diode in the reverse direction is still present. When current is forced from source to drain, the drain voltage fails down to a point where it begins to turn the channel on, acting like a diode. As no minority carriers are involved in this conduction process, these devices have no reverse recovery. However, the forward voltage drop is higher than in silicon counterparts and the body-diode conduction time should be minimized to reduce losses and improve overall efficiency.

The maximum gate voltage limits of -5 V to +6 V on the eGaN FET, is lower than silicon MOSFETs limitations. It means lower total gate drive losses, but it poses some restrictions to the gate drive supply range, and requires a more accurate design.

4.2.2   TAB Design

At the beginning of the design, an important parameter to be defined is the switching frequency, f_s. When high power density is required, the general trend is to raise the switching frequency, since the volume decreases increasing f_s. The selected value of 250 kHz, however is rather based on general considerations than on an in-depth system optimization (time for calculations, EMI, layout,...). Once the fixed switching frequency is chosen, the power transfer in the TAB converter is only related to the in-

ductor value and the relative phase-shift angles. Smaller inductance results in higher amount of maximum available power, or in smaller phase angle for the same transferred power. For the same delivered power, current stresses are lower if the converter is designed to operate with small phase-shift angle, improving converter efficiency. On the other hand, to achieve ZVS over a wide operation range, the value of the total inductance should be chosen as high as possible (to store more energy). With this trade-off condition as a background, the transformer was designed to obtain a total leakage inductance, $L_{lk} = 2.2\ \mu H$. The value of the other circuit parameters are listed in Table 4.1.

Table 4.1: Details of the TAB power circuit.

Attribute		Value	
Power rating	P_n	1	*kW*
Switching frequency	f_s	250	*kHz*
DC Link Voltage	V_{dc}	120	*V*
Trafo turns ratio	$N_1 : N_2 : N_3$	1:1:1	
Trafo leakage inductance	L_{lk}	2.2	*μH*
Trafo magnetizing inductance	L_m	0.2	*mH*

The aim of the three-port converter is to automatically and proper combine the contributions of the primary sources (PV panel and battery) in order to provide the required power at the load side (inverter DC Link), while simultaneously maintaining the stability of the entire system. Assuming the situation depicted in Fig. 4.2, port 1 is connected with the PV string, port 2 with the DC Link, and port 3 to the energy storage device. According to the model derived in Sec. 2.4, the active power at the

load side P_2 and at battery side P_3, can be expressed as follows:

$$
\begin{aligned}
P_2 = P_{23} - P_{12} &= \frac{V_2 V_3}{\omega L_{23}} \delta_{23} \left(1 - \frac{|\delta_{23}|}{\pi}\right) - \frac{V_1 V_2}{\omega L_{12}} \delta_{12} \left(1 - \frac{|\delta_{12}|}{\pi}\right) \\
P_3 = P_{31} - P_{23} &= \frac{V_3 V_1}{\omega L_{31}} \delta_{31} \left(1 - \frac{|\delta_{31}|}{\pi}\right) - \frac{V_2 V_3}{\omega L_{23}} \delta_{23} \left(1 - \frac{|\delta_{23}|}{\pi}\right)
\end{aligned}
\tag{4.1}
$$

where $\delta_{23} = -(\delta_{31} + \delta_{12})$ and $L_{31} = L_{23} = L_{12} = L_{lk}/3$ (since the selected turns ratio is $N_1 : N_2 : N_3 = 1 : 1 : 1$). Eq. (4.1) explicits the coupling between the three ports. Any change concerning any phase-shift angle will affect the three power flows and voltages, and depending on the relation between δ_{12} and δ_{31}, each port can be sinking power, sourcing power or remaining at null power.

The dependency of the active power at load side P_2 on the phase-shift angles δ_{12} and δ_{31} with this design is illustrated in Fig. 4.4.
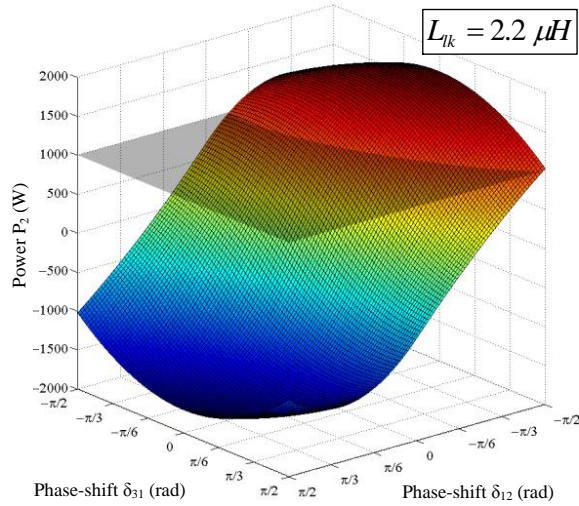
Figure 4.4: Effect of the control variables upon the DC Link power characteristic.

4.3 Control Design

The controller proposed for the TAB converter is still based on the phase-shift modulation. Each power device operates at fixed switching frequency with 50% duty ratio and the phase displacements between the pure square waveforms produced by the active bridges at the transformer terminals manage the power flow among the three ports. In this strategy, only two degree of freedom (i.e. two phase-shift angles) are available as control variables, therefore two port currents of the converter could be the control objectives.

The control algorithm aims to achieve a constant voltage on the DC Link (connected to the output multilevel inverter) and to regulate the power flow from/to the secondary source (the energy storage device) simultaneously. To obtain fast dynamic response, a decoupled power flow management is implemented, as shown in Fig. 4.5.
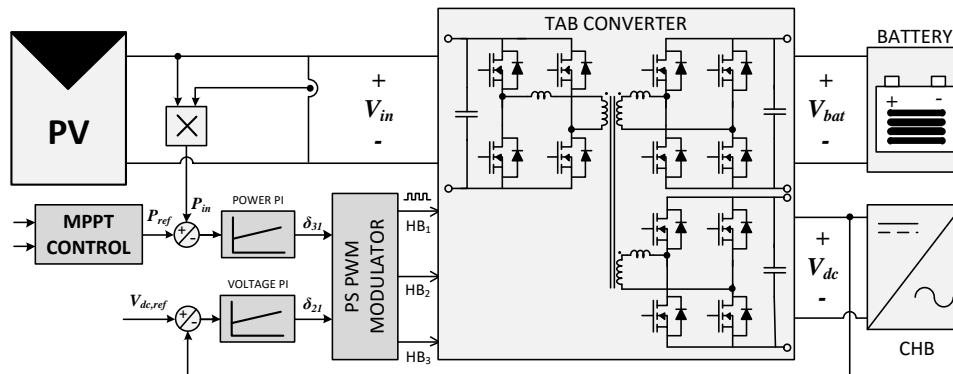
Figure 4.5: Block diagram of the controller for the triple active bridge converter. Two independent feedback loops are employed in order to balance the power consumption and to keep the bus voltage constant.

The power distribution profile is controlled by δ_{31}. Regulation of δ_{21} keeps the bus voltage constant. Since the three-port converter can be viewed as a two-input two-output first-order system, PI regulators would be sufficient to close the feedback loops. To take into account the MPPT technique of every DC/DC module, an ad-

ditional control block is added into the schematic representation, that dynamically changes the operating point.

The voltage and power PI parameters were designed according to Matlab-PLECS simulations in order to achieve an accurate response and keep the whole system (including the plant and the controller) stable. Then, arbitrary power flow profiles have been simulated to study the dynamic behavior of the system and to assess the controller performance. Fig. 4.6 and Fig. 4.7 show simulation results when step changes are applied to the available input power or to the load request, under normal mode operation. In this configuration the main goal of the multi-port converter is to handle the power flows between the three electrical networks in order to balance the total power consumption. The storage element supplies/sinks the energy mismatch between the user and the primary source. At any variation the DC Link voltage experiences a fast transient. However, at the steady-state it remains nearly constant, despite the changes of input and output power.
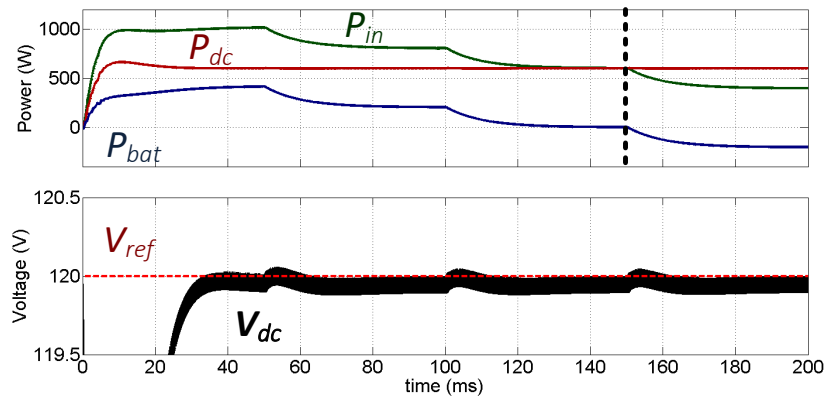
Figure 4.6: Simulation results showing the system response for constant power request ($P_{dc} = 600$ W) under variable available power (P_{in}) from the PV panel.

In order to extend soft-switching operation range in case of wide voltage variations, duty-ratio control can be added (as proposed in [25]). However it is beyond the purpose of this section to discuss further ZVS design methodology.
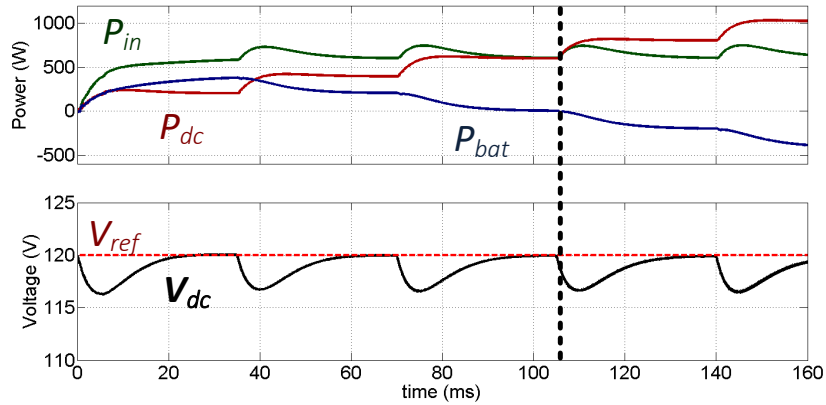
Figure 4.7: Simulation results showing the system response for almost steady input conditions ($P_{in} = 600$ W) and variable power demand (P_{dc}).

4.4   Converter prototype

In order to test the proposed solution a converter was designed. The prototype includes the CPU, that implements the control strategy, the active full-bridges, the high-frequency transformer, the sensors, and the power supply for the logic and analog circuits. Due to the complexity of the design and the number of components involved, a modular approach was preferred to a single circuit board. The basic element of the converter architecture is the H-Bridge circuit. Thus, a stand-alone 1kW 150V full-bridge inverter was chosen as the main building block of the power system.

Overall, three types of PCB were employed in this project: the control board, the interface board, and the power board. In the final realization, three separate power modules will be connected through a multi-winding coupling transformer in order to obtain the TAB converter. The same full-bridge cells could be also arranged to create the CHB inverter.

4.4.1   Power board

The power board includes the full-bridge inverter along with its driving circuits, the DC Link filter capacitors and current/voltage sensors (LA 55-P and LV-25P, respectively), the receivers for optical fiber communications and additional logic elements to generate complementary gate signals (Fig. 4.8). The control board connector provides the main constant voltages (+5 V, ±15 V) needed by the logic circuits, and sends the electrical measurements acquired by the sensors back to the interface card. Individual optical fibers are used to transmit the command pulses to every power switches and an extra input signal is added that activates (or completely disables) the full-bridge. Since the power module must be able to perform well even using only two external commands, a circuit is included to hardware generate the complementary gate driver signals for each converter leg.

The complete schematic and PCB layout are found in Appendix B.
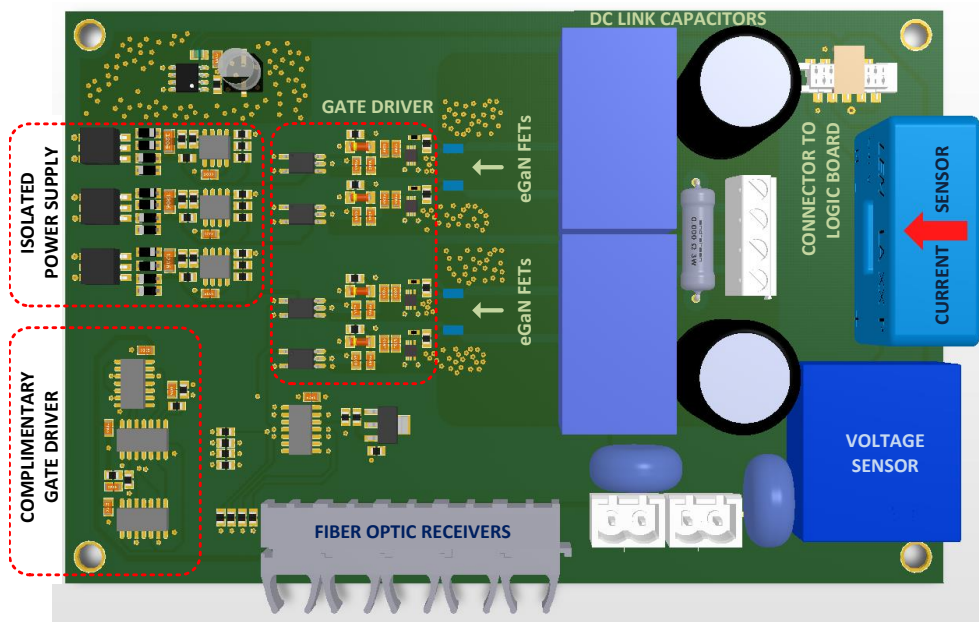
Figure 4.8: 3D PCB layout of the power board (eGaN H-Bridge).

Power section

The power section contains the four active switches and the DC Link capacitors plus the bleeder resistor to discharge them. The eGaN FETs with voltage ratings of 200 V (or less) come in a chipscale Land Grid Array (LGA) package, that reduces board space, stray inductance and parasitic resistance. The impact of the common source inductance should be minimized through careful layout. Given the above consideration, the PCB was designed as close as possible to the manufacturer recommended layouts. As shown in Fig. 4.9, the long sides of the power devices are placed side by side to reduce inter-device inductance, and two ceramic bus decoupling capacitors are located directly beneath the switching pairs of each half bridge to minimize the physical loop size.
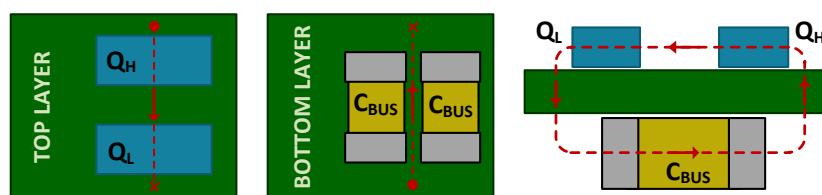
Figure 4.9: The suggested layout places the decoupling capacitors on the bottom side in close proximity to the top power switches.

Gate driver

The gate driver circuit consists of an optocoupler and an insulated power supply for each power device that allow for an independent and flexible control of every switch. The schematic is depicted in Fig. 4.10. The isolated power supplies are generated by the IC MAX256 which drives a 1:2.5 transformer followed by a full-wave rectifier and the LP2954 adjustable voltage regulator. In order to better cope with the gate driver requirements for gallium nitride devices, a single-channel commercial integrated circuit optimized for the selected eGaN FETs has been selected. The UCC27611 by Texas Instruments is a high-speed gate driver that offers asymmetrical rail-to-rail peak current capability with split output configuration that allows for individual turn-on and -off time optimization. The parasitic board inductance in conjunction with the Miller capacitance can cause excessive ringing on the gate drive

waveform, resulting in charging up the decoupling capacitor higher than the 6V max-
imum allowed on the specific GaN transistor. As recommended by the application
notes, a low capacitance Schottky diode is placed in the turn-on current path to pre-
vent this from happening.
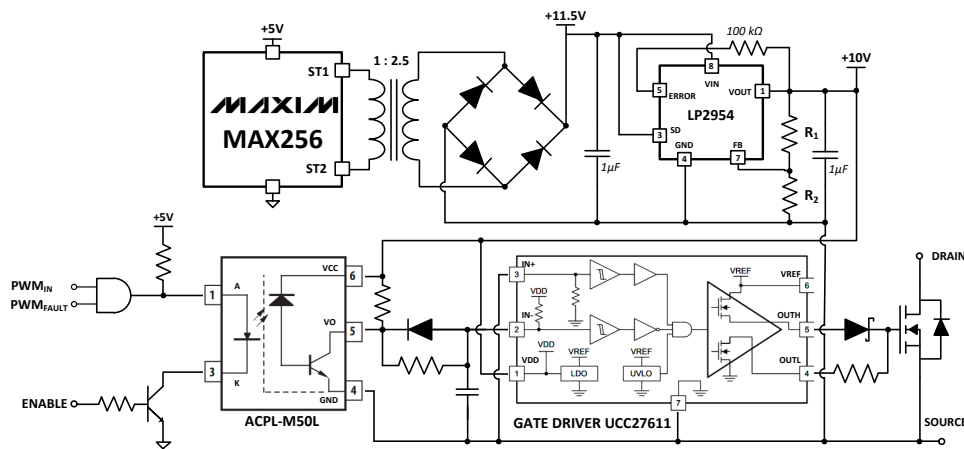
Figure 4.10: Gate driver circuit with insulated power supply.

The PWM signals coming from the DSP are connected to AND gates with the
hardware protection signal generated by the fault detection circuit, that disables all
the logic gates in case of overcurrent event to prevent potential damages. The logic
gates are in open drain configuration, so the current for the photodiodes is given
directly by the 5V power supply. However, if the logic gate is not powered every
photodiode is conducting due to the pull-out resistor. For this reason, every cathode
of the optocouplers is connected to the collector of a BJT driven by the enable signal.
In that way, only if the transistor is polarized it is possible to turn-on the gate drivers.

Logic interface

When only two command inputs are used to control the full-bridge, the comple-
mentary PWM signals (with blanking time) are generated directly on the power board
by the circuit in Fig. 4.11. For each leg of the converter, the PWM input is manipu-
lated by a delay stage and a logic combination circuit to provide the proper control
signals for the upper and lower side devices. In particular, the RC network determines

the dead-time, as shown by the simulation results.
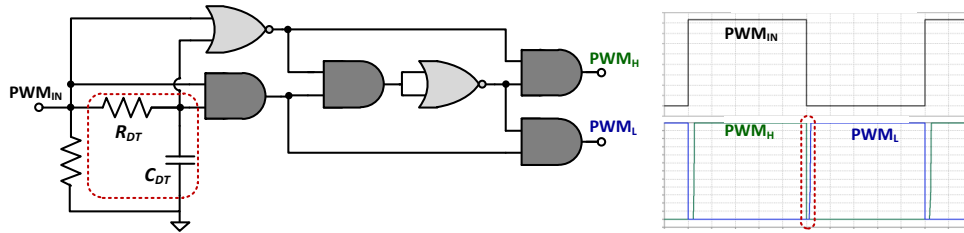
Figure 4.11: Implemented logic circuit that derives the complimentary signals (PWM_H and PWM_L) for each half-bridge, starting from the single command pulse (PWM_{IN}).

4.4.2 Control and interface boards

The control and modulation strategies are implemented on a multipurpose controller platform already developed for other projects in precedent Ph.D. thesis [56], [57]. This circuit board embeds the MPC5643L, a 120 MHz, 32-bit processor by Freescale Semiconductor. Two flex PWM units with four 16-bit channels per module, and sixteen ADC channels make this microntroller particularly appropriate for the proposed converter. Along with the CPU, the control board includes also voltage regulators (3.3 V for the peripheral and 1.5 V for the core), protection circuits for the analog-to-digital converters, and filters for the analog and digital input/output pins.

In order to control the converter prototype with the microcontroller unit at our disposal, a specific interface board was designed and fabricated (Fig. 4.12), that can be easily connected between this controller platform and several H-Bridge cells. The aim is to provide the capability of directly controlling the power modules to the DSP unit. The interface board accepts analog current signals from the field sensors, then it filters, amplifies, converts and scales these measured quantities to analog outputs suitable for the microcontroller data acquisition ports. A main socket conveys these signals to the control board and receives the instructions that operate the converter. The transceivers for data communication over optical fiber cables adapt the PWM

commands to the gate driver requirements. In particular, the board features 12 optic fiber transmitters, 4 flat cable connectors and the conditioning circuits to interface up to four full-bridges.

The complete schematic and PCB layout are found in Appendix C.
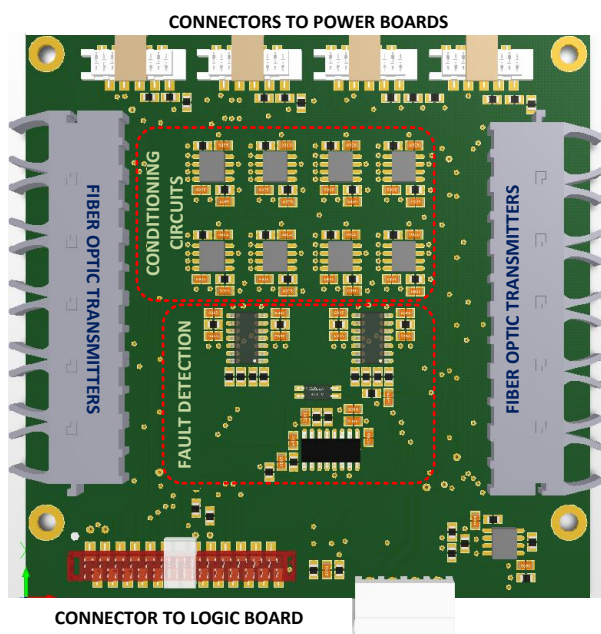
Figure 4.12: 3D PCB layout of the interface board (top view).

The schematic of the signal conditioner circuit is illustrated in Fig. 4.13. The sensor signals are converted by the voltage buffer stage, where the input resistors are selected to adjust the level before further processing can occur (50 Ω and 100 Ω are used for current or voltage measurements, respectively). Then the signals are manipulated by the amplifier stage in such a way that they meet the requirements of the DSP analog-to-digital converter. In this conditioning chain, opto-isolators are not required, since the transducers already provide galvanic isolation between the primary (power) and the secondary (logic) circuits.

The conditioned measurements of the currents are sent also to the fault detection
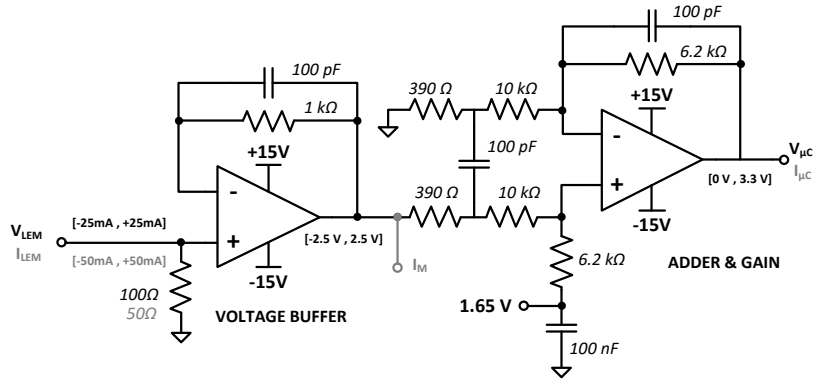
Figure 4.13: Signal conditioning of the measurements coming from the sensors on the power module.

circuits depicted in Fig. 4.14. The overcurrent protection circuit consists of a SR latch driven by the ACPL-217 phototransistor optocoupler, and two dedicated comparators with two voltage dividers for each sensed current (I_M). The resistor networks set the equivalent thresholds for positive and negative power flow. If at least one of the specified limits is exceeded, the output is forced to zero.
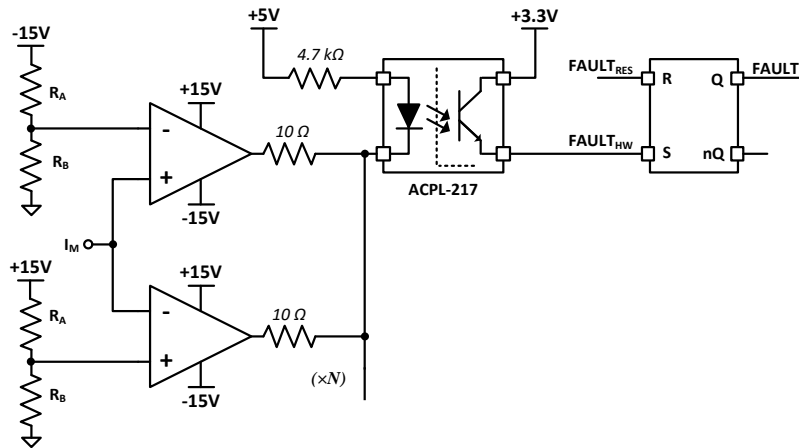
Figure 4.14: Schematic diagram of the fault detection circuit.

Fig. 4.15 presents a picture of the eGaN full-bridge prototype. The interface board was designed to be stacked under beneath the control board. In a similar way, other two H-Bridge modules can be connected to the primary power board through the three-winding high-frequency transformer, for the TAB implementation.
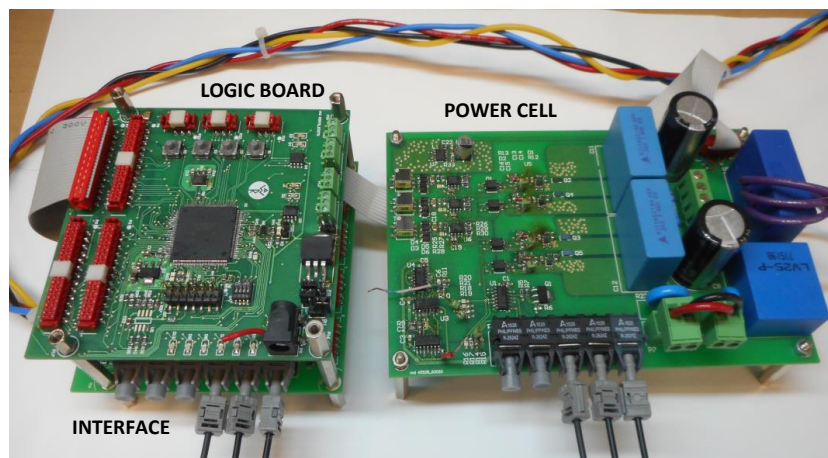
Figure 4.15: GaN-based H-Bridge prototype with control and interface circuitries on separate boards.

4.5   Conclusion

The architecture of a novel solar inverter configured for self-consumption use in residential systems was presented. A three-port bidirectional DC/DC converter links the PV input to the user load and embeds a battery energy storage via a single three-winding isolation transformer.

A dual-PI-loop control based on phase-shift modulation was employed to handle the power flow in order to minimize the energy exchange with the electrical grid, while keeping the voltage on the inverter DC bus constant. For the initial investigations, corresponding circuit simulations under a variety of operating conditions were carried out and they confirmed the theoretical behavior of the energy management system.

Finally, the hardware design of a DSP-controlled 1kW laboratory prototype based on eGaN FETs was described in detail.

In the next steps, after the characterization of the full-bridge module, the TAB prototype will be assembled to verify the functionality and the performance of the proposed concept.

Conclusion

In the presented work, a dual active bridge converter rated at 1.2 kW has been developed for future avionic applications. The use of SiC MOSFETs endows additional benefits in terms of switching losses and high-temperature withstanding. The converter was evaluated in terms of efficiency, dynamic response, either to abrupt load or input voltage variations, and thermal performance. The key characteristics obtained for the realized prototype are summarized in the following list:

- bidirectional power flow capability, with flexible control method;

- average efficiency of 94%;

- soft-switching commutations within almost the entire operating range, realized without auxiliary circuits;

- wide input voltage range (230 V to 300 V), that generates a stable DC output voltage (28 V);

- fully integrated FPGA-based controller;

- safe start-up without any additional pre-charge circuit;

- feasible parallel connection, that can be achieved by choosing between two different approaches.

Simulations and experimental results show that the proposed solution allows to obtain very good performance with respect to the application requirements.

The design of a 1kW GaN-based triple active bridge was also explained herein. According to the theoretical analysis and the simulation results, the converter exhibits the attractive capability of processing the power flow among multiple sources, through a single conversion stage. However, further experimental trials are required to assess the GaN devices performance in this application and to confirm the functionalities of the proposed three-port converter.

Appendix A

Supplement to the small signal model of the DAB

A.1   State space representation

The state-space representation is a mathematical model of a physical system as a set of input, output and state variables related by first-order differential equations. The most general formulation of a linear system is written in the following form:

$$\begin{cases} \dot{x}(t) = Ax(t) + Bu(t) \\ y(t) = Cx(t) + Du(t) \end{cases} \tag{A.1}$$

where $x(t)$, $y(t)$, $u(t)$ are respectively the state, the output, and the control vectors; while A, B, C, D are the state, the input, the output, and the feed-through matrices.

A.1.1   Input Model

The input model of the DAB converter is derived starting from the dynamic phasor equivalent circuit, described by the following equation:

$$\frac{d\langle i \rangle}{dt} = \frac{1}{L} \left[\langle v_1 \rangle - \langle v_2 \rangle - (R + j\omega_s L) \langle i \rangle \right] \tag{A.2}$$

Considering that $\langle x \rangle = x_c + jx_s$ (where x is a generic dynamic phasor), it is possible to split the system into its real and imaginary components, as given by:

$$\begin{cases} \frac{di_c}{dt} = \frac{1}{L} \left(\overbrace{v_{1c} - v_{2c}}^{V_c} - Ri_c + \omega_s Li_s \right) \\[3ex] \frac{di_s}{dt} = \frac{1}{L} \left(\underbrace{v_{1s} - v_{2s}}_{V_s} - Ri_s - \omega_s Li_c \right) \end{cases} \tag{A.3}$$

According to Fourier representation and first harmonic approximation, the two square-wave voltages can be expressed as:

$$v_1(t) = \sum_k \frac{4V_1}{k\pi} sin\left(k\frac{\pi}{2}\right) sin(k\omega_s t) \qquad \xrightarrow[k=1]{FHA} \qquad \frac{4V_1}{\pi} sin(\omega_s t)$$

$$\tag{A.4}$$

$$v_2(t) = \sum_k \frac{4V_2}{k\pi} sin\left(k\frac{\pi}{2}\right) sin(k\omega_s t - \vartheta_d) \qquad \xrightarrow[k=1]{FHA} \qquad \frac{4V_2}{\pi} sin(\omega_s t - \vartheta_d)$$

Remember the general definition of the dynamic phasor for a sinusoidal signal:

$$y(t) = Y cos(\omega_s t + \alpha) \quad \rightarrow \quad \langle Y \rangle = \frac{Y}{\sqrt{2}} e^{j\alpha} = Y_c + jY_s \tag{A.5}$$

the voltage sources in the general averaging model can be written as follows:

$$\langle v_1 \rangle = \frac{4V_1}{\sqrt{2}\pi} \left[cos\left(-\frac{\pi}{2}\right) + jsin\left(-\frac{\pi}{2}\right) \right] \rightarrow \begin{cases} V_{1c} = 0 \\[2ex] V_{1s} = -\underbrace{\frac{2\sqrt{2}}{\pi}}_{A_1} V_1 \end{cases}$$

$$\langle v_2 \rangle = \frac{4V_2}{\sqrt{2}\pi} \left[cos\left(-\frac{\pi}{2} - \vartheta_d\right) + jsin\left(-\frac{\pi}{2} - \vartheta_d\right) \right] \rightarrow \begin{cases} V_{2c} = -\frac{2\sqrt{2}}{\pi} V_2 sin(\vartheta_d) \\[2ex] V_{2s} = -\underbrace{\frac{2\sqrt{2}}{\pi}}_{A_2} V_2 cos(\vartheta_d) \end{cases}$$

$$\tag{A.6}$$

Hence,

$$V_c = v_{1c} - v_{2c} = A_2 sin(\vartheta_d)$$
$$V_s = v_{1s} - v_{2s} = A_2 cos(\vartheta_d) - A_1 \tag{A.7}$$

$$\begin{cases} \frac{di_c}{dt} = \left(\frac{1}{L}A_2 sin(\vartheta_d) - \frac{R}{L}i_c + \omega_s i_s\right) = f_1(i_c, i_s, \vartheta_d) \\ \frac{di_s}{dt} = \left(\frac{1}{L}\left(A_2 cos(\vartheta_d) - A_1\right) - \frac{R}{L}i_s - \omega_s i_c\right) = f_2(i_c, i_s, \vartheta_d) \end{cases} \tag{A.8}$$

Then, the non-linear state space model can be finally linearized around the operating DC point $(I_{c0}, I_{s0}, \vartheta_{d0})$ as follows:

$$\underbrace{\begin{bmatrix} \hat{i}_c \\ \hat{i}_s \end{bmatrix}}_{\dot{x}} = \underbrace{\begin{bmatrix} \frac{\partial f_1}{\partial i_c}|_{I_{c0}} & \frac{\partial f_1}{\partial i_s}|_{I_{s0}} \\ \frac{\partial f_2}{\partial i_c}|_{I_{c0}} & \frac{\partial f_2}{\partial i_s}|_{I_{s0}} \end{bmatrix}}_{A} \cdot \underbrace{\begin{bmatrix} i_c \\ i_s \end{bmatrix}}_{x} + \underbrace{\begin{bmatrix} \frac{\partial f_1}{\partial \vartheta_d}|_{\vartheta_{d0}} \\ \frac{\partial f_2}{\partial \vartheta_d}|_{\vartheta_{d0}} \end{bmatrix}}_{B} \cdot \underbrace{\hat{\vartheta}_d}_{u} \tag{A.9}$$

where the state and control matrix are given by:

$$A = \begin{bmatrix} -\frac{R}{L} & \omega_s \\ -\omega_s & -\frac{R}{L} \end{bmatrix} \quad B = \begin{bmatrix} \frac{2\sqrt{2}}{\pi L}V_2 cos(\vartheta_d 0) \\ -\frac{2\sqrt{2}}{\pi L}V_2 sin(\vartheta_d 0) \end{bmatrix} \tag{A.10}$$

A.1.2 Output Model

The output model equations can be derived starting from the power at the secondary H-bridge.

$$p(t) = v_2(t) \cdot i(t) \quad \rightarrow \quad \langle p \rangle = (v_{2c}i_c + v_{2s}i_s) = -\frac{2\sqrt{2}}{\pi}V_2\left(i_c sin\vartheta_d + i_s cos\vartheta_d\right) \tag{A.11}$$

The resulting function of the state (i_c, i_s) and the input ϑ_d can be linearized as:

$$\hat{p} = \begin{bmatrix} \frac{\partial p}{\partial i_c}|_{I_{c0}, I_{s0}, \vartheta_{d0}} & \frac{\partial p}{\partial i_s}|_{I_{c0}, I_{s0}, \vartheta_{d0}} \end{bmatrix} \begin{bmatrix} \hat{i}_c \\ \hat{i}_s \end{bmatrix} + \frac{\partial p}{\partial \vartheta_d}|_{I_{c0}, I_{s0}, \vartheta_{d0}} \cdot \hat{\vartheta}_d =$$
$$= \frac{2\sqrt{2}}{\pi}V_2 \left[\begin{bmatrix} -sin\vartheta_{d0} & -cos\vartheta_{d0} \end{bmatrix} \begin{bmatrix} \hat{i}_c \\ \hat{i}_s \end{bmatrix} (cos\vartheta_{d0}I_{c0} - sin\vartheta_{d0}I_{s0}) \hat{\vartheta}_d \right] \tag{A.12}$$
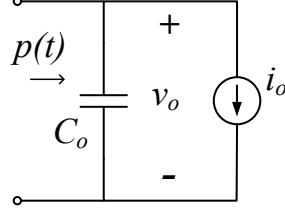
Figure A.1: DAB output stage

In order to have the voltage v_o as an output of the state space representation, the DC load has been modeled as an equivalent current source (Fig. A.1) and the energy balance equation of the output capacitor is exploited.

$$\frac{dW_c}{dt} = \begin{cases} C_o v_o \frac{dv_o(t)}{dt} \\ p(t) - p_o(t) = p(t) - v_o(t)i_o(t) \end{cases} \tag{A.13}$$

$$\frac{dv_o(t)}{dt} = \frac{1}{C_o v_o(t)} \left(p(t) - v_o(t)i_o(t) \right) = f_o(v_o, i_o, p) \tag{A.14}$$

In this way, a model can be derived, where the voltage across the capacitor is the state of the system, while the load current and the power are the input.

$$\dot{v}_o = \frac{\partial f_o}{\partial v_o}|_{v_{o0},p_0,i_{o0}} + \begin{bmatrix} \frac{\partial f_o}{\partial p}|_{v_{o0},p_0,i_{o0}} & \frac{\partial f_o}{\partial i_o}|_{v_{o0},p_0,i_{o0}} \end{bmatrix} \begin{bmatrix} \hat{p} \\ \hat{i}_o \end{bmatrix}$$

$$= -\frac{1}{C_o} \frac{p_o{}^2}{v_o} + \begin{bmatrix} \frac{1}{C_o v_o} & \frac{1}{C_o} \end{bmatrix} \begin{bmatrix} \hat{p} \\ \hat{i}_o \end{bmatrix} \tag{A.15}$$

A.1.3   General Model

The input and output models are not decoupled, in fact $V_2 = V_o/n$. The full model can be built as a merged state space system, by defining $v_o(t)$ as a state.

$$\begin{bmatrix} \hat{i}_c \\ \hat{i}_s \\ \hat{v}_o \end{bmatrix} = \underbrace{\begin{bmatrix} A^{2\times2} & C_1{}^{2\times1} \\ C_2{}^{1\times2} & F_o{}^{1\times1} \end{bmatrix}}_{F} + G^{3\times2} \begin{bmatrix} \hat{\vartheta}_d \\ \hat{i}_o \end{bmatrix} \tag{A.16}$$

where

$$C_1 = \begin{bmatrix} \frac{\partial f_1}{\partial v_o} \\ \frac{\partial f_2}{\partial v_o} \end{bmatrix} = \frac{2\sqrt{2}}{nL\pi} \begin{bmatrix} sin\vartheta_{d0} \\ cos\vartheta_{d0} \end{bmatrix}$$

$$C_2 = \begin{bmatrix} \frac{\partial f_o}{\partial i_c} & \frac{\partial f_o}{\partial i_s} \end{bmatrix} = -\frac{2\sqrt{2}}{nC_o\pi} \begin{bmatrix} sin\vartheta_{d0} & cos\vartheta_{d0} \end{bmatrix}$$

$$G = \begin{bmatrix} \frac{\partial f_1}{\partial \vartheta_d} & \frac{\partial f_1}{\partial i_o} \\ \frac{\partial f_2}{\partial \vartheta_d} & \frac{\partial f_2}{\partial i_o} \\ \frac{\partial f_o}{\partial \vartheta_d} & \frac{\partial f_o}{\partial i_o} \end{bmatrix} = \begin{bmatrix} \frac{2\sqrt{2}}{nL\pi}V_o cos\vartheta_{d0} & 0 \\ -\frac{2\sqrt{2}}{nL\pi}V_o sin\vartheta_{d0} & 0 \\ -\frac{1}{C_o}\frac{2\sqrt{2}}{n\pi}\left(cos\vartheta_{d0}I_{c0} - sin\vartheta_{d0}I_{s0}\right) & \frac{1}{C_o} \end{bmatrix}$$

(A.17)

Thus, the overall model of the DAB converter results:

$$\begin{bmatrix} \hat{i}_c \\ \hat{i}_s \\ \hat{v}_o \end{bmatrix} = \begin{bmatrix} -\frac{R}{L} & \omega_s & \frac{2\sqrt{2}}{nL\pi}sin\vartheta_{d0} \\ -\omega_s & -\frac{R}{L} & \frac{2\sqrt{2}}{nL\pi}cos\vartheta_{d0} \\ -\frac{2\sqrt{2}}{nC_o\pi}sin\vartheta_{d0} & -\frac{2\sqrt{2}}{nC_o\pi}cos\vartheta_{d0} & -\frac{P_o}{C_oV_o^2} \end{bmatrix} \begin{bmatrix} i_c \\ i_s \\ v_o \end{bmatrix} + \begin{bmatrix} \frac{2\sqrt{2}}{nL\pi}V_o cos\vartheta_{d0} & 0 \\ -\frac{2\sqrt{2}}{nL\pi}V_o sin\vartheta_{d0} & 0 \\ -\frac{1}{C_o}\frac{2\sqrt{2}}{n\pi}\left(cos\vartheta_{d0}I_{c0} - sin\vartheta_{d0}I_{s0}\right) & \frac{1}{C_o} \end{bmatrix} \begin{bmatrix} \hat{\vartheta}_d \\ \hat{i}_o \end{bmatrix}$$

(A.18)

The matrix of the transfer functions (with reference to the load current and the controllable phase-shift), can be finally obtained as:

$$M(s) = (sI - F)^{-1} \cdot G = \begin{bmatrix} M_{11} & M_{12} \\ M_{21} & M_{22} \\ M_{31} & M_{32} \end{bmatrix} \begin{bmatrix} \hat{\vartheta}_d \\ \hat{i}_o \end{bmatrix} = \begin{bmatrix} i_c \\ i_s \\ v_o \end{bmatrix}$$

(A.19)

Appendix B

eGaN Full-Bridge: circuit schematic and PCB layout

FULL-BRIDGE

PWR_DC — R37 100k, 3W — PWR_GND

C7 + / C8 + 220uF, 200V — PWR_DC / PWR_GND

C11 / C12 1.5u, 250V — PWR_DC / PWR_GND

C10 / C9 / C27 / C28 2.2uF, 250V — PWR_DC / PWR_GND

PWR_DC

Q3 EPC2010 200V 12A 25mE — GATE H B — SW OUT B

Q5 EPC2010 200V 12A 25mE — GATE L B

Q2 EPC2010 200V 12A 25mE — GATE H A — SW OUT A

Q4 EPC2010 200V 12A 25mE — GATE L A

PWR_GND

COMMAND STAGE

GATE DRIVER

POWER SUPPLY

ISOLATED POWER SUPPLY

INTERFACE

U_OptoIn OptoIn.SchDoc OPTO_IN

U_OptoIn OptoIn.SchDoc OPTO_IN

U_OptoIn OptoIn.SchDoc OPTO_IN

U_OptoIn OptoIn.SchDoc OPTO_IN

U_EnaOptoIn EnaOptoIn.SchDoc ENA_IN — PWM_ENABLE

R14 0R NM — PWM_A_H
R15 0R NM — PWM_A_L
R16 0R NM — PWM_B_H
R17 0R NM — PWM_B_L

U_ComplementaryGate ComplementaryGate.SchDoc
CMD_A
CMD_B
CMD_A_H — R18 0R NM
CMD_A_L — R19 0R NM
CMD_B_H — R20 0R NM
CMD_B_L — R21 0R NM

DGND DGND
PIN_3_NC PIN_2_NC PIN_4_NC +5V
P1
1 2
3 4
5 6
7 8
9 10
Header 2X5
R22 0R NM
LEM_LA +15V −15V LEM_LV

U_Sensors Sensors.SchDoc
HT− — HT−
HT+ — HT+
LEM_LV — LEM_LV
LEM_LA — LEM_LA

P2 earth1 Plug
P3 earth2 Plug
P4 earth3 Plug
P5 earth4 Plug

P6
4
3 PWR_GND
2 SW_OUT_A
1 SW_OUT_B
Header 1x4
PWR_DC

PWR_DC
R23 SIOV-S14Kxxx
P7
2
1
Header 1x2
PWR_GND

HT+
R24 SIOV-S14Kxxx
P8
2
1
Header 1x2
HT−

OPTO IN

+5V
C20 0.1u
HFBR 25XXZ (Rx)
P10
Vcc RL 4
GND NC Vo 1
HFBR_5_NC HFBR_8_NC
DGND
+5V
R38 2.2k — ENA_IN
Q7 MOSFET-N
R39 20k

ENA OPTO IN

+5V
C17 0.1u
AFBR 26XXZ (Rx)
P9
Vcc NC 4
VEE GND Vo 1
GND
AFBR_4_NC
DGND
+5V
R31 2.2k — OPTO_IN
Q6 MOSFET-N
R32 20k

COMPLEMENTARY GATE

Appendix C

Interface board: circuit schematic and PCB layout

COMMAND STAGE

GATE DRIVER
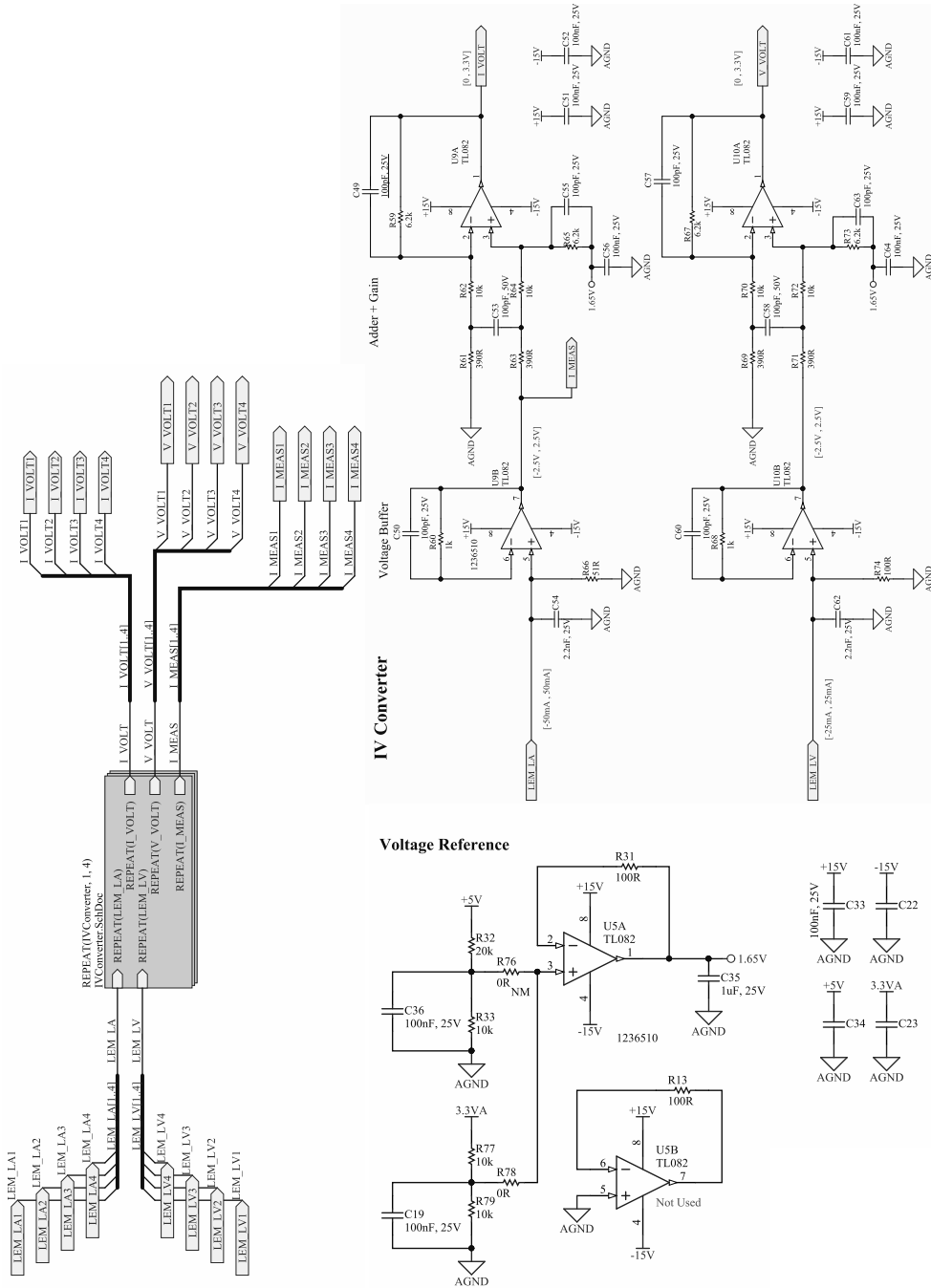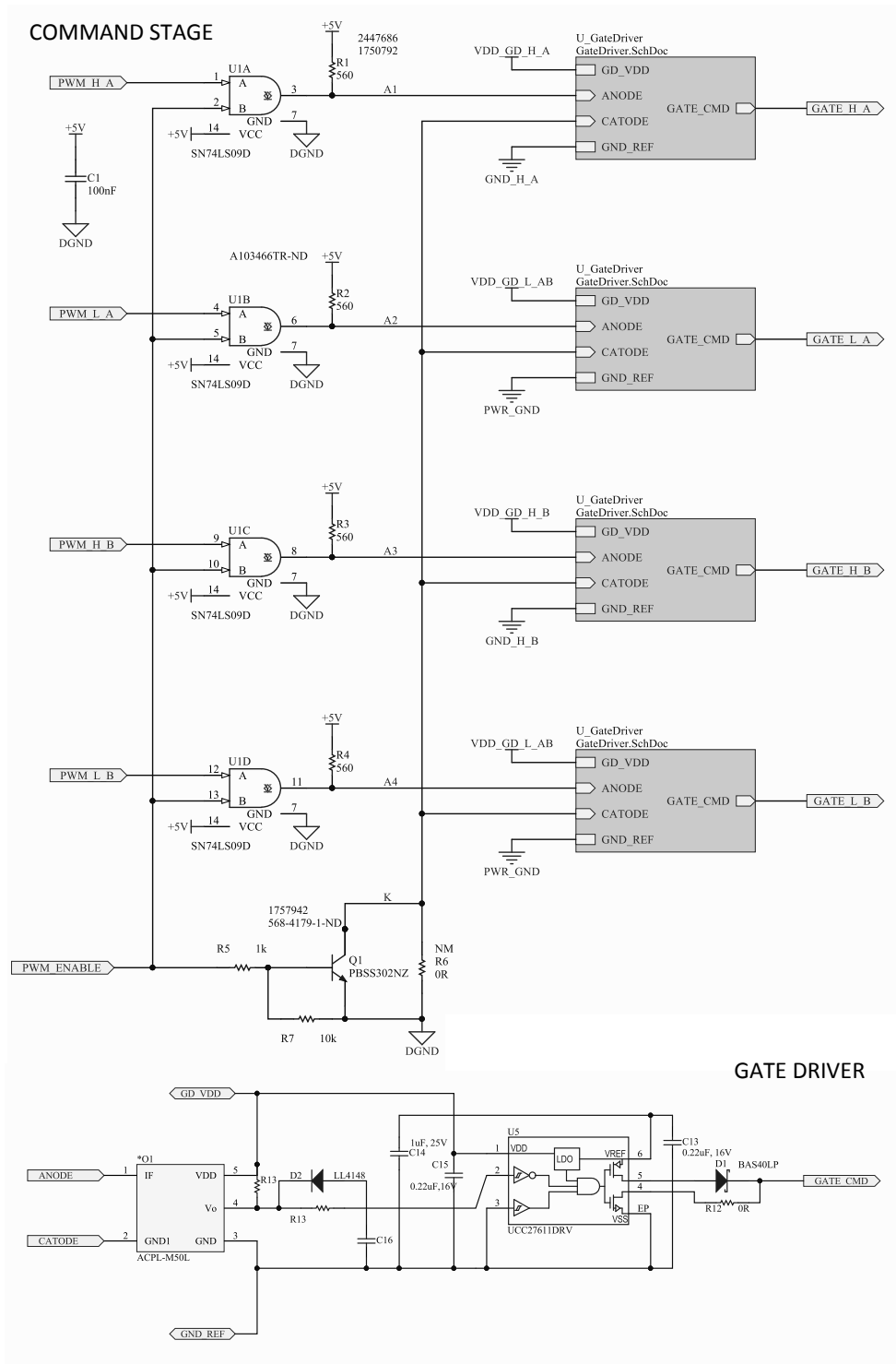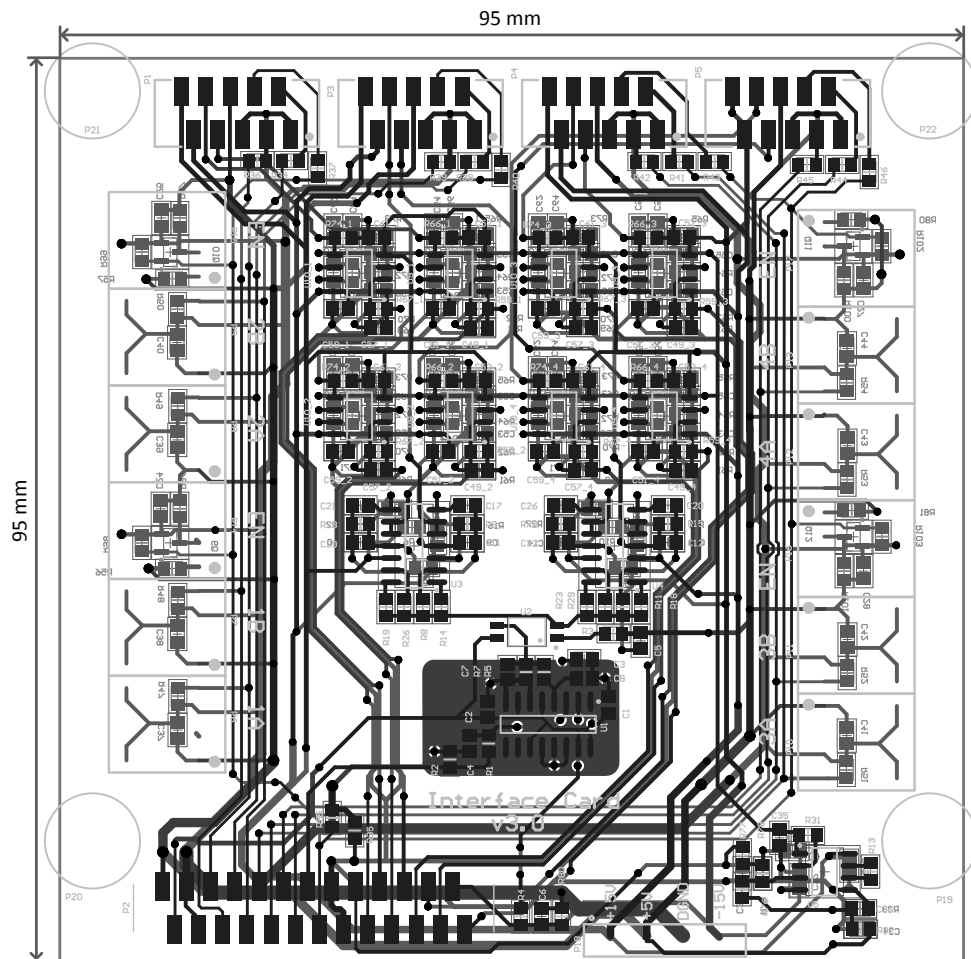
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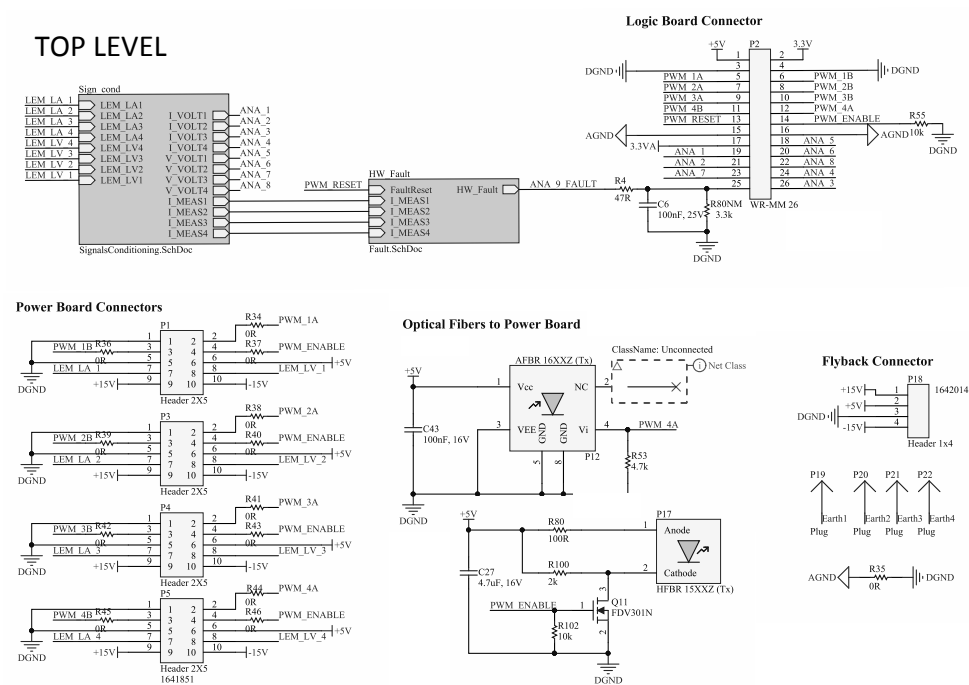[4] J. Biela, M. Schweizer, S. Waffler, and J. W. Kolar. SiC versus Si - Evaluation of potentials for performance improvement of inverter and DC-DC converter systems by SiC power semiconductors. *IEEE Transactions on Industrial Electronics*, 58(7):2872–2882, 2011.

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