



UNIVERSITÀ DEGLI STUDI DI PARMA

Dottorato di ricerca in Scienza e Tecnologia dei Materiali
Innovativi

Ciclo XXVIII (2013-2015)

Tuning the functional properties of Silicon Carbide
Thin Film and Nanowires

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2016

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Most used abbreviations

A.U.	Arbitrary Units
ADF	Annular Dark-Field imaging (TEM imaging technique)
AES	Auger Electron Spectroscopy
AFM	Atomic Force Microscopy
AP	Atmospheric Pressure
APB	Anti-Phase domain Boundary
BE	Backscattered Electron (in scanning electron microscopy)
BL	Buffer Layer
BOE	Buffered Oxide Etch
CL	CathodoLuminescence
CMOS	Complementary Metal–Oxide–Semiconductor
CVD	Chemical Vapour Deposition
DRIE	Deep Reactive Ion Etching
EBID	Electron Beam Induced Deposition
EBL	Electron Beam Lithography
EDX	Energy Dispersive X-Ray Spectrometry
EFTEM	Energy-Filtered Transmission Electron Microscopy
FET	Field Emission Transistor
FFT	Fast Fourier Transform
FIB	Focussed Ion Beam
FIBID	Focussed Ion Beam Induced Deposition
FWHM	Full Width at Half Maximum

HAADF	High-Angle Annular Dark-Field imaging (TEM imaging technique)
HNA	Hydrofluoric acid, Nitric acid and Acetic acid etching solution
HRTEM	High Resolution Transmission Electron Microscopy
IDC	InterDigitated Contacts
LO	Longitudinal Optical
LP	Low Pressure
LTPL	Low Temperature PhotoLuminescence
MEMS	MicroElectroMechanical Systems
MOS	Metal Oxide Semiconductor
MTS	Methyltrichlorosilane (CH ₃ SiCl ₃)
NBE	Near Band Edge
NBOHC	Non-Bridging Oxygen Hole Centre
NW	NanoWire
OAm	Oleylamine
ODC	Oxygen Deficiency Centre
PE	Pass Energy (in the XPS measurement)
PECVD	Plasma Enhanced Chemical Vapour Deposition
RIE	Reactive Ion Etching
RMS	Root Mean Square (square root of the arithmetic mean of the squares of a set of numbers)
RT	Room Temperature
SAED	Selected Area Electron Diffraction
sccm	Standard Cubic Centimetres per Minute
SE	Secondary Electron (in scanning electron microscopy)
SEM	Scanning Electron Microscopy

SF	Stacking Fault
SiCOI	Silicon Carbide on Insulator (layered SiC–insulator–silicon substrate)
SLS	Solid Liquid Solid
SOI	Silicon On Insulator (layered silicon–insulator–silicon substrate)
SSP	Single Source Precursor
STE	Self-Trapped Exciton
STEM	Scanning Transmission Electron Microscopy
TB	Twin Boundary
TEM	Transmission Electron Microscopy
TLM	Transmission Line Measurement
TMA	Trimethylaluminium ($\text{Al}_2(\text{CH}_3)_6$)
TMAH	Tetramethylammonium hydroxide
TO	Transverse Optical
VLS	Vapour Liquid Solid
VPE	Vapour Phase Epitaxy
VS	Vapour Solid
VSS	Vapour Solid Solid
XPS	X-Ray Photoelectron Spectroscopy (also called ESCA)
XRD	X-Ray Diffraction
Y_{SiC}	Young modulus of SiC
β SiC	Cubic Silicon Carbide

Introduction

The reductionist approach is the basis of modern development. It allows any scientist to focus on a single topic and to see outcomes of his discoveries that he wouldn't think of, in disciplines which are poles apart. This fact is evident both for "intensive" research, which looks for fundamental laws, and "extensive" research, whose task is to explain phenomena in terms of fundamental laws. The case of materials science is significant: on the model of stone age, bronze age, iron age... the second part of twentieth century is often called "silicon age", as to say that the discovery of new materials or new applications of a given material mark time of human development. Niels Bohr said: "Prediction is very difficult, especially about the future" so, if we analyse the present times, functional nanomaterials are already a key tool that is driving economic growth. Worldwide inventories are trying to create a "taxonomy" of the phenomenon: European Consumer Organization (EU), Nanotechnology Consumer Product Inventory (US), Nano Products and Technologies (DE), National Institute of Advanced Industrial Science and Technology (JP), The Nanodatabase (DK) are the most recognized examples [1]. Although possible applications include nano-biosensors, drug delivery, nano-robots, nano-scaled electronics, etc. the most diffused functional nanomaterials up to now are nanoparticles mainly used as catalyst and this suggests that the transition from the laboratory bench to commercial marketplace is still on-going. In addition to that, from cosmetics to cars catalytic silencers, the pervasiveness of nanotechnology is still combined with lack of knowledge on its potential effects to the human health and environment.

Silicon carbide represents one candidate to bridge silicon age to nanotechnology age. In fact bulk SiC electronic devices are now widely diffused on the market, while a large family of SiC nanostructures has been intensively investigated. Consequently, SiC due to its well established microelectronics and excellent biocompatibility can open new scenarios in short term development toward nanoelectronics and biomedical applications.

This thesis regards the synthesis and functional properties of both silicon carbide thin film and nanostructures. The crosslink of results about the films and

nanostructures acquired in the framework of this thesis can pave the way to a new generation of devices based on SiC nanostructures.

In **chapter 1** the properties of the material are reviewed, with a specific attention dedicated to the cubic polytype. In particular, the state-of-the-art of electrical contacts on 3C-SiC is presented, together with n and p doping, in view of device development. A brief survey on SiC MEMS processing and fabrication technique is presented being one of the most promising field of application of this material with outstanding mechanical properties. Examples of SiC MEMS devices are then provided in order to show the current technological possibilities. The final section of the chapter is dedicated to SiC nanowires, a particular attention is devoted to the synthesis from gas phase, in order to anticipate the introduction to the final experimental chapter of this thesis. SiC nanowires applications in research and technology are finally showed, as a crosslink with topics outside the mere material science.

In **chapter 2** the developments of SiC heteroepitaxial deposition technique realized during this PhD work are presented. In particular, it is shown how the use of a carbonization layer and the optimization of the buffer layer allowed to increase the crystalline quality of the epitaxial 3C-SiC film on silicon substrates. The introduction of methyltrichlorosilane during the synthesis and its effect on the growth rate and crystalline quality is described and analysed. Nitrogen doping by means of a gaseous line was implemented in the reactor and the characterization of the samples obtained with n-type doping is depicted. In particular, the effect of methyltrichlorosilane on doping level is investigated.

In **chapter 3** the advances in the synthesis of silicon carbide and silicon oxide nanowires are discussed. The substrate preparation proved to be crucial for the morphology and structure of the nanowires synthesized on it. The growth of the core-shell SiC/SiO₂ nanowires is described from the catalyst distribution to the chemical vapour deposition process. Subsequently, the structural and morphological analysis is presented by means of SEM and TEM analysis and a deep investigation of the surface composition is carried out thanks to XPS data. A special section is dedicated to the optical properties of the core-shell nanowires: cathodoluminescence characterization allowed to identify the optical emission centres and the effect of the silicon oxide shell. Carbon doped silicon oxide nanowires were also synthesized and the growth technique is briefly presented. A

deep morphological, structural and compositional analysis was carried out on the nanowires and it is presented by means of SEM, TEM, TEM-EDX and XPS techniques. Finally, studies on the interesting optical properties of these nanowires were carried out using Auger electron spectroscopy (AES) and cathodoluminescence. In the last part of the chapter the processing techniques on core-shell nanowires are presented: after the insulating shell removal by means of chemical etching, electron beam induced deposition was used to contact the nanowires in several zones. Measurements performed to characterize the electrical properties of the single nanowire are then presented.

To understand and finely tailor the structural, electronic and optical properties of silicon carbide and nanowires is of fundamental importance not only for future developments but also for present applications, proven by recent research lines of the group [2]–[4] based on the material presented in this work.

We think that once again material science can be the primary player for technological development, to provide the suitable tools for engineers for the next step in order to deliver effective results in everyday life.

Experimental

The present work was carried out in Imem-CNR Parma (IT) under the supervision of Prof. Giancarlo Salviati and partially at INP-PHELMA Grenoble (FR), under the supervision of Prof. Laurent Montes.

Samples preparation was carried out by the undersigned in collaboration with dr. Matteo Bosi, dr. Giovanni Attolini and dr. Paola Lagonegro. An induction heated vapour phase epitaxy reactor was used to synthesize SiC thin films on silicon substrate. The reactor is composed of a horizontal hot wall graphite chamber and it uses gas phase precursors and hydrogen as carrier gas (more details are provided in chapter 2). Nanowires synthesis was performed in an open-tube CVD reactor on Si substrates with carbon monoxide (CO) as the gaseous precursor and nitrogen as carrier gas.

SEM analysis was carried out by the undersigned in collaboration with dr. Filippo Fabbri using a Field Emission Gun Scanning Electron Microscopy (FEG-SEM) (Jeol – 6400F) and an accelerating voltage of 4 kV.

TEM analysis and images of this work are courtesy of dr. Cesare Frigeri and dr. Francesca Rossi and they were acquired using a Field Emission Gun (FEG) TEM/STEM JEOL 2200FS microscope operated at 200 kV. Images were acquired in the TEM two beam diffraction contrast and high resolution (HR-TEM) modes as well as in the STEM mode with a High Angle Annular Dark Field (HAADF) detector.

Atomic Force Microscopy (AFM) analysis on 3C-SiC films was carried out by dr. Matteo Bosi in contact mode by using a Digital Instruments Nanoscope IIIa.

Cathodoluminescence studies were realized by dr. Filippo Fabbri using a S360 Cambridge scanning electron microscope (SEM) equipped with a MONOCL system (Gatan). Room temperature CL spectra were acquired at an accelerating voltage of 10 kV and a current of 100 nA.

X-ray diffraction was courtesy of dr. Claudio Ferrari, dr. Elisa Buffagni, dr. Elisa Bonnini, dr. Carlo Mora and dr. Francesca Rossi. It was obtained with a custom modified Philips X-Ray diffractometer using Cu K α radiation and a Göbel mirror to investigate the (002) reflection of SiC.

X-ray photoemission spectroscopy (XPS), courtesy of dr. Roberto Verucchi, dr. Lucrezia Aversa and dr. Roberta Tatti, was performed ex-situ in a UHV apparatus for surface electron spectroscopy. The Mg-K α emission at 1253.6 eV was used as X-ray source while the photoelectrons were analysed by a PSP electron energy analyser, leading to a total energy resolution of 0.85 eV. Spectra were performed at low (Pass Energy=50 eV) and high (PE=10 eV) resolution to achieve wide range spectra and the C 1s, Si 2p core levels analysis. Lineshape analysis has been performed by subtracting a Shirley background and then applying Voigt lineshape with Lorentzian to Gaussian ratio of 0.3. X-ray Photoelectron Diffraction (XPD) has been performed at fixed azimuthal angle and variable polar angle on the bulk samples at low resolution (PE=20 eV), to investigate the presence of ordered structure in the films. In order to remove air contaminants, samples were cleaned in an ultrasonic bath of trichloroethylene, acetone and final isopropyl alcohol before the introduction into the analysis chamber, then outgassed in UHV (at 250°C).

Raman spectra are courtesy of dr. Tiziano Rimoldi, dr. Davide Orsi and dr. Luigi Cristofolini. They were collected in backscattering depolarized geometry with a long focal 50x objective, using a JobinYvon T64000 spectrometer in single monochromator mode (employing a 1800 grating/mm grating, with a typical resolution <math><4\text{ cm}^{-1}</math>) and laser at 488 nm with maximum power to the sample <math><1\text{ mW}</math>. Typical integration times ranged from 10 to 60 s.

Metal depositions and photolithographic processes were carried out by dr. Enos Gombia and dr. Marco Calicchio using Microposit positive photoresist S1813, Microposit MF 321 developer and a Karl Suss mask aligner.

Platinum deposition was courtesy of dr. Giacomo Baldi on a Dual beam Zeiss Auriga Compact system equipped with a GEMINI Field-Effect SEM column and a Gallium Focused Ion Beam (FIB) source. Platinum deposition was obtained using focussed ion beam with a beam energy of 30 KV and beam current of 20 pA and electron beam with 30 μm aperture auto mode (auto current).

AFM studies on nanowires were carried out by dr. Ran Tao on a VEECO Dimension 3100 atomic force microscope at room temperature and normal atmosphere pressure in a quasi-dark box by using a high performance controller Digital Instruments.

Electrical measurements on the single wire were obtained by the undersigned using HP 4156 semiconductor parameter analyser.

Chapter 1 - Material properties and applications

Silicon carbide (or carborundum) is the only stable compound merely made of carbon and silicon. It is a wide, indirect, bandgap semiconductor composed of silicon and carbon in equal amounts and its chemical formula is SiC. Silicon carbide is studied for its excellent characteristics as a semiconductor, its interesting mechanical properties, its chemical inertness and its biocompatibility.

Its discovery is frequently credited to the Swedish scientist Jöns Jacob Berzelius [5], one of the founders of modern chemistry, in 1824, while the wide-scale production came after the synthesis by Edward Acheson in 1891. After he found the extreme hardness possessed by the crystal (9,5 points out of 10 on the Mohs scale), comparable to diamond, he realized the potentiality of his discovery and he applied for a patent [6]. The SiC synthesis obtained melting clay (aluminium silicate) and coke (carbon), called Acheson process, was the first industrial method for SiC production. The most used modern production method is basically the same using silica (silicon oxide) and coke (carbon) as precursors. The first applications of SiC were related to its hardness: abrasive or coating for mechanical tools.

In 1907 Henry J Round, an assistant of Guglielmo Marconi, reported a 'bright glow' from diodes made of carborundum produced with the Acheson process, this was the first reported observation of electroluminescence from a semiconductor [7]. Since then, the synthesis of silicon carbide has been gaining increasing attention not only for the mechanical uses, but also for electronic applications.

In the present days, the use of SiC is still widely dominated in volume by the metallurgical, refractory and abrasive use for aerospace, industrial furnaces and wear-resistant mechanical industries among others, but mass-production SiC electronic devices are commercially available. Silicon carbide is one of the few wide bandgap semiconductor which has an extensive commercial distribution. Schottky diodes, FETs and MOSFETs made of SiC are currently widely used for high temperature or high voltage devices, even if defects reduction is still an issue limiting the massive potential properties of this material.

While the drop of the wafers cost allows SiC to attack market areas traditionally reserved to silicon, its particular features such as high temperature stability, thermal conductivity, hardness, chemical stability[8] and its biocompatibility [9]–[11] nowadays foster the use of SiC for recent developed applications like microelectromechanical systems, nanodevices and biocompatible implantable systems.

1.1 General properties of SiC

The high energy of Si-C bond ensures an elevated young modulus (e.g. comparison with silicon $Y_{SiC} = 424 \text{ GPa}$ e $Y_{Si} = 150 \text{ GPa}$) and a Vickers Hardness of $2600 \text{ kg}\cdot\text{mm}^{-2}$. It is chemically resistant to harsh environments and almost inert to all known substances at room temperature. The potentialities of silicon carbide as a material for **high-power**, **high-frequency** and **high-temperature applications** are attested not only by a wide literature, but especially by the diffusion of commercial devices based on this material.

Wide bandgap, along with high breakdown electric field strength, high saturated drift velocity of electrons, and a high thermal conductivity made silicon carbide the optimal candidate for many devices, since the availability of substrates with reasonable price. Silicon carbide **native oxide** (SiO_2) is stable and it has well-known good dielectric properties. It can be used for devices using similar technologies as it is done for silicon MOS structure.

A **wide bandgap** hampers the thermal ionization of electrons from the valence band to the conduction band, allowing therefore to operate devices at higher temperatures. The **high saturated drift velocity** is very important for high frequency devices, in order to obtain high channel currents and high gain as a consequence. The electric field needed for the breakdown of a material is called **breakdown electric field** (E_b) and a higher value of this parameter means being able to manufacture components such as diodes capable to withstand a high potential in inverse polarization. **Thermal conductivity** was included in the table because it is an important parameter for high power device applications. A weak thermal conductivity leads to a temperature increase which is detrimental for semiconductor devices. The

carrier mobility is inversely proportional to the temperature, so keeping a low operational temperature ensures higher performances.

In Table 1.1 a comparison between SiC physical and electronic properties and those of other semiconductors is reported. The SiC wide indirect bandgap depends on the polytype between 2,39 eV for 3C-SiC to 3,26 eV of 4H, to 3,33 eV for 2H-SiC [12].

Table 1.1: Selection of physical and electronic properties of 3 common used SiC polytypes and other semiconductors (From [13])

	Si	GaAs	GaN	Diamond	3C-SiC	4H-SiC	6H-SiC
Specific density [g·cm ⁻³]	2.33	5.32	6.1	3.51	3.21	-	3.21
Lattice parameter [Å]	5.43	5.65	3.19	3.57	4.36	3.07	3.08
Vickers Hardness [kg·mm ⁻²]	1000	600	-	10000	2600	2600	2600
Band gap (E _g) [eV] 300 K	1.12	1.43	3.39	5.45	2.39	3.26	3.02
Saturated drift velocity V _{sat} [10 ⁷ cm·s ⁻¹]	1.0	2.0		2.7.	2.5	2.0	2.0
Melting point (or subl.) [K]	1690	1510	112 3	3820	2700	2700	2700
n mobility [cm ² ·(Vs) ⁻¹]	1400	8500	900	2200	1000	460	600
p mobility [cm ² ·(Vs) ⁻¹]	600	400	150	1600	40	115	50
Breakdown electric field (E _b) [10 ⁶ V·cm ⁻¹]	0.3	0.4	5	10	2.2	4	2.4
Thermal conductivity [W·cm ⁻¹ ·K ⁻¹]	1.45	0.46	1.3	20	4.9	3.7	4.9
Dielectric constant ε	11.8	12.8	9	5.5	9.7	-	9.66

Although some materials listed in this table, like diamond, have better characteristics than SiC, the lack of suitable techniques available to produce high quality single crystal wafers at a reasonable price hampers their diffusion for commercial devices.

Today direct bandgap materials such as GaN are preferred to produce light emitting devices for their higher light intensity, even if SiC itself is still used as substrate for these applications. The most diffused SiC devices to-date are for high power and high frequency electronics.

1.2 SiC polytypism

The SiC crystalline structure is formed by the close-packed stacking of silicon-carbon bilayer [14]. Each atom of one specie is bonded to four atoms of the other specie in a tetrahedral configuration. Three different arrangements of atoms are possible in a single layer, named A, B and C. Each and every allowed stacking sequence of the layers forms a different crystalline structure called “polytype”. All the silicon carbide polytypes have the same chemical formula, the same composition but many different physical properties and a different crystalline structure, in particular each polytype has a unique and peculiar stacking sequence of the layers.

Polytypism is a particular case of polymorphism where the structure is identical in two dimensions and differ only in the third. The two-dimensional crystallographic translations within the layers are essentially preserved.

The stacking sequence of the bilayers causes the presence of non-equivalent hexagonal and cubic lattice sites, as depicted in Figure 1.1.

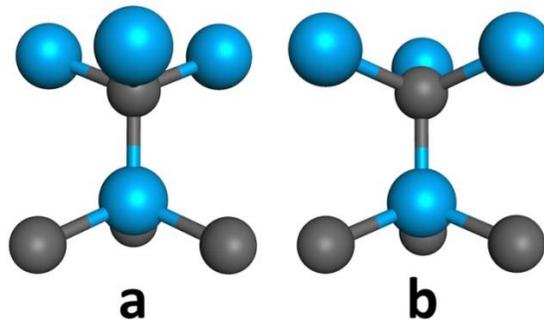


Figure 1.1: Schematic view of the (a) cubic and (b) hexagonal lattice sites. Silicon atoms are depicted as blue spheres and carbon atoms as grey spheres.

In the Ramsdell notation [15], close packed structures are designated by indicating the number of layers in the hexagonal unit cell, followed by the letter **C**, **H** or **R** to indicate cubic, hexagonal or rhombohedral lattice types respectively. Thus the nomenclature $n\mathbf{C}$ represents a structure whose primitive lattice is cubic (**C**) and contains n layers in the primitive hexagonal unit cell. The $[0001]$ axis in the hexagonal structure corresponds to the $[111]$ orientation in the cubic lattice.

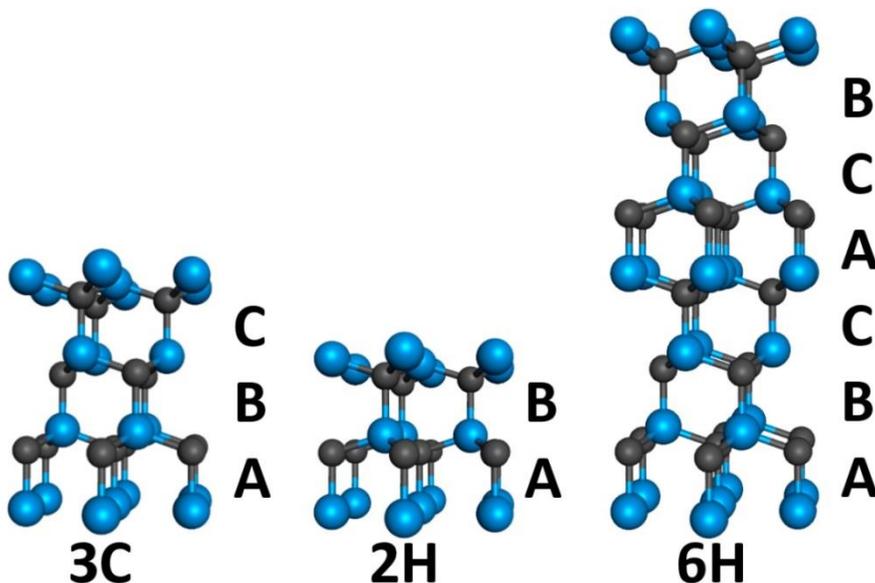


Figure 1.2: Crystal lattices of 3 among the most common silicon carbide polytypes. On the left 3C-SiC, with a stacking sequence of ABC along $[111]$ axis. At the centre 2H-SiC, having AB as stacking sequence. At the right side 6H-SiC, with a ABCACB

stacking sequence. Silicon atoms are depicted as blue spheres and carbon atoms as grey spheres. A single hexagonal unit cell is represented.

3C-SiC and 2H-SiC are antithetic structures: all lattice sites in 3C-SiC are cubic and all lattice sites in 2H-SiC are hexagonal (see Figure 1.2 and Figure 1.1).

6H-SiC was the first polytype available as single crystalline wafer, used to fabricate electronic devices. 4H-SiC is to-date more used for power electronic devices. 3C-SiC is the only silicon carbide cubic polytype and since it is the most similar structure to silicon crystal (cubic lattice), it can be grown on silicon substrates.

This thesis focuses on the cubic SiC polytype, both as thin film and as nanostructure.

Table 1.2: comparison between crystalline properties of the most used SiC polytypes [16]

Ramsdell notation	2H-SiC	4H-SiC	6H-SiC	3C-SiC
Stacking order of reticular planes	AB	ABCB	ABCACB	ABC
Jagodzinski notation	h	hc	hcc	c
Space group	$C_{6v}^4-P6_3mc$	$C_{6v}^4-P6_3mc$	$C_{6v}^4-P6_3mc$	T_d^2-F43m
Percentage of hexagonal lattice sites	100%	50%	33%	0%
Lattice parameter	a = 3.076 c = 5.048	a = 3.073 c = 10.053	a = 3.08 c = 15.117	4.34
Band gap (eV)	3.33	3.26	3.02	2.39
Mobility μ_n (cm ² /v*s)		950	500	1000

1.2.1 Cubic SiC

Cubic silicon carbide (also called 3C or β) shows similar interesting features to the other polytypes, such as wide bandgap (2.39 eV), high breakdown field ($2.2 \cdot 10^6$

V/cm), high thermal stability and conductivity, mechanical strength. In addition to that, 3C-SiC has some peculiar features that fostered the attention of researchers.

Among the three most common polytypes (3C, 6H, 4H), the cubic one has the highest saturated drift velocity ($2.5 \cdot 10^7$ cm/s [17]), which allow to obtain high channel currents in microwave devices[18] and it is helpful for high gain solid state devices.

Owing to the higher symmetry and consequently a reduced phonon scattering, 3C has also the highest electron mobility (≈ 1000 cm²/V·s [17]) (often indicated with μ_n) compared to the other polytypes. The mobility is directly linked to the conductivity of a semiconductor and having a high μ means a higher current ceteris paribus. This will lead to faster capacitance charge. In general, a device built with a material with high mobility has a better high frequency response. Finally, a high maximum current density is fundamental to increase the number of components per integrated circuit chip, towards a large-scale integration.

The thermal conductivity of cubic SiC is significant (3.2 W cm⁻¹ K⁻¹ (poly-3C)) even if compared to those of the most common metals, although slightly lower than other polytypes (3.6 W cm⁻¹ K⁻¹ for 6H-SiC and 3.7 W cm⁻¹ K⁻¹ for 4H-SiC).

Additionally, cubic SiC is more and more used as substrate for the epitaxial deposition of other materials such as gallium nitride [19] or boron nitride [20].

The feature that most of all determined the success of the applied research on cubic SiC over the other polytypes is the possibility of epitaxial growth on silicon, which also has a cubic lattice, but with different constant ($\approx 20\%$ lattice mismatch).

1.3 SiC thin films

Even if SiC has proven to be a strategic material for its mechanical, electrical and chemical properties, and commercial devices are available, there are still many problems to be solved for silicon carbide to pave the way to other applications and to reduce the cost.

Epitaxy (from the Greek *epi* (ἐπί), meaning "above", and *taxis* (τάξις), meaning "ordered") is the deposition of a crystalline layer over a crystalline substrate. When the material of the substrate is different from the one of the layer, the

technique is called heteroepitaxy (in Greek heteros (ἕτερος) means "different" or "other").

Silicon carbide epitaxy is generally performed using vapour phase epitaxy, using gaseous precursors both for silicon and for carbon. Hexagonal SiC polytypes can be homoepitaxially grown on SiC wafers obtained by other techniques in order to achieve a good crystalline quality in the surface layers, while only the cubic polytype can be grown on silicon substrates because of the similar lattice structure.

1.3.1 Advantages of 3C-SiC heteroepitaxy on silicon

Cubic SiC may be heteroepitaxially grown on 6H-SiC [21], on TiC [22], but most notably on a silicon substrate [23] and, since the growth of large 3C-SiC single crystal is still a challenge, heteroepitaxy is the preferred way to obtain state of the art cubic silicon carbide. In addition to that, the bulk SiC available to-date contains screw dislocations that can propagate into the epitaxial layer, as in the case of 4H-SiC [24], while it is possible to find nearly defect-free silicon wafers.

The availability of silicon wafers with diameter up to 17.7 inches compared to the smaller diameters of commercially available SiC, together with the extreme difficulties to obtain single crystal, large area bulk 3C-SiC crystals, pushes the choice for the preferred substrate for 3C-SiC epitaxy towards silicon. Moreover, the lower cost of silicon wafers, even for high quality substrates, may help to bring the benefits of SiC technology to consumer devices.

There are many technological advantages about using SiC on Si, like the easy integration in silicon electronics, which is already extremely developed and almost ubiquitous. Silicon and silicon carbide have also the same native insulating oxide that might be exploited for the processing and fabrication of a Si-SiC based electronic device.

The silicon lattice constant is 5.43 Å [25], while in 3C-SiC it is 4.36 Å [26], this results in a lattice mismatch of approximately 20% that can lead to a highly defective epitaxial film, which can be detrimental for electronic devices.

The substrate thickness is much higher than the epi-layer and this leads the strain to be located almost completely in the deposited layer. The effect is the presence

of shear stresses in crystal planes that may cause defects formation when a critical epilayer thickness is reached.

In addition to that, the different thermal expansion ($\approx 8\%$ difference between Si and SiC) foster the formation of defects during the cooling stage after the growth [16].

A brief review on the defects generated in the SiC layer and strictly correlated to the heteroepitaxy on silicon such as misfit dislocations, twins, stacking faults, antiphase domain boundaries (IDBs) on Si (100) and double positioning boundaries (DPBs) on Si (111) is presented in the next section.

1.3.2 Defects of the epitaxial SiC layer

The difference in lattice parameter between silicon substrate and silicon carbide epilayer causes an “island” growth mode in the very first stages and then may originate many defects in the epitaxial layer.

Misfit dislocations

In the heteroepitaxy of two materials with different lattice parameters a particular type of dislocation called misfit dislocation is generated at the interface of the two crystals, in order to allow the minimization of the bonding strain. The misfit dislocation leaves dangling bonds at the interface and it may propagate as a threading dislocation in the epitaxial layer often causing high leakage currents in a Si/3C-SiC device.

Meaningful TEM images help in understanding the phenomenon (see Figure 1.3): five (111) SiC lattice planes match with four (111) silicon planes, which correspond to a 20% lattice mismatch. The case depicted in Figure 1.3.

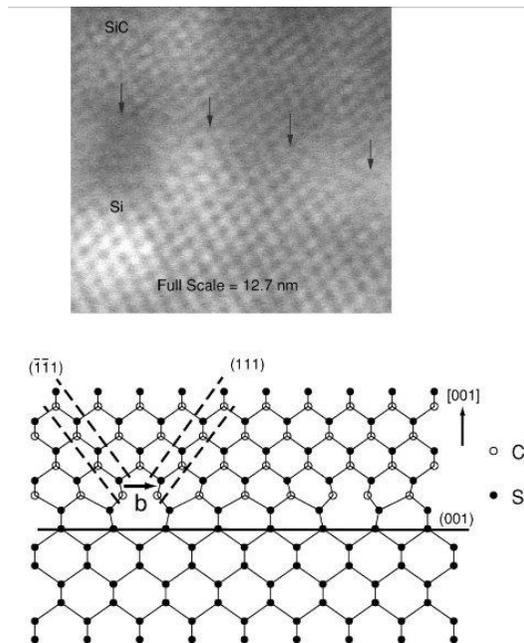


Figure 1.3: Top: high resolution STEM bright field image of the Si(100)/SiC interface. Each arrow corresponds to an edge misfit dislocation. Bottom: scheme of the lattice at the interface projected along [110] axis: Image taken from [27]

In the case of silicon carbide grown over silicon, the difference in the two thermal expansion coefficients contributes to create additional misfit dislocation during the cooling stage after the growth, in order to relieve the stress created at the interface between the two crystals.

Voids

Another typical defect at the SiC/Si interface are voids that are formed due to outdiffusion of Si during the heating process. If the carbonization is not properly optimized and if a continuous, thick SiC layer is not formed after the low temperature carbonization, during the second heating up to the growth temperature Si outdiffusion from the substrate may occur, leaving voids of the dimension of some μm^2 at the interface [28]. These defects may degrade the electrical properties in vertical devices, where current flows in the Si substrate. Also, the presence of voids may disturb the SiC lattice arrangement above them, thus increasing the concentration of extended defects. An example of void at the SiC/Si interface is reported in Figure 1.4.

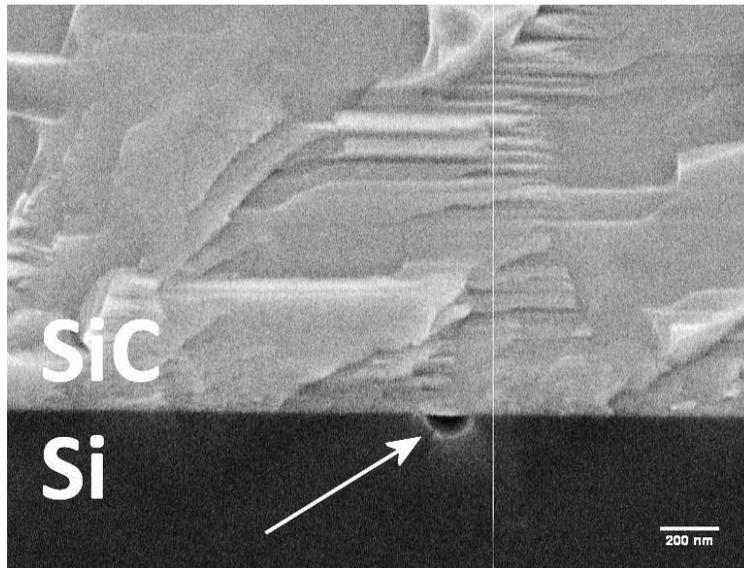


Figure 1.4: SEM cross-section image of the silicon/silicon carbide interface: a small void is created in the silicon layer.

Planar defects

A two dimensional deviation of the position of the atoms from their corresponding lattice site is called generically “planar defect”. The most common types found in heteroepitaxial silicon carbide are stacking faults (SF), twins and antiphase boundaries (APB).

Stacking faults

The difference between the various silicon carbide polytypes is the stacking sequence: each polytype is identified by the sequence of the different layers (ABCABCABC for 3C, ABABAB for 2H, ...). In a perfect crystal the stacking sequence is repeated periodically, while inside a real single crystal, an anomaly in the stacking sequence is called “stacking fault”. This can be also considered as a local occurrence of another polytype.

The energy associated with this kind of defects is very low if compared to other planar defects, because this doesn't affect the near neighbour bonding, therefore, it is very common to observe stacking faults in cubic silicon carbide along the stacking of {111} planes. The (111) face of SiC crystal is the lowest energy surface

and that's the reason for the occurrence of the stacking errors mostly along this plane. This could be an hint to understand why, when the growth orientation is a (111) plane, the formation of stacking faults is increased [27]. It is also appropriate to remember that there is almost the same interface spacings between hexagonal and cubic planes [29].

Twin boundaries

A twin boundary (TB, sometimes called "twin") is a particular defect in the stacking sequence of the planes in which the sequence at the opposite side of the defect plane are mirror images of each other. For example in the cubic polytype, where the stacking sequence is ABCABCABC... a TB may occur like this: ABCABCACBACBA. This correspond to a change in the crystal orientation. TBs tend to propagate along {111} planes.

Antiphase domain boundaries

As said previously, the lattice mismatch between the substrate and the epilayer causes the growth of three dimensional islands in the first stages of the synthesis, a process known as "island growth mode". The genesis of antiphase boundaries (APB) is linked to the non-perfect planarity of the substrate. In addition to the initial roughness of the silicon, that to-date can be significantly reduced, the carbonization process introduce many irregularities. During the island growth mode, islands generated in different sites of the substrate may be at different levels owing to the presence of surface steps on the substrate. During the growth and coalescence of the islands, a Si outer layer of an island may bond with a Si layer of another island, thus forming Si-Si bonds. The same phenomenon may occur with C layers of two different islands generating C-C bonds. These APB bring deep energy levels within the bandgap and behave as strong scattering centres, thus degrading the characteristics of electronic devices [30]. As TB, these boundaries usually propagate along {111} planes, and when two boundaries with opposite orientation combine, they annihilate themselves and the result is the disappearance of the island (and of the APB) (Figure 1.5). For a comprehensive dissertation on APB in 3C-SiC and their annihilation see [30].

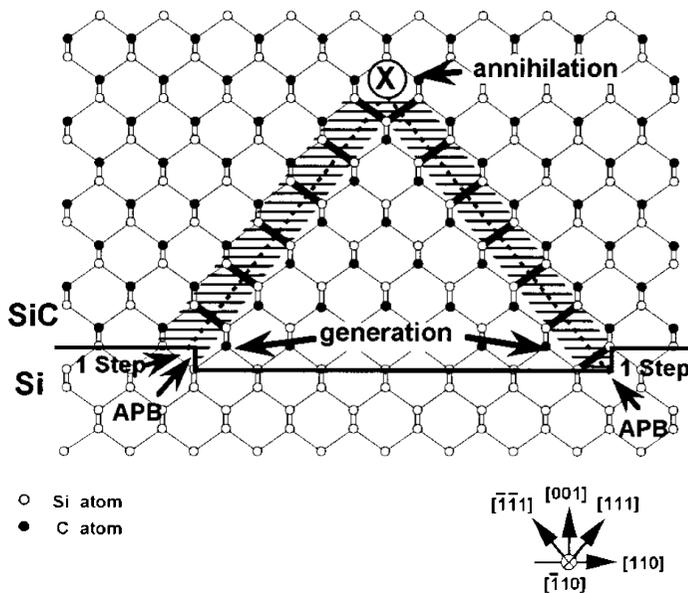


Figure 1.5: schematic structure of two APBs derived from an interface between 3C-SiC film and Si substrate (From [31])

Double positioning boundaries

It is possible to find double positioning boundaries (DPBs) on SiC grown on a (111) surface. A DPB is the result of twins which start from the epilayer-substrate interface. The epilayer may orient with respect to the substrate in two ways that are crystallographically equivalent but are rotated 60° relative to each other. A DPB is formed when two growth nuclei with different orientations coalesce.

1.3.3 Defect reduction

In order to try to reduce the effect of the different lattice parameters between Si and SiC, a carbonization process is often used in the first stages of the epitaxial synthesis. Flowing carbon precursors like propane, methane or ethane at high temperature over the silicon substrate is a well-known technique [23] to create a thin layer of SiC on the surface of the silicon substrate. Since the SiC lattice parameter is lower than the one of Si, in many cases atoms with bigger size like germanium [32] are added during this process.

Frequently the terms “carbonization” and “buffer layer” are mixed up in literature, but in this work we will refer to carbonization as the process performed only with the carbon precursor turning the outer layers of the silicon substrate into silicon carbide. Other precursors may be added, but not the one for silicon, as it happens in the “buffer layer” process, as reported hereafter.

Another technique to ensure the relaxation of elastic energy at the interface between the substrate and the epilayer and to help to stop the propagation of the defects generated at Si-SiC interface is the introduction of a buffer layer prior to the growth. This can be made of silicon and carbon or other materials with less difference in lattice parameters. Typically, the gradual matching between the substrate and final overlayer is ensured via a continuous composition gradient of the buffer layer.

Another common way to reduce the strain is to pattern the silicon substrate in order to grow SiC crystal with a finite size. The first material used and the most common one to manufacture the mask is silicon oxide [33], [34], but other materials like silicon nitride or aluminium nitride also proved to be effective [35].

1.4 Contacts on cubic SiC

The great potential of silicon carbide as a semiconductor hinges upon the control of metal contact properties such as uniformity and thickness of the interfacial region, stability at high temperatures, but, most of all, the **Schottky barrier height** Φ_B , namely the energy barriers for electrons traversing the interface. This value defines the electrical behaviour of a metal contact, determining a ohmic or a Schottky contact.

The characteristics of a good ohmic contact are:

- A linear and symmetric relationship between voltage and current for positive and negative voltages
- Negligible resistance compared with the bulk of the device.

When two materials come in contact, the two Fermi levels must align. In an ideal semiconductor-metal contact, according to the Schottky-Mott relationship [36], for a n-type semiconductor the Schottky barrier height is equal to the difference

between the work function of the metal Φ_M and the electron affinity of the semiconductor χ_S .

$$\Phi_B = \Phi_M - \chi_S \quad 1.1$$

Basing on the above rule one may think it is possible to fabricate good ohmic or rectifying contacts by choosing the metal with the ideal work function. In the real world, however, the Φ_B is weakly dependent on Φ_M , and that is due to surface states. The surface of a crystal is itself an imperfection, thus creating states within the energy gap of the semiconductor. According to Bardeen [37] the density of surface states can be so high to influence Φ_B enough to make it independent of Φ_M . In other words the surface states “pin” the Fermi level, and the control over barrier height is lost. In most of the cases, though, the behaviour is in between the Schottky-Mott and the Bardeen limits.

In addition to that, the interface isn't generally abrupt, because very few interfaces contains material which are inert with respect to each other. Owing to the low diffusion rate of most of the metallic species into silicon carbide and the chemical inertness of the material, the approximation of an abrupt interface can be adopted at ambient temperature. Nevertheless, solid state diffusion, chemical and structural interactions must be taken into account to foresee the behaviour of a metal contact at high temperatures. A rapid review on metal contacts on 3C-SiC shows that one must take into account that a different surface preparation may change completely the results obtained and the behaviour of the contact *ceteris paribus*.

Even if the technology for creating Schottky barriers contacts or ohmic contacts is developed both for hexagonal polytypes and 3C-SiC, this work will focus on the latter because the material synthesised during this PhD was on silicon substrate, therefore, as said before, only cubic polytype.

Generally speaking, an ohmic contact on a semiconductor is more easily fabricated when the semiconductor is highly doped nearby the junction; a high doping narrows the depletion region at the interface and enhances the tunnelling through the barrier thus allowing carriers to flow in both directions easily at any bias.

If the metal contact act as a dopant for the semiconductor, high temperature annealing helps in creating a highly doped region near to the contact that shrinks the energy barrier for the carriers. This works when the initial doping of the semiconductor is of the same type of the doping caused by the metal contact. On the other hand, the fact that the annealing process promotes ohmic contact behaviour limits the temperature range for a metal to be used to obtain a Schottky contact. A high doping in the surface layers can be obtained using other techniques such as high-dose ion implantation [38] with the disadvantage of the easy formation of lattice defects or amorphization. These defects are very stable and high temperature annealing ($\approx 2000\text{K}$) is needed to recover the crystalline order. The quest for straightforward technologies is the reason why the first method (metal contact annealing) is often preferred.

The choice of the metal to use for contacts depositions depends on the doping of the semiconductor. The annealing temperature and time can change the contact behaviour. The typical example for 3C-SiC is nickel: it is possible to obtain a good ohmic contact or a good rectifying contact simply changing the annealing process [39].

A wide range of materials have been examined in a trial-and-error research approach to find the best candidates. Among all materials, metal contacts have been investigated in particular because their fabrication is simple, standard and already well-developed for other semiconductors.

n-type 3C-SiC

Most frequently, the elemental metal layers deposited on n-type 3C-SiC exhibit a Schottky behaviour at room temperature with high barrier height, while the compartment changes after annealing.

As it happens for hexagonal polytypes [40], most of the papers show **Nickel**-based contacts for ohmic purposes on n-type 3C-SiC, owing also to the simple preparation method. Without annealing nickel forms Schottky barrier, while after annealing forms ohmic contacts [39]. Surface defects can break this general rule and allow ohmic contacts even without annealing, in spite of the relatively high Ni work function [41].

As-deposited **Aluminium** is reported to have a ohmic behaviour [42], but annealing results in rectification. This change is attributed to the creation of a p-n junction by diffusion of Al into the SiC, being Al a p-type dopant.

Other metals have been used to fabricate ohmic contacts, in literature it is possible to find many works on **Ti**, but also Cr, Ta, Ag, W, Mo, Au, Re, Pt. For a deeper review see [40].

There are many possibilities to fabricate Schottky contact at room temperature on n-type 3C-SiC, but it is harder to find suitable candidates that preserve the ohmic behaviour at high temperatures. Platinum and copper form good Schottky contacts up to 500°, while Tungsten-based and Molybdenum contacts are suitable for high temperature rectifying contacts [43].

p-type 3C-SiC

The small number of studies on ohmic contacts on p-type testifies not only the relative difficulty in obtaining a good p-type doping in 3C-SiC, but also the limited possibilities for obtaining an ohmic contact.

As mentioned, **Aluminium** is a p-type dopant for SiC and it can be used to obtain high doping concentrations on the SiC surface, thus narrowing the energy barrier for carriers flow. This is the reason behind the choice of this metal in the majority of the studies on contacts fabricated on p-type 3C-SiC [40].

Nickel was also used to deposit contacts on p-type obtaining conflicting results [41], [44]. This may be due to differences in the crystalline quality of 3C-SiC films, but, most of all, differences in the state of the surface prior to metal deposition.

To obtain Schottky contacts on p-type 3C-SiC, tungsten is a promising candidate [43].

1.5 Cubic SiC doping

One of the basic device fabrication processes may become difficult when speaking of silicon carbide. One of the most widespread techniques to obtain semiconductor doping is diffusion but, owing to the strong SiC bonds, the diffusion rate in silicon carbide are very low for all its doping elements. SiC doping

techniques are thus ion implantation, whose treatise is beyond the scope of this work, and in-growth doping.

It is very difficult to achieve a low **unintentional doping** level for 3C-SiC grown on silicon substrates, sometimes 10^{15} cm^{-3} is reported but most frequently 10^{16} or 10^{17} cm^{-3} [45]. Reducing unintentional doping level seems more challenging for 3C than for other polytypes. This can be explained because unintentional doping is usually attributed to nitrogen and nitrogen incorporation is lower at high temperatures owing to enhanced surface desorption effects [45], [46]. Since the substrate is silicon, the maximum synthesis temperature is given by Si melting point (1414°C), lower than those of 4H or 6H SiC synthesis. The only way to reduce unintentional (nitrogen) doping seems to be site-competition epitaxy, as explained below.

n-type doping

Nitrogen doping is a well-established technique to obtain n-type SiC [46], [47], while few studies have been carried out for **phosphor** [48]. N doping level can be controlled varying nitrogen precursor flow (can be N_2 or NH_3 [48]) during growth in CVD process.

Several mechanism have been proposed for nitrogen incorporation in SiC during CVD growth, the two most likely seem to be decomposition of N_2 molecule to monoatomic radicals and then incorporation to SiC surface [49] or nitrogen reaction in the gas phase with SiC precursors to form reactive species [50].

Nitrogen is incorporated in the **carbon atom lattice site** in all SiC polytypes, included 3C. This site-competition principle generates a direct correlation between the **carbon to silicon ratio** ($[\text{C}]/[\text{Si}]$) and the nitrogen doping: by raising the $[\text{C}]/[\text{Si}]$ nitrogen incorporation is hindered and vice-versa [51]. This fact is exploited in order to reduce unintentional doping: raising the carbon to silicon ratio even when not using a nitrogen precursor helps in contrasting unintentional N incorporation. Moreover, it was shown that N incorporation is lower at higher deposition **temperatures** owing to increased surface desorption effects [45], [46]. The correlation between growth rate and N doping varies for the C-face and the Si-face in hexagonal polytypes [47], while, for cubic SiC, nitrogen incorporation at

constant nitrogen flow rate decreases with increasing **growth rate** [46]. An interesting observation for 4H SiC is that nitrogen incorporation during chlorine species-based CVD is not affected by the growth rate [52]. This was never investigated in cubic polytypes to our knowledge.

p-type doping

For p-type doping, **boron** [53] or, most frequently, **aluminium** [54] can be used as acceptors as it is done for hexagonal polytypes. Aluminium incorporation levels can be high ($\approx 10^{20} \text{cm}^{-3}$), but usually only a small portion ($\approx 1\%$) is electrically active due to the deep energy level of this impurity within the bandgap (0,24 eV). Moreover, the usually high unintentional n-type doping of 3C-SiC indicates that p-doped samples are always partially compensated. This fact can be confirmed using low temperature photoluminescence techniques [45], [55].

1.6 SiC MEMS

The recent advances in silicon carbide technology involved also the development of robust material structures, sensors and microelectromechanical sensors (MEMS). Together with the silicon technology achievements, the ability to deposit SiC thin films, to synthesize SiC nanostructures, to fabricate stable contacts and to perform etchings, allowed to obtain SiC based MEMS to be employed for applications where silicon is inappropriate. Silicon devices are limited to temperatures below 200°C owing to thermal carriers generation and junction leakage, while SiC is suitable for high temperature electronic applications [56]. SiC MEMS have a strong resistance to harsh chemical environments [57] or to radiations and the good SiC thermal conductivity is a valid help in dissipating heat from the devices. Furthermore, its excellent mechanical properties make SiC a promising choice as MEMS material for high mechanical stress environments [58]. In addition to that, the biocompatibility of the material is exploited to fabricate bio-oriented devices, included MEMS [59].

Owing to the difficult etching for SiC hexagonal polytypes, the polytype of choice for the realization of MEMS is most frequently 3C, either polycrystalline or heteroepitaxial deposited on Si, SOI, or on a sacrificial layer such as SiO₂ or poly-Si.

Its main limitations of are still due to the low material quality (low crystallinity, high concentration of lattice defects) and the high amount of residual strain due to the heteroepitaxy. However, advances in 3C-SiC epitaxial techniques and the possibility to use well developed silicon wet-etch techniques to realize SiC MEMS provided a convenient way to fabricate even complex devices. Suspended 3C-SiC structures are released by surface machining using both wet and dry etching process.

1.6.1 Processing and fabrication techniques

SiC can be processed with many of the techniques used also for silicon, while, owing to its mechanical hardness and chemical inertness, not all of the silicon etching techniques can be used for silicon carbide.

Oxidation

It is possible to grow a stable thermal oxide layers on all SiC polytypes, as it is commonly done for silicon, but the oxidation rate is much lower. Owing to its chemical stability, SiC is less likely than silicon to dissociate and react with oxygen to form silicon oxide. Furthermore, CO, one of the reaction products, must diffuse out of the oxide layer for the reaction to proceed. Even if the presence of hydrogen or water vapour increases the oxidation rate, frequently, a thick oxide is required for MEMS fabrication; for this reason the deposition of polycrystalline silicon and following oxidation [60] or the direct deposition of silicon oxide is chosen.

Etching

Owing to the excellent SiC chemical properties, the material shows a strong resistance to chemical or physical attacks, nevertheless, several etching techniques have been developed for silicon carbide.

Wet etching proved to be effective but arduous and difficult to perform. Molten salts such as potassium hydroxide are used as anisotropic etch at high temperature ($>460^{\circ}\text{C}$) [61], but etch selectivity and contamination are still issues to solve. Electrochemical or photoelectrochemical etching performed in KOH or

HF can be a choice and doped SiC can act as etch stop. This method has proven to be effective as aid to the wet etching to obtain MEMS devices [62].

Dry etching is the most preferred choice to-date for industrial applications. The most diffused technique is reactive ion etching (RIE) with different chemistries: SF_6/O_2 , SF_6/CHF_3 , CF_4/O_2 , NF_3/O_2 , CHF_3/O_2 , CBrF_3/O_2 , CHF_3/CF_4 , NF_3/CHF_3 , and HBr/Cl_2 silicon oxide, silicon nitride and aluminium nitride are used as etching masks, while metal masks are less used to avoid contaminations [63]. Other dry etching techniques are ion bombardment through ion milling [64] or focused ion beam [65].

SiC-coated MEMS

One can exploit the well-developed state-of-the art of silicon micromachining techniques to obtain devices with complicated design using well-known silicon etchings and covering them with monocrystalline or polycrystalline silicon carbide after the MEMS is released. It has been shown [66] that depositing a thin SiC film over a silicon MEMS improve significantly the wear resistance, decrease the static friction, thus enhancing the device lifetime. The erosion resistance typical of silicon carbide is exploited for SiC-coated MEMS operating in chemically harsh environments [67]. In prospect, the direction of MEMS development will be towards an additional size reduction, for this reason, another feature that is gathering interest is the reduction of adhesion of SiC-coated MEMS [68] thanks to the reduction of surface forces owing probably to topographical surface properties and slower oxidation rates.

SiC on insulator substrates

There is a great interest in obtaining SiC-on-insulator (SiCOI) substrates for micromachining both for obtaining electrical insulation of the SiC layer from substrate and to use oxide as a sacrificial layer or etch stop.

Silicon-on-insulator (SOI) substrates are obtained by ion implantation of O into the subsurface region of Si wafers, or, more frequently, bonding two silicon wafers covered by oxide. The first attempts to achieve a 3C-SiC layer over silicon oxide started from a SOI and performed epitaxial growth over it [69]. This method has some challenges: the buried oxide quality must be high to withstand the elevated

temperatures needed for growing monocrystalline SiC (typically high T, near silicon melting point, 1414 °C, ensures better quality epitaxial SiC, but for MEMS a lower crystalline quality may be acceptable). When silicon oxide reaches high temperatures undergoes glass transitions [70] and start to degrade leaving a holey structure (outdiffusion of oxygen [69]) and worsening the electrical characteristics. Another important challenge is the complete conversion of the silicon overlayer into silicon carbide, if not, an undesirable 3C-SiC-on-Si-on-SiO structure is obtained. The carbonization step, as explained in the epitaxial growth part of this chapter, may help in obtaining that, but the method is limited because the diffusion process can reach a limited thickness (around 200 nm in the Si layer). Finely tuning the growth parameters it was demonstrated the production of SiCOI without significant degradation of the buried layers [71].

The “smart cut” process was already developed for obtaining SOI [72], [73]. The process starts with two oxidized silicon substrates, called handle wafer and the implant wafer. Hydrogen ions are implanted into the implant wafer under the oxide layer and buried in the silicon bulk at a low depth. After the bonding of the two wafers, an annealing is performed and the implanted hydrogen forms a void layer inside the silicon. After that it is possible to break the implant wafer along these voids leaving the thin silicon layer still bonded to the handle wafer. The same process was successfully used using 6H-SiC substrates with 1- μm -thick deposited oxide layer as implant wafer and 6H-SiC, polycrystalline SiC, and Si layers as handle wafer [74] thus obtaining SiCOI.

As for SOI, wafer bonding is also used to obtain SiCOI [75]; in this case the handle wafer is thermally oxidized silicon. A film of cubic silicon carbide is epitaxially grown on a silicon wafer, and silicon oxide is deposited on this SiC layer. The two wafers oxide surfaces are treated and bonded together, then the handle wafer is protected and the silicon is removed from the second wafer generally using wet etching techniques. The result is a 3C-SiC-on-insulator-on-silicon structure. In literature it is possible to find other wafer bonding processes to obtain SiCOI, such the polysilicon-polysilicon bonding technique [76].

1.6.2 Brief overview of SiC MEMS devices

Currently, SiC is the wide bandgap semiconductor material with higher potential for MEMS sensors and actuators to be used in harsh environments and at high temperatures.

The resonators are one of most investigated SiC MEMS. SiC resonant structures can present much higher resonant frequencies compared to the same dimensioned Si or GaAs structures due to its high Young's modulus and the relatively low mass density [77]. SiC MEMS resonators have been fabricated with higher power handling capabilities and operating frequencies, compared to those of similar polysilicon-based resonators. Two types of SiC-based resonators have been reported, which uses a: (i) SiC grown on Si (or SOI) substrates and (ii) homoepitaxial layer grown on single-crystalline 4H- or 6H-SiC substrates [78].

SiC resonators can be easily fabricated on Si substrates using surface micromachining fabrication technology. This fabrication process is attractive because of compatibility of integration with CMOS processes, low-cost film deposition and minimal compromises between the electrical and mechanical performances of the fabricated structures [78]. Wang et al. reported the fabrication of MEMS resonators based on SiC thin film deposited by low temperature PECVD [77]. These resonators were tested and showed a good performance for harsh environments, such as high temperature, erosion and high pressure. The use of mono- and poly-crystalline 3C-SiC grown on Si wafers by CVD in resonators able to work at high frequencies with high quality factors has also been reported in many studies [79].

Regarding the resonant structures made of homoepitaxial layers grown on single-crystalline 4H- or 6H-SiC substrates, their fabrication process is more difficult than that of SiC/Si MEMS. However, high resonant frequency makes 4H-SiC MEMS very attractive for high-sensitivity sensors. Adachi et al. compared the resonance characteristics of 4H-SiC cantilevers on 4H-SiC substrate with the same dimensions 3C-SiC cantilevers fabricated on Si substrate. It was observed that the resonant frequency of the 4H-SiC cantilevers was 10 times that of 3C-SiC cantilevers [80].

Recently, Yang et al. reported high frequency torsional resonators based on a single-crystal 6H-SiC thin layer on top of a SiO₂-on-Si wafer by using a "smart-cut"

process. 6H-SiC smart technology is an alternative process to micromachining of 6H-SiC which not only very time consuming but also require deposited metal masks and still lack precision when thin films and small dimensions are required for devices [81].

Another important type of SiC MEMS is the piezoresistive sensors for harsh environment applications. In the 1990s, the first piezoresistive pressure sensors developed on 6H-SiC substrates were reported for applications up to 500°C [82]. These sensors were batch-microfabricated using a combination of photo and dark etching methods to create the diaphragm. In 2004, Ned et al. reported the fabrication of 6H-SiC pressure sensors, with optimized sensing diaphragms containing “bossed” areas, using a combination of deep reactive ion etching (DRIE) and electrochemical etching [83]. The reports on 4H-SiC pressure sensors are more recent than those of 6H-SiC. In 2011, Akiyama et al. introduced a new approach for fabrication of 4H-SiC bulk sensors using a mechanical milling (drilling) to form the membrane of the sensor. The detailed milling process done by Tecnisco (Japan) was not disclosed [84]. Earlier that year, Okojie et al. investigated 4H-SiC piezoresistive pressure sensors when operated up to 800°C. This is the first experimental work published under piezoresistance vs. temperature for 4H-SiC [85].

On the other hand, the piezoresistive properties of 3C-SiC and a-SiC films and the influence of the temperature on them have been reported by different authors as reviewed in [86]. The first studies were focused on polycrystalline 3C-SiC films. However, recent publications have demonstrated that p-type single crystalline 3C-SiC film is a valuable material for MEMS sensors [87].

1.7 SiC nanowires

3C-SiC nanowires are interesting because of their good physical (mechanical, electrical, thermal) properties. This makes them a promising material for devices operating in harsh environment due to the reason that their elasticity and strength is much greater than the ones of their bulk counterparts, SiC-NWs are also attractive for nanostructured composite materials [88]. Further, functionalized 3C-SiC nanowires have the potential to act as highly sensitive detector elements in bio-chemical field [89].

Being SiC one of the most promising materials for new technologies, the efforts in developing SiC nanostructures is strategic. The increasing number of scientific publications proves that the interest in the topic is rapidly arising among different research groups worldwide.

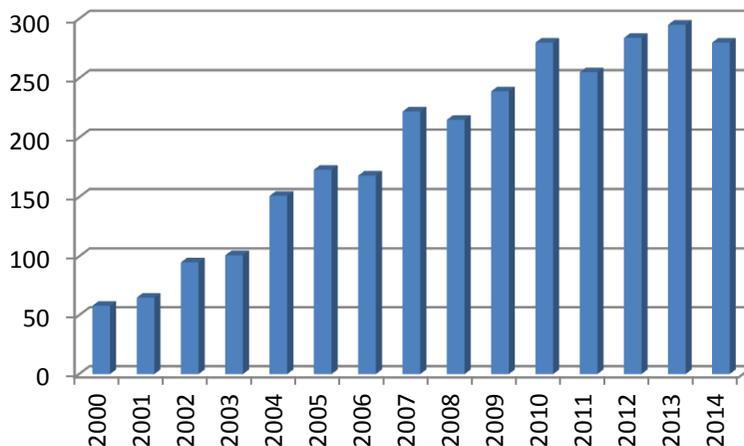


Figure 1.6: Number of publications containing “SiC nano*” in the title. Source: ISI web of Science

Cubic SiC nanowires are obtained by two main methodologies, the bottom-up (B-U), which is the most used, and the top-down (T-D). Many procedures have been used in B-U methodology, one of the most important techniques to fabricate nanowires is chemical vapour deposition (CVD) and this method is used to grow both SiC-SiO₂ core-shell and SiC nanowires.

1.7.1 Synthesis of SiC nanowires

In 1964 R. S. Wagner and W. C. Ellis of Bell telephone laboratories theorized the vapour-liquid-solid (VLS) growth mechanism and they proposed it as an explanation for silicon whiskers growth from gas phase [90]. In the same article they mentioned “crystals of SiC [...] may have grown by the VLS mechanism” as a by-product due to the impurities present in the reactor. Other groups tried to use the same mechanism expressly for silicon carbide and in the following years they reported the synthesis of SiC whiskers [91]. Since then, VLS growth mechanism has been the main route to fabricate SiC microwhiskers. Only in recent years other mechanisms, some of them catalyst free, were reported. Moving to the nanometer scale the term “nanowire” gradually replaces “whiskers” in the literature.

After the work of Iijima [92] focused an unprecedented interest in the carbon nanostructures, the conversion of carbon nanotubes into SiC nanowires was demonstrated [93] through reactions between silicon precursors such as SiO or SiI₂ and carbon nanotubes.

For many decades SiC whiskers or nanowires have been studied for the incorporation in composite materials (metal matrix especially) in order to enhance the strength, toughness and stiffness thanks to their superior mechanical properties [94], [95]. In recent times many other possible applications have been studied and with the miniaturization of electronic devices a brand new field for the nanostructures electronics aroused.

Growth mechanisms of SiC nanowires synthesized from vapour phase

More than 250 polytypes of silicon carbide have been identified [14], [96], but only the cubic (3C or β , stacking sequence ABC) and two hexagonal (4H and 6H, both called α , stacking sequence ABCB and ABCACB respectively) are the most common in literature for nanowires.

The polytype obtained in the final structure of the wires is strictly correlated to the growth parameters, both because the cubic polytype is the most stable at low growth temperature [97] and it is the most energetically favourite for nanowires with larger diameters (approximately more than 20 nm) [98]. That is due to the

lower number of 4H-SiC dangling bonds per surface unit, which makes it the most stable polytype for smaller diameters. For large diameters the bulk energy contribution becomes preponderant and 3C polytype is then the most likely to be found. For these two reasons cubic polytype constitutes the majority of SiC nanowires that is possible to witness in literature.

Epitaxy is a well-established technique used to grow films over a substrate and it is commonly used also for silicon carbide deposition. In order to obtain the growth of a quasi-one-dimensional structure instead of a two-dimensional one, it is necessary to have preferential sites on the substrate surface acting as nucleation points for the vapour deposition.

Some growth mechanisms for the synthesis of silicon carbide need a catalyst in order to occur, like vapour-liquid-solid (VLS), vapour-solid-solid (VSS) and solid-liquid-solid (SLS); all of these are called catalytic growth mechanisms

Frequently a catalytic growth mechanism is spotted by the presence of a catalytic particle either on the tip or at the bottom of the nanowire, but it would not be correct to exclude catalytic growth by the absence of it. It is possible to make a distinction for two catalytic growth processes: float growth and root growth. In the former the particle remains at the top of the nanowire, while in the latter the particle stays at the bottom [99].

Dewetting

The catalyst can be dispersed prior to the growth in the form of nanoparticles but, most frequently, the so-called “dewetting” process is exploited.

A thin film deposited on a solid substrate is frequently a metastable phase and it agglomerates when the temperature is raised to the melting point of the metal or of the alloy formed by the metal and the substrate. The result is the formation of an array of nanoscaled islands whose size can be controlled by varying the procedure parameters such as temperature and dewetting time or by starting from a different film thickness.

Surface energy minimization is the driving force of this process, since the surface to volume ratio of a nanoparticles array is smaller than that of a thin film [100].

As said before, the size of the islands demonstrated to be determinant for the final diameter of the wires [101] and it is strictly correlated to the metal layer thickness [102] so, by varying this in the deposition stage, it is possible to obtain a certain control over the size of the islands and, consequently, over wires diameter.

According to equilibrium thermodynamics it is possible to calculate the minimum radius (r_{min}) of a liquid metal cluster as

$$r_{min} = \frac{2\gamma_{LV}V_L}{RT \ln \sigma} \quad 1.2$$

where γ_{LV} is the liquid vapour surface free energy, V_L is the molar volume, R is the ideal gas constant, T is temperature and σ is the vapour phase supersaturation [103]. Nevertheless droplets diameters smaller than those predicted by this formula have been frequently experimentally found [102] suggesting that this constraint from thermodynamics can be overcome out of equilibrium. This can still be used as a general rule of thumb to know the dependence of droplets size from the thermodynamic conditions.

A scheme of a VLS growth mechanism with the dewetting of a solid-state film is represented in Figure 1.7.

Vapour-liquid-solid growth mechanism

The vapour-liquid-solid mechanism, described by Wagner and Ellis in 1964 [104], is the most exploited process for the synthesis of semiconductor nanowires and this is true in particular for silicon carbide synthesis, given that this method was also used to produce microstructures and bulk crystals [105], [106]. The process is used to synthesize many other materials and it was found also occurring in nature, even some minerals found on the moon were probably grown by a VLS mechanism [107].

The process takes advantage of metal nanoclusters used as catalyst acting as preferential site on the substrate surface for the vapour deposition. They can be formed after a dewetting process on a metallic thin film, as explained before, or

metal nanoparticles can be dispersed on the substrate prior to the growth. The clusters are in liquid phase because the synthesis is carried out above the eutectic temperature of the metal-semiconductor system. The vapour is rapidly adsorbed by these liquid droplets and the solute supersaturates the eutectic until precipitation occurs, leading to the nucleation of a crystalline phase. The growth proceeds at the solid-liquid interface leading to an axial growth of an elongated structure. The metal nanoparticle has a larger sticking coefficient than the semiconductor surface, therefore this method allows lower growth temperature and a faster growth rate than direct growth on solid surface from gas phase.

As shown in Figure 1.7, the gas phase precursor is incorporated in the liquid droplets and forms a solution. When supersaturation is reached, precipitation occurs and the growth takes place.

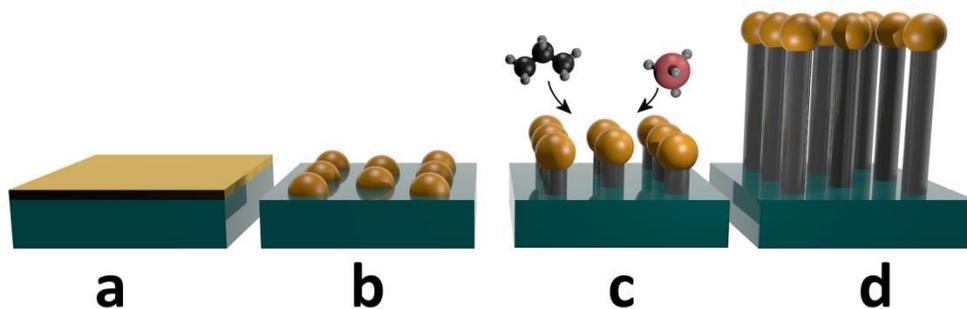


Figure 1.7: schematic view of the dewetting process followed by a VLS growth mechanism for the synthesis of SiC nanowires. (a) A substrate is covered with a thin film of the catalyst material. (b) Temperature is raised and the dewetting occurs: the catalyst melts and forms small droplets on the surface. (c) The precursors (in this case silane and propane are depicted) are incorporated into the droplets and growth occurs. (d) The final result is a nanowires array with catalyst particles on top in case of a “float growth” process.

The larger sticking coefficient of the nanoparticle can be due to many different reasons: liquid surface can have a large accommodation coefficient compared to an H-terminated silicon surface or even to a generic solid surface. Sometimes, like the case of silanes, metals have a catalytic action on the gas precursors, and that’s the reason for a greater dissociation rate on the particle compared to that on the sidewalls [99]. Often the energy barrier for new material incorporation in the crystalline wire is lower at the liquid-solid interface than on the solid-gas interface on the sidewalls.

What appears to be critical is to have a lower nucleation energy barrier at the nanoparticle/wire interface in order to obtain an axial growth.

The droplets size has a direct influence on the final diameter of the nanowires [101] and on growth kinetics as a manifestation of the Gibbs-Thompson effect [108]. This explains how the curvature of an interface can affect the chemical potential of a body:

$$\Delta\mu = \Delta\mu_0 - \frac{4\Omega\alpha}{d} \quad 1.3$$

where $\Delta\mu$ is the supersaturation of the droplet, which is the growth driving force, $\Delta\mu_0$ is the difference between the chemical potential of the precursor in vapour phase and in solid phase (inside the nanowire), Ω is the atomic volume of the precursor specie, α is the surface free energy of the wire and d is the diameter of the droplet. This means that the solubility of a specie in a catalyst particle becomes dependent of the particle size when the diameter is small enough. As a general consequence, starting from bigger particles leads to faster kinetics in nanowires growth.

Since the first study of VLS by Wagner and Ellis [104] researchers have been synthesizing silicon carbide wires or whiskers exploiting this growth mechanism [105], [106], [109] but only many years after some “nano” sized object were obtained [93], [110].

The nanoscale size turns out to be critical for some structural characteristic of silicon carbide nanowires, such as the crystallographic orientation, strongly dependent on the nanowire diameter.

The most common growth direction for VLS growth mechanism in SiC literature is the nanowire axis parallel to $\langle 111 \rangle$ crystallographic orientation, but in some cases also $\langle 100 \rangle$ direction has been observed [111]. This is strongly dependent from the diameter, since crystallographic orientation of the nanowire is driven by the minimization of the total free energy. The contribution to the total free energy are the bulk energy of the nanowire, the surface energy of the interface between liquid catalyst and nanowire and finally the nanowire surface in vacuum (similar to that in gas atmosphere). With small nanowire diameters the surface energy of the

NW in vacuum is dominating but, for bigger diameters, the contribution of the surface free energy of the interface between the semiconductor and the metal catalyst becomes predominant [112], [113].

Vapour-solid-solid growth mechanism

In many cases nanowires growth was observed at temperatures far below the eutectic point of the semiconductor-metal system [114]. The melting point of a small body is smaller than the corresponding bulk [115], but in some cases the low temperature used and the size of the nanoparticles exclude the possibility for these particles to melt [116], [117].

In some circumstances [118] this phenomenon was explained with a growth mechanism very similar to the VLS, but presuming the diffusion through or around the solid catalyst nanoparticle. In general, when an axial growth is nourished from gas phase and catalysed by a solid particle the growth mechanism is called vapour-solid-solid.

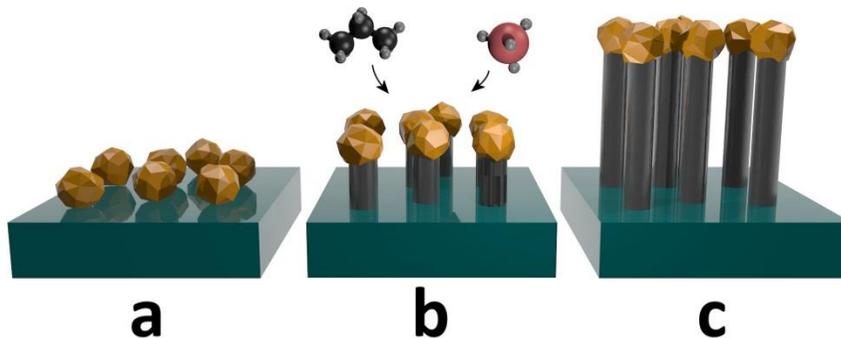


Figure 1.8 Scheme of the VSS process. Solid particles deposited on the substrate prior to the growth (a) act as nucleation sites for the gaseous precursors (b) and cause the growth of the nanowires (c).

It is hard to find a strict borderline between VLS and VSS, since the catalyst nanoparticle act as a nucleation point in both cases and there are many examples in which the structure of the nanowires seems not to be affected by the catalyst phase [99].

Vapour-solid growth mechanism

The presence of a catalytic specie isn't always necessary, since many other factors can induce an axial growth. The nucleation probability P_N on the surface of a whisker is related to thermodynamic variables and to crystallographic parameters:

$$P_N = B \exp\left(-\frac{\pi\gamma^2}{k^2T^2 \ln \sigma}\right) \quad 1.4$$

(after Dai et al. [119] and Sears [120])

where B is a constant related to the material, γ is the surface energy of the solid, k the Boltzmann constant, T is temperature and σ the supersaturation ratio:

$$\sigma = \frac{p}{p_0} \quad 1.5$$

Where p is the actual partial pressure of the vapour specie and p_0 is the equilibrium partial pressure at temperature T.

This means that the nucleation probability is related to γ , the surface energy of the solid, which can change for different crystallographic planes. An anisotropic growth can therefore be caused by a wide disparity between the surface energy of different crystallographic planes of the nanowire and the consequent surface energy minimization

Owing to the high temperature of an epitaxial process, incoming adatoms have high energy on the substrate surface and high mobility as a consequence. The motion of these adatoms stops when a point with lower surface energy is reached, in this way defects or impurities can act as nucleation points for a uniaxial growth. The typical example, also depicted in Figure 1.9, is the growth starting from a screw dislocation [121], propagating axially until the formation of a helical SiC nanowire [122], [123].

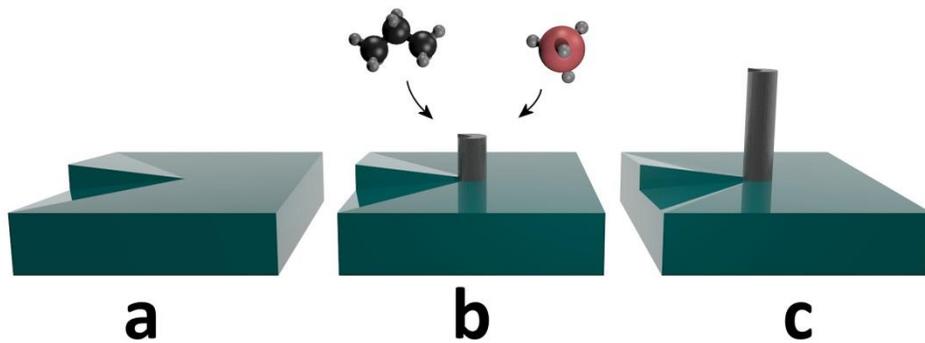


Figure 1.9: A screw dislocation on a crystalline substrate (a) can act as nucleation site for the uniaxial growth from vapour phase (b). The nanowire itself acts as the propagation of the dislocation (c).

The possibility of growing catalyst free SiC nanowires [124] can be an advantage: the presence of a catalyst (usually a metal) on the nanowires can be deleterious for electronic applications and this is the reason why catalyst-free growth mechanisms are studied.

Other growth mechanisms and techniques

In the **Solid-Liquid-Solid** mechanism the precursor is provided from the (solid) substrate (see Figure 1.10). In the case of SiC, the silicon substrate is the source of SiC. A metal rich catalyst remains at the base of the nanowires and it is the vehicle for the reaction between the silicon of the substrate and the carbon provided from a carbon-rich catalyst like Ni-C [125] or Fe-C [126] or from vapour phase [127]. In the latter case the mechanism can be defined as an hybrid of SLS and VLS. The SLS has always been observed as a root growth because at least one of the precursors must be continuously provided from the substrate. This is the reason because the term “root growth” is sometimes erroneously used as a synonym of SLS, but some VLS mechanism with root growth were also observed [99], [128].

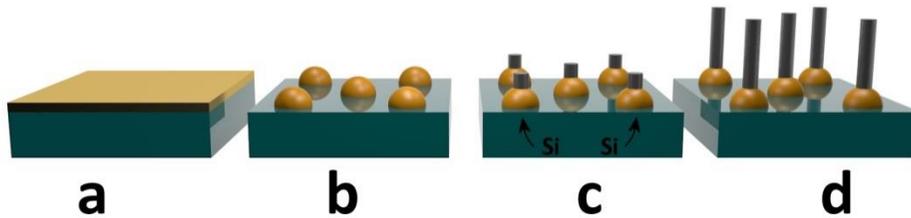


Figure 1.10: general scheme of a dewetting process followed by a SLS mechanism. (a) A thin film deposited on the substrate prior to the growth melts and forms droplets (b) on the surface. Both the precursors or only one (E.g. Silicon in the case depicted above) are provided from the substrate (c) and promote the growth of the nanowires from the bottom. The final morphology (d) is showing the root-growth mechanism with the catalyst particles at the bottom of the wires.

Other techniques than CVD are gaining attention for their relative simplicity: the **polymers conversion** into SiC nanowires allows to obtain big quantities of nanowires. Some polymers used as a precursor contain both carbon and silicon and can origin the SiC nanowires. The uniaxial growth can be obtained thanks to the presence of a catalyst like Fe (Feng, Ma, & Yang, 2012; G. Li et al., 2009). The starting material can also be prepared via **sol-gel** process and treated with **carbothermal reduction** to obtain the SiC growth [129]. Frequently in these cases the mechanism is still VLS, but the precursors are not provided in gaseous phase with a CVD apparatus.

The so-called **top-down** approaches for the fabrication of SiC nanowires have proven to be valid alternatives to more traditional techniques. The microfabrication methods are well established for silicon and they allowed to obtain short gate length MOSFET using Si NWs [130], but silicon carbide has a strong resistance to chemical etching and plasma etching is not straightforward as well. Nevertheless, inductive coupled SF_6/O_2 plasma etching proved to be suitable to obtain nanopillars with aspect ratios of about 1:7 [131]. The employment of top-down techniques has several advantages like the possibility to have well-ordered structures with uniform diameter and length. Further development of the Bosch/STS process [132] might obtain nanostructures with higher aspect ratios.

Using a target made of SiC as the starting material under the action of laser (**laser ablation**), it is possible to have evaporation and condensation to form nanostructures on a cold finger [133].

Using **arc discharge**, it is possible to obtain SiC nanostructures with an hole anode made in graphite with inside silicon carbide powder and pure graphite as cathode to reach high temperature [134], [135].

Although the aforementioned methods are the most used, other techniques to obtain nanowires such as **direct chemical reaction** at low-temperature and high-pressure [136] have been developed. To enter in the details of these techniques is beyond the aim of this work.

While all of the mentioned synthesis method are used to obtain SiC nanowires, many of them allows to obtain more complex nanostructures based on SiC nanowires, such as core-shell structures obtained with self-assembled growth mechanism [137] or by multiple steps procedure such as CVD, carburization, etc. [138].

1.7.2 SiC nanowires applications

As other nanostructures, nanowires exhibit outstanding properties not possessed by their bulk counterparts. The effect of the reduced size along two dimensions on the mechanical properties was measured on nanowires of different materials [139]. Basing on the excellent mechanical properties of bulk silicon carbide one can infer that its nanostructured counterpart might show remarkable mechanical properties: nanomechanical studies observed indeed a super-plasticity of the NWs [140], but even before this discovery one of the first applications of SiC NWs was as reinforcement for **composite materials**.

SiC nanowires embedded in a polymer matrix [141], [142] sensibly enhance tensile strength and bending strength of the composite. Ceramic/SiC composite were studied [143] with a measurable enhancement of properties like thermal conductivity, chemical and thermal stability. Even SiC/SiC composite were fabricated [144] and superior mechanical properties were found.

The use of nanowires as **field emission transistors** (FET) is another promising application to obtain small electronic semiconductor devices suitable to develop sensors [145]. From the first attempts [146], [147] many improvements have been achieved to obtain better performances, but still many issues have to be overcome, like obtaining ohmic or rectifying behaviour of metal contacts

deposited on SiC depending on the need is not trivial but it is essential to fabricate NW FET [148]. Another problem is the control of n or p type doping of the channel [149]. The unintentional doping level measured to-date in the SiC NWs is still too high to use ohmic contacts as source and drain, because it is impossible to fully deplete the nanowire in the off state, so Schottky barrier contacts are still needed to have satisfactory device performances [150].

Other interesting applications of SiC NWs are the use as **microwave absorbers** to avoid electromagnetic interference [151], as electrodes for **micro-supercapacitors** [152] to be used as energy source for micrometric devices or as **anode material** for lithium ion batteries showing increased capacity and lifetime thanks to the ability to retain the integrity over multiple charge-discharge cycles [153].

The use of nanowires for **nanoelectromechanical** devices [154] must be mentioned and the field emission properties of SiC nanowires [155] make SiC NWs very promising for electron-emitting device applications (displays, etc.).

Semiconductor nanowires are widely studied as **catalyst supports**, photocatalysts and electrocatalysts for the high surface to volume ratio. The quest to find new supports for catalytic active phases is gaining increasing attention for the possibility to pave the way to new industrial processes or improve the yield of the existing ones. The advantages of using silicon carbide instead of traditional supports like alumina are linked to the chemical inertness of the material, both because the support has to withstand reaction in sometimes harsh chemical environment to allow the recovery of the active phase at the end of catalyst lifetime and because any chemical interaction between the support and catalytic active phase may lead to a decrease in the catalyst performance [156], [157]. Moreover, the good thermal SiC conductivity can help in dispersing the heat formed during the reaction. One of the drawbacks of the well-established alumina support is its thermal insulation leading to the formation of hot spots that may hinder the catalytic process. Even if these problems regarding alumina can be partially overcome using carbon based supports which are suitable for certain processes, the weak resistance to oxidation of the latter pushes towards the investigation of more inert materials.

The use of more conventional SiC structures as catalyst support is nowadays well developed and there are companies (SICAT <http://www.sicatcatalyst.com>) already using them for industrial processes such as coal/gas-to-liquid, Fischer-Tropsch,

methane conversion, selective oxidation, selective hydrogenation, biomass conversion, waste water purification and photocatalysis. Using nanowires might lead to higher yield owing to the superior surface-to-volume ratio.

SiC nanostructures proved to be an excellent support for Ni catalyst in low temperature selective oxidation of H₂S into elemental sulphur [158], [159], Pd nanoparticles for methanol combustion [160]. As a support of noble catalyst as Pt and Pd, SiC NWs are also studied for fuel cells applications [161], [162].

Many research groups have been studying SiC NWs as **active catalyst**. Zhou et al [163] found that SiC nanowires accelerate the photodegradation of acetaldehyde under UV irradiation. SiC NWs proved to be a valid photocatalytic agent for water splitting under UV or visible irradiation for hydrogen production [164], [165].

The excellent biocompatibility of silicon carbide [10] encouraged many research groups to focus on **biomedical applications**. SiC nanocrystals (quasi-one-dimensional) already demonstrated to be excellent labels for bioimaging [166] and the in-vitro studies of the cytocompatibility of core-shell SiC-SiO₂ nanowires [2] encourage to use SiC nanowires in medical nanosystems. SiC NWs seem to be promising also as biosensors: the well-known silicon functionalization chemistry allowed Fredetal et al. to functionalize SiC nanowires with desoxyribo nucleic acid [167] and to use them as FET sensor for DNA detection [168]. Williams et al. demonstrated the possibility to functionalize silicon carbide nanowires with streptavidin protein thus creating a NW-based sensing platform for the multiplexed electrical detection of bioanalytes [169].

My research group studied a system based on SiC/SiO₂ core-shell nanowires conjugated with an organic photosensitizer, a tetracarboxyphenyl porphyrin derivative, to be used as oxidizing agent for photodynamic therapy in cancer treatments [3].

1.7.3 Open issues

As demonstrated, the research progress on SiC nanowires are strictly connected to achievements in many other fields such as fundamental physics or biotechnology. Thanks to the interesting silicon carbide properties coupled with

those of one dimensional nanostructures many promising applications may emerge in the future.

Nevertheless, even if preliminary experiments at laboratory level are very promising and fruitful, scaling the technologies up to industrial production keeping the unique peculiar properties is still a challenge. The assessment of a single nanowire properties is a hint on the material properties but collective properties may be also sensibly different and unpredictable.

Chapter 2 - Development of SiC thin film deposition technique

The performance of SiC based devices is still limited by the crystalline quality of the synthesized material and this issue is more critical for SiC than for other wide bandgap semiconductors such as gallium nitride. The growth of high quality cubic silicon carbide films on silicon substrates still remains an open challenge. The final goal is to find a cheap technique that ensures a high growth rate of a single crystalline material with defect density low enough to have high performance devices.

Since the growth of large area single crystal 3C-SiC has not been demonstrated so far, heteroepitaxy is still needed to grow cubic silicon carbide crystals on a large area. Chemical vapour deposition over silicon substrates is not surprisingly the most used technique to obtain 3C-SiC, because other approaches such as liquid based growth techniques or molecular beam epitaxy in this case face many problems in terms of crystalline quality, growth rate and purity. A short review of the substrates used and the reason of the frequent choice of silicon as substrate is reported in the previous section. The complete description of 3C-SiC growth techniques is beyond the aim of this work and it can be found in good textbooks[11]. The following discussion will be focused on the synthesis technique developed at IMEM-CNR institute in Parma i.e. Vapour Phase Epitaxy (VPE) on silicon.

The introduction of hot wall reactors in 1993 by Kordina et al. [170] allowed to obtain thick SiC layer with a low unintentional doping and a good crystalline quality, which are essential for the fabrication of high voltage power devices. The following development of hot wall reactors has brought to state-of-the-art industrial machines which ensure high growth rate and throughput. At the present time, non-intentional doping ranges of 10^{14} cm^{-3} and growth rates of $10 \mu\text{m/h}$ have been achieved. In addition to that, wafer rotation, which ensures layer thickness homogeneity is now a standard in commercial reactors manufactured by various producers. Thickness uniformity better than 3% is now available on 3 inches wafers in modern reactors [171].

The growth of cubic silicon carbide on silicon substrates in this work is obtained using vapour phase epitaxy (VPE) in a home-made horizontal hot-wall reactor radio frequency heated developed in IMEM-CNR institute in Parma since 2005 [172], [173].

2.1.1 VPE reactor

The reaction chamber consists in a quartz tube supported by water cooled stainless steel flanges. An inner quartz tube funnels gaseous precursors into the graphite chamber (the hot zone). Water-cooled copper coils around the quartz tube carry alternate current (8-9 KHz) which generates radiofrequency induction on the conducting graphite chamber. Eddy currents are generated only in the graphite susceptor which is electrically conductive, while all the other components inside the coils are insulating. This system can reach temperatures higher than 1500° C, but the reaction temperature is limited by the choice of silicon substrates, whose melting temperature is 1414°C. Temperature control is obtained by an S type thermocouple in a recess inside the graphite susceptor. The hot zone consist of the graphite susceptor covered by a graphite tunnel and an insulating graphite foam which encapsulates and supports the assembly. The graphite foam helps in obtaining a good thermal insulation thus maintaining temperature uniformity and preventing radiation losses.

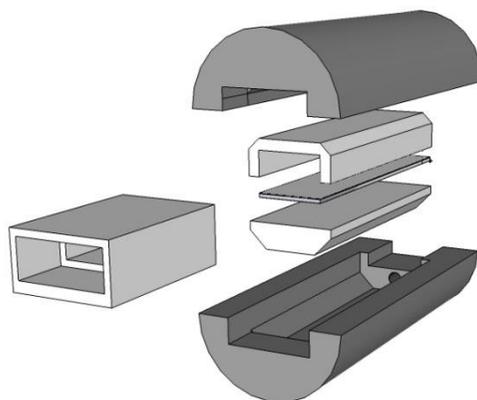


Figure 2.1: exploded-view drawing of the reactor hot zone. In dark grey the graphite foam parts, while in light grey the graphite parts.

Silane (SiH_4) and propane (C_3H_8) are used as precursors and palladium purified hydrogen is the carrier gas. In the current configuration, helium or argon can be used as carriers as well. A dry vacuum pump ensures pressure tuning in the growth chamber from 40 mbar to atmospheric pressure. In addition to that, a thermostatic bath with methyltrichlorosilane (CH_3SiCl_3) can add this organosilicon compound to the precursors (more details are provided below). Two doping lines, one with gaseous nitrogen for n-type doping and one with trimethylaluminium ($\text{Al}_2(\text{CH}_3)_6$) for p-type doping were added to the reactor and tested during this work.

After the hot zone, the exhaust gas is funnelled into a tube and brought to a cracking furnace set at 850°C , to ensure the complete decomposition of toxic precursors (silane, methyltrichlorosilane and trimethylaluminium). The operator must be sure that the cracking furnace reaches the working temperature before introducing toxic precursors in the reactor. Active carbon filters ensure that even in the case of a malfunction of the cracking furnace, no toxic compound can be released by the system.

2.2 Process development

The silicon carbide heteroepitaxial process developed during this thesis work starts from a process already established with a cold-wall configuration using the same reactor but at lower temperatures (1100°C) and without intentional doping [173]–[175]. In order to obtain 3C-SiC layers with high crystallinity, flat surface, and low defect density the growth temperature in literature is usually close to the silicon melting point (1414°C). The standard 3C-SiC deposition processes are carried out at about $1350\text{--}1380^\circ\text{C}$ [11]. Lower deposition temperatures ($1000\text{--}1200^\circ\text{C}$) are also employed but the resulting film, even if it is suitable for MEMS realization, generally has poorer crystal quality and rough surfaces and may not be suitable for advanced (bio)sensor devices or graphene synthesis, which requires a very flat and perfect surface.

The aim of the work was to increase the growth rate and obtain a diminution of defect density and to obtain a control over in-growth doping level. As said, the large mismatch of about 20% between Si and SiC lattices and 8% difference in thermal expansion coefficients generate most of the defects in 3C-SiC

heteroepitaxy on silicon. One of the key points is then to optimize the interface in order to get rid of the defects or, at least, to relegate them near to the interface. Moreover, the strain generated at the interface can be detrimental for MEMS development. In order to obtain the release of the strain due to lattice mismatch and consequently the defect density reduction in the epitaxial film, a carbonization layer and a buffer layer are deposited prior to the growth of the final SiC layer. In Figure 2.2 a graphical scheme of the layers is reported, more details on the fabrication procedures are described in the following.

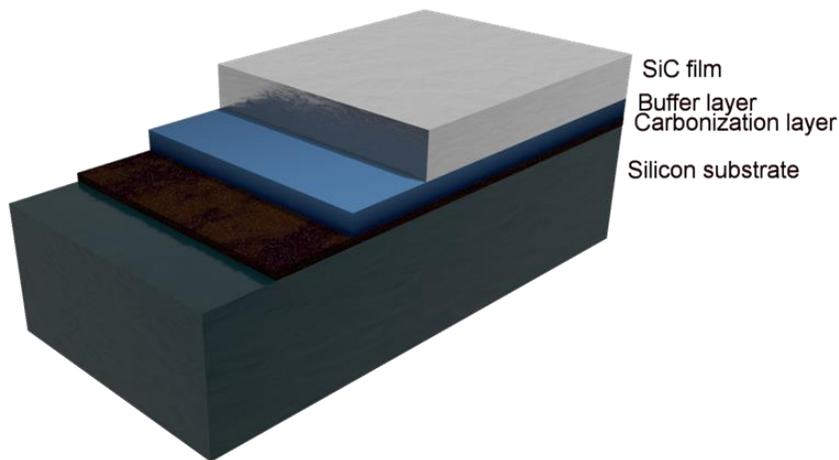


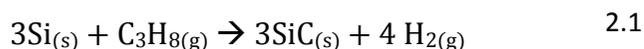
Figure 2.2: scheme depicting the different layers fabricated during SiC heteroepitaxy on silicon.

2.2.1 Carbonization process

In the early eighties, the group of prof. Nishino (NASA) demonstrated that the introduction of a carbonization layer, obtained with the exposition of Si substrate to the carbon precursor at high temperatures, could significantly improve the SiC layer crystalline quality [23]. The carbonization layer, also called buffer layer in Nishino work, proved to be much more effective than previous techniques, like SiC sputtering [176] to obtain good epitaxial films quality. A SiC thin film growth without this step may result in rough layer composed of many grains. Using XRD it is easy to verify that the result of a SiC heteroepitaxy on silicon without carbonization and buffer layer is a polycrystalline film [28]. This is probably caused by the high reactivity of the silicon substrate at high temperatures. It is essential

to stabilize the surface prior to the epitaxial growth. Hydrogen itself act as etchant on the silicon surface at high temperatures, that's the reason why the best results are obtained introducing the carbon precursor from RT (room temperature) during the heating.

Frequently, it is easy to know the initial species and the resulting ones in a VPE synthesis, but it is more difficult to identify the intermediate chemical reactions. In the case of propane, the overall carbonization reaction can be written as:



The actual reaction taking place during the carbonization step is more complex: hydrogen may act as reducing agent on propane, generating ethane or methane, so the real reaction is a sum of partial reactions involving propane and hydrogen [28].

The limit of carbonization step is the low diffusion coefficient of many species (in this case carbon) inside silicon carbide. After a fast carbonization of the first layers, the process drastically slows down when a SiC layer of 2-3 nanometres is reached and the SiC layer acts as a diffusion barrier for further carbon incorporation in the underlying silicon substrate. This fact can be seen as an advantage since, as a collateral result, the interface between Si and SiC is extremely abrupt without any visible sub-stoichiometric $\text{Si}_x\text{C}_{1-x}$ phase or Si-SiC intermixing [28]. This detail can be important for small scale MEMS.

In this work, the optimized carbonization step was obtained by flowing 4000 sccm of H_2 and 200 sccm of C_3H_8 during a 15 minutes linear heating ramp rate from RT to 1125 °C. The pressure was set at 700 mbar for the entire duration of the ramp and once reached 1125 °C the temperature was held constant for 5 minutes to complete the carbonization step.

To analyse in detail this step, the growth was interrupted immediately after the end of the carbonization. The sample was cut to fabricate a "sandwich" for TEM cross-section investigations and another part was analysed using XPS (X-Ray Photoelectron Spectroscopy). The sample was glued inside a sandwich made with two slabs of silicon. The sandwich was mechanically grinded down to 30–40 mm and subsequently thinned to electron transparency by Ar ion beam

bombardment. The result of our carbonization procedure was a macroscopically mirror-like surface and TEM analysis (Figure 2.3) shows that Si substrate was actually converted in SiC with a thickness of 4 - 5 nm. The Selected Area Electron Diffraction (SAED) pattern clearly shows the diffraction spots of SiC along with those of Si and it is important to emphasize that the SiC layer is smooth, densely packed, and no holes/pits were evidenced at the SiC/Si interface.

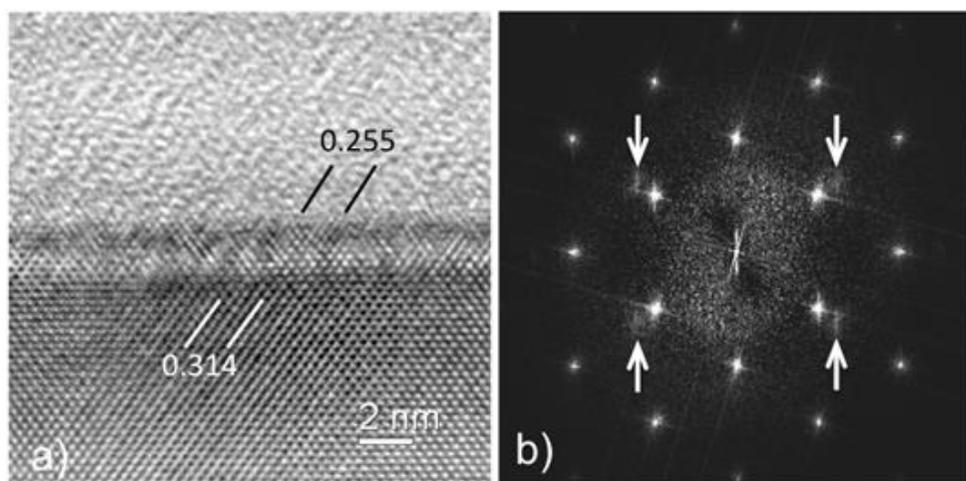


Figure 2.3: a) High resolution TEM image along a $\langle 110 \rangle$ cross section of a carbonized silicon substrate. From the bottom it is possible to observe the silicon substrate, the carbonization layer and an amorphous layer at the top used for the cross-section. In black the distance between two SiC (111) planes is reported (0,255), while in white the distance between two Si (111) planes (0,314 nm) is reported. The distance between the segments is 6 planes in both cases. b) Fast Fourier Transform of image a) showing the reciprocal lattice. The strong diffraction peaks correspond to silicon, while the weak $\{111\}$ Bragg spots of SiC are indicated by arrows, confirms the formation of a carbonized layer.

XPS analysis (Figure 2.4) confirmed the uniform carbonization of the whole substrate. In Figure 2.4 high resolution (PE = 10 eV) spectra centred C1s and Si2p are reported. C1s main peak is at 283.00 eV (FWHM=1.05eV), in the same energy range already found for similar peaks from the thickest growths. This proves the presence of a crystalline SiC layer already after this step, together with a small peak around 285.4 eV caused by residuals of air carbon contaminations. The Si 2p is composed of different contributes: 99.35 eV representative of Si-Si species and 103.35 eV linked to Si-O species, probably caused by residuals of native oxide,

while peaks at 100.64 eV (FWHM=1.12eV) and 101.85 eV are related to the SiC film. The thinness of the SiC layer after a carbonization step allows the analysis to concern both layer and substrate, since the attenuation length of photoelectron is in the order of 1nm.

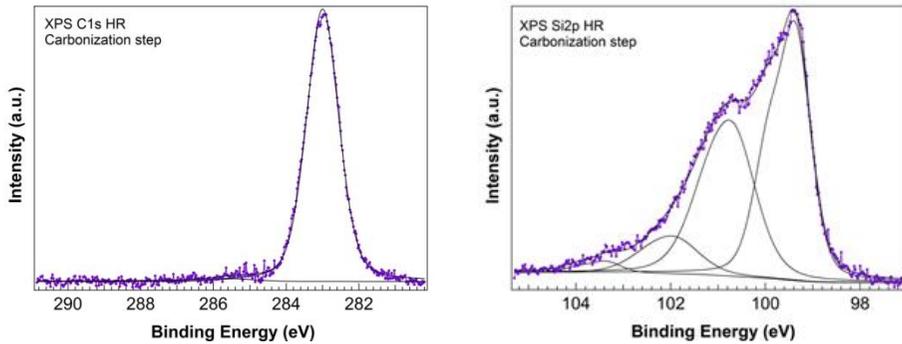


Figure 2.4: XPS high resolution spectra centred on C1s (on the left) and Si2p (on the right) peaks of the carbonization layer

The aforementioned carbonization procedure was found to be optimal for the growth of thick SiC layers, therefore it was used as “standard” for all the subsequent depositions and trials.

2.2.2 Buffer layer

The deposition of a low temperature buffer layer (BL) is a technique used for heteroepitaxy of many materials when there is a lattice mismatch between the substrate and the epi-layer.

The goal of the buffer layer is the strain reduction by relieving the lattice mismatch and, as a consequence, an increase of the epitaxial layer quality. Moreover, the growth of 3C-SiC is carried out at temperatures close to silicon melting point, but the heating from carbonization temperature to growth is crucial for the good epitaxial layer quality. In hydrogen atmosphere silicon etching and outdiffusion is promoted at high temperatures, so to hinder this phenomenon, silane is added in gas phase. If no care is taken during this step, the carbonization layer may deteriorate and create voids (see dedicated paragraph in defects dissertation).

To demonstrate this, a synthesis **without any BL** was carried out. The reactor pressure was lowered to 200 mbar and temperature was raised to 1380° with a fast heating ramp (60-80 °C/min) without reagents, only the carrier gas (hydrogen) was provided. Many recipes were tried with different Si/C ratios ranging from 0.6 to 1.6 but the resulting film was macroscopically hazy, with a milky, not mirror-like surface. In the XRD spectra it is possible to identify only the (111) peak, thus indicating that the resulting film isn't epitaxial with the substrate and it has not the same crystallographic orientation.

An important step is to reduce reactor pressure during the BL in order to reduce the tendency of silicon to react in the gas phase and to form precipitates [28], on the other hand, the problem of etch pit formation is more pronounced.

To try **different BL recipes** we divided the process in three steps:

1. From carbonization (1125°C) to 1240°C
2. From 1240°C to 1280°C
3. From 1280°C to film growth temperature (1380°C)

We carried out synthesis with different recipes up to these set points and suspended the growth to analyse the results using morphological and structural analysis techniques. The parameters that we varied were the heating ramp (degrees per minute) and the precursors flow (sccm). In all the recipes the carbon-to-silicon ratio was held constant and equal to one ($[Si]/[C]=1$), as it is in silicon carbide crystal.

First step: from carbonization (1125°C) to 1240°C

Using the same fast heating ramp (60-80 °C/min) up to 1240°C but adding the silicon and carbon precursor we still obtained a milky and not mirror-like surface. TEM cross-section observation revealed a high density of holes and pits at the SiC/Si interface, as also reported in literature [177]. As previously said, voids are attributed to silicon outdiffusion from the substrate through the silicon carbide layer. It is therefore important to "seal" the substrate with a uniform, dense and monocrystalline SiC layer as soon as possible. The thin layer obtained after the carbonization step may not be enough and a non-optimal coalescence between SiC islands or mutual disorientation of micro-crystallites nucleated on the carbonized Si, could act as preferential channels for Si diffusion from the substrate, thus promoting the formation of pits [178].

We thought that a slower heating ramp may have been a good solution to the problem. Two different heating ramps and two different precursors flow were tested:

- 21,5°C/min “**slow ramp**”
- 25,5°C/min “**fast ramp**”
- SiH₄ = 17 sccm and C₃H₈ = 6 sccm “**low flow**” regime
- SiH₄ = 27 sccm and C₃H₈ = 9 sccm “**high flow**” regime

Naked eye observations after the first buffer layer step revealed that using a slow ramp and both with low and high flow regimes an evident enhancement of sample quality was achieved: the haziness previously observed completely disappeared. Thanks to AFM investigation (Figure 2.5) it was possible to have a more quantitative analysis of grain size and uniformity. The nucleation of smaller grains and islands with dimensions of about 200 – 300 nm is promoted with higher flow regimes, while larger grains and an increased surface roughness are the results of a low flow regime buffer layer.

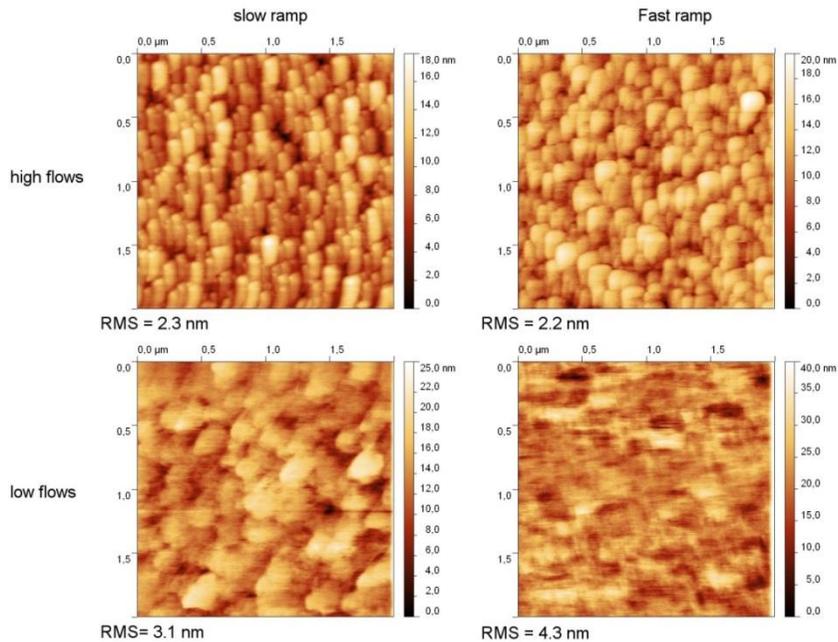


Figure 2.5: AFM images of buffer layer obtained with different growth conditions after the first step (1240°C). X and Y scale are maintained, while Z scale is different for every sample in order to enhance the contrast.

Second step: from 1240°C to 1280°C

Keeping the same recipes as the first step and using them for the second step produced a degradation of surface morphology, so we had to find a different optimal recipe for this step. Many reasons can be behind this result: with the temperature increase, a higher precursor cracking rate is expected and a faster depletion of SiH₄ and C₃H₈ is a direct consequence. In order to maintain a sufficient growth rate to grow a high quality SiC buffer, the flows in the second step must be increased:

- 21,5°C/min “**slow ramp**”
- 25,5°C/min “**fast ramp**”
- SiH₄ = 34 sccm and C₃H₈ = 12 sccm “**low flow**” regime
- SiH₄ = 48 sccm and C₃H₈ = 16 sccm “**high flow**” regime

To enhance the precursor transport and delay precursors cracking, the carrier gas flow was increased to 2500 sccm in this step.

A slow ramp ensured a mirror-like sample surface, while a fast heating ramp, regardless of precursors flow, brought to a milky, hazy film.

Third step: from 1280°C to film growth temperature (1380°C)

For the aforementioned reasons, to compensate the precursors depletion, it was necessary to increase the flows again in the third step:

- 21,5°C/min “**slow ramp**”
- 25,5°C/min “**fast ramp**”
- SiH₄ = 51 sccm and C₃H₈ = 18 sccm “**low flow**” regime
- SiH₄ = 72 sccm and C₃H₈ = 24 sccm “**high flow**” regime

A higher temperature means also a faster precursors cracking and, to compensate the consequent precursors depletion gradient, the carrier gas flow was increased to 3300 sccm.

As in the other steps, the slow ramp ensured good results, regardless of the flows, while the fast heating ramp resulted in pits formation, that could be noticed by naked eye from the milky, hazy surface.

Process analysis and comparisons

A recapitulation of the three different steps, the corresponding precursors flows and the carrier flow is reported in Table 2.1.

Table 2.1: Prospect of the precursors flows used un the three buffer layer steps. Flows are reported in sccm.

	First buffer step 1125 - 1240 °C		Second buffer step 1240 - 1280 °C		Third buffer step 1280 - 1380 °C	
	SiH4 flow	C3H8 flow	SiH4 flow	C3H8 flow	SiH4 flow	C3H8 flow
Low flows	17	6	34	12	51	18
High flows	27	9	48	16	72	24
H ₂ carrier	1600		2500		3300	

Analysing the step singularly, a **higher precursors flow and a slower heating ramp** ensured good results without pits formation on the substrate in each one of the three steps. For this reason, the surface of the samples obtained using this conditions was characterized using AFM after each step (Figure 2.6). Studying the evolution of the islands nucleated in the first step it is interesting to observe that there is a progressive enlargement, resulting in the formation of well-defined squared plateau about 200 nm wide and with almost flat top surface at 1380° C.

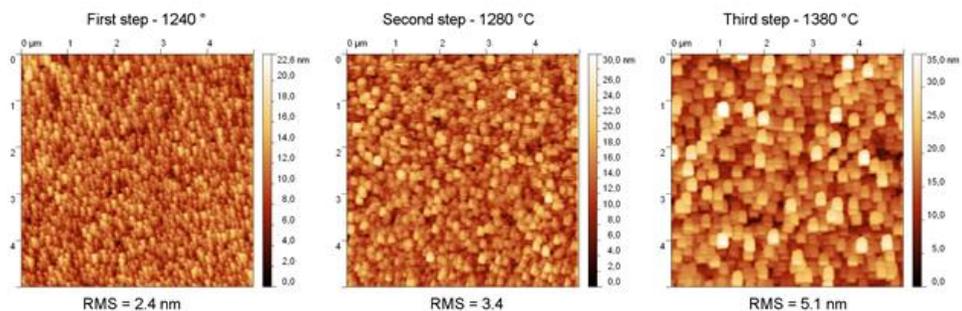


Figure 2.6: AFM analysis of the three buffer layer steps. The sample was obtained using slow ramp and high flows regime (called “sample B” in the following).

Nevertheless, for a better understanding of the overall process going on during the buffer layer obtained with different growth conditions, 4 samples were prepared completing all the buffer layer steps in the four possible combinations:

Sample A: low flows + fast ramp (25.5 °C / min)

Sample B: high flows + slow ramp (21.5 °C / min)

Sample C: low flows + slow ramp (21.5 °C / min)

Sample D: high flows + fast ramp (25.5 °C / min)

The flows were the same as previously reported in Table 2.1. The synthesis was halted at 1380°C, just before the film deposition, the samples were removed from the reactor and analysed. Optical investigation can be a direct, easy method to detect the presence of pits if their density is high enough. Optical microscope images, especially with the aid of optical colour filters clearly show the reduction of interfacial voids in samples obtained with slow temperature ramp (Figure 2.7), but for a deeper analysis SEM can be a suitable technique because the sample preparation and the observation are fast.

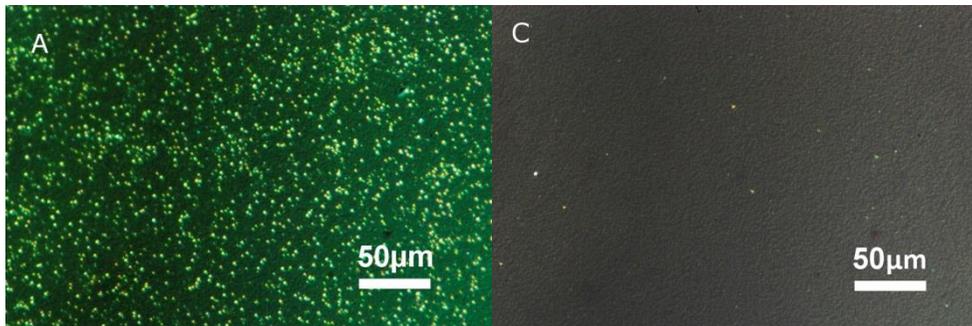


Figure 2.7: Optical microscope images of samples A and C

The samples were cleaved along (110) plane, the cross section was then analysed by SEM mounting the sample on a vertical sample holder. The secondary electron images collected on the four samples are reported in Figure 2.8. The different densities and electrical conductivity of SiC and Si help to locate the boundary between the silicon carbide film and the substrate. This technique can be a method to measure the film thickness but, more than that, it can give information on the pits density and size below SiC thin film. The samples obtained with a fast heating ramp in the buffer layer (samples A and C) exhibit a high voids density

(voids are indicated by red arrows in Figure 2.8) and the sample obtained with high precursors flow (sample D) presents pits with bigger size. From SEM analysis it is possible to state that the buffer layers obtained with a slow temperature ramp (like in samples B and C) have a lower pits density and also a smoother surface. From SEM observation it is difficult to observe differences between sample B and C, because in both cases the interface is good, and the precursors flow intensity seems to affect only the film surface.

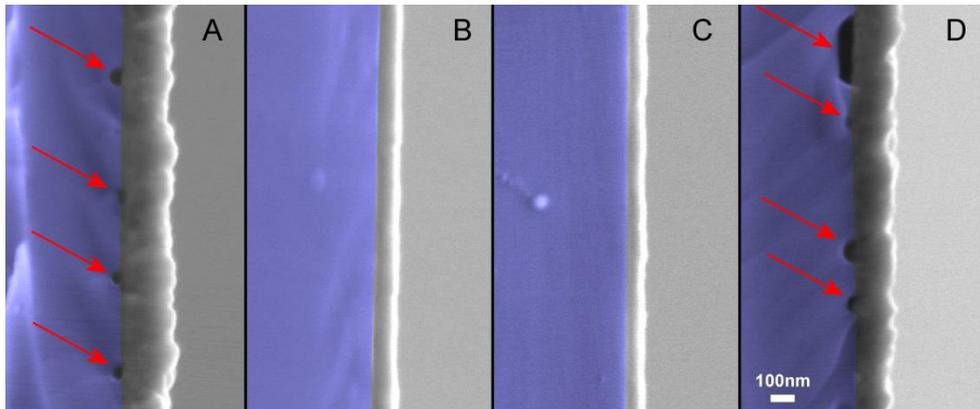


Figure 2.8: Secondary electron SEM image of cross-sections of the four samples obtained with buffer layer fabricated in different conditions as previously explained. The silicon substrate is highlighted using false colours (light blue) and the pits at SiC/Si interface are indicated by arrows.

SEM is a valuable tool to investigate the morphology of the different layers, but to deeply understand how the different growth condition affected the film structure, cross-sections of samples A and B were analysed using **TEM** (Figure 2.9). Different morphologies correspond in this case to significant differences in the structures. **Sample A** shows a high degree of polycrystallinity with a misoriented arrangement of the grains, a non-uniform thickness of the film and a high defect density. From the SAED pattern it is possible to identify a main orientation of the grain (with (100) planes parallel to those of the silicon substrate), but many other spot prove that other orientations are present too. In **Sample B**, on the contrary, the buffer layer appears perfectly (100) oriented as the silicon substrate, with uniform thickness and a smooth surface consisting mainly of plateau 200-300 nm wide, as observed using AFM. Planar defects like stacking faults and twin boundaries (see

previous chapter) are still present and their density is higher near to SiC/Si interface, as expected, due to lattice mismatch.

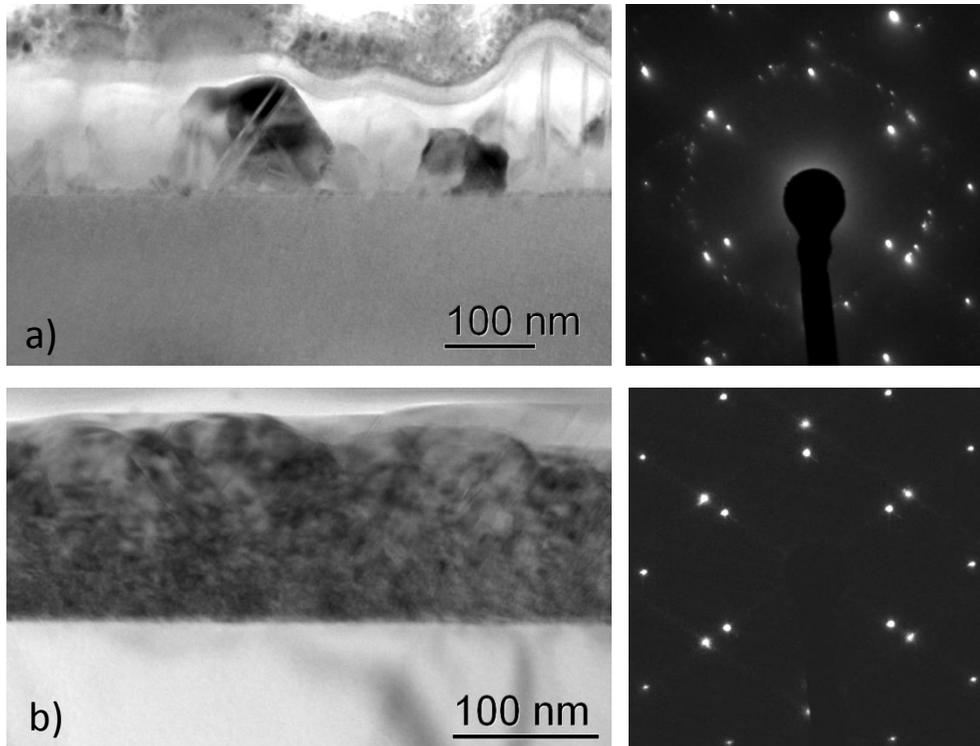


Figure 2.9: TEM cross-section images of the complete buffer layer after the three steps. Top: sample prepared using low precursors flow and fast ramp (sample A). Bottom: sample B prepared using high precursors flow and fast ramp. The corresponding SAED patterns are reported in the right panels. It is possible to observe SiC and Si diffraction peaks as the substrate was included in the SAED aperture.

Owing to the presence of big pits at the SiC/Si interface, sample D was excluded from further analysis. The comparison of **X-ray diffraction** between samples A, B and C (Figure 2.10) is very meaningful to show the crystalline quality of the buffer layers. The (111) diffraction peak is the most intense in SiC, so in a polycrystalline material, where all possible orientations are present, this is a residual peak that can be visible. The (111) peak is present in sample A spectrum, thus indicating the polycrystallinity of the film and the absence of an epitaxial relation with the substrate. In samples B and C a single (200) peak is found, indicating that the film has the same orientation of the (100) substrate. There is a remarkable difference

between sample B and C in the full width half maximum (FWHM) of the peak which is about 1400 and 1800 arcsec for sample B and C respectively. This is an indication of the higher crystallinity obtained with high flows regime in sample B.

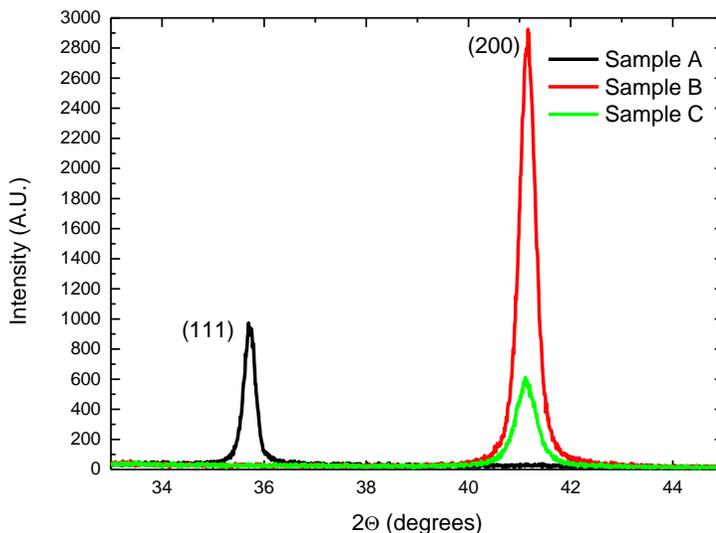


Figure 2.10: X-ray diffraction spectra of samples A, B and C. Only in sample A the (111) peak is present, while samples B and C spectra show an intense (200) peak.

2.3 Growth of 3C-SiC thin films

As described previously, varying the different synthesis parameters, the best results were obtained in sample B, so this process was used as a model for all the following experiments.

The process is summarized in Figure 2.11:

- A 15 minutes linear heating ramp allowed to reach the carbonization temperature (1125°C) and then temperature was held for 5 minutes. The pressure was set to 700 mbar with a constant flow of 4000 sccm of H_2 and 200 sccm of C_3H_8 for the whole step.

- b) The pressure was decreased to 200 mbar and temperature was raised with a linear heating ramp of 21,5°C/min varying precursors flows in three steps as described in Table 2.1 (low flows).
- c) The growth was carried out at 200 mbar pressure and 1380°C temperature. The “reference” process consisted of 30 minutes film growth with a carbon to silicon ratio of 0,7.
- d) The cooling was carried out down to RT in hydrogen atmosphere without silicon and carbon precursors and without a temperature ramp at low pressure (60 mbar).

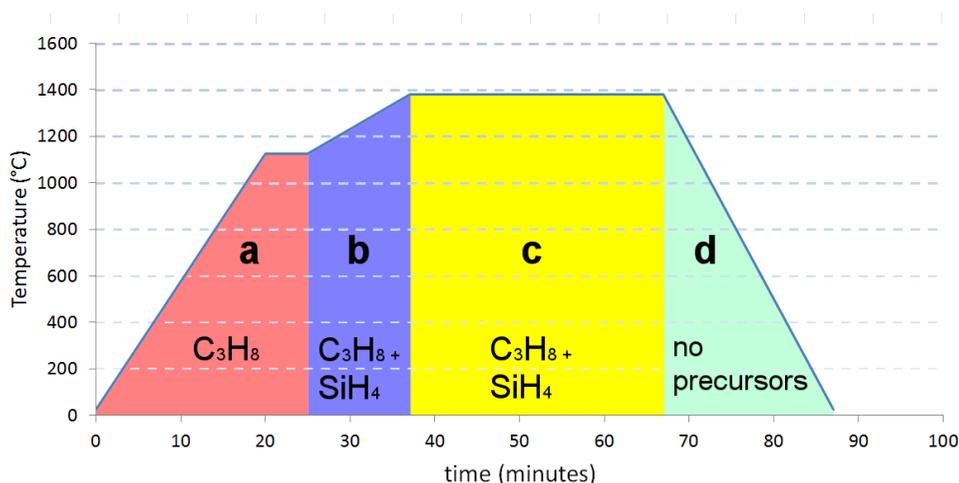


Figure 2.11: Graphical scheme of the ideal synthesis process based on “B” buffer layer. This was used as a reference for all the experiments.

2.3.1 Characterization

The naked eye aspect of the so-obtained thin 3C-SiC film is mirrorlike and coloured interference fringes suggest that there is a thickness gradient from inlet to outlet.

To assess the crystalline quality of the film, X-ray diffraction measurement were carried out (Figure 2.12) and the presence of a very intense (002) 3C-SiC peak at $2\theta=41,5^\circ$ with FWHM of about 790 arcsec, indicates a high quality monocrystalline film, comparable with the state-of-the-art [179]. The lack of (111) 3C-SiC peak

indicates the absence of randomly oriented grains with adequate size to give a measurable signal.

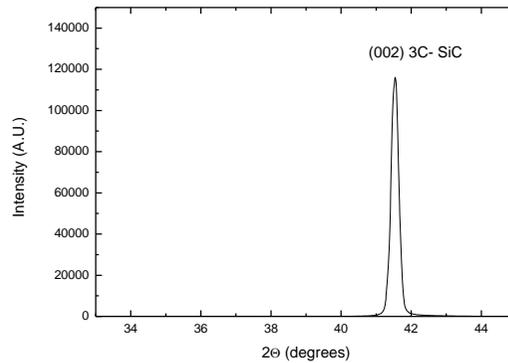


Figure 2.12: X-ray diffraction of the 3C-SiC thin film grown using the aforementioned process.

In order to understand the mosaic spread of the layer, if there is a misorientation between different grains of the crystal, the reciprocal lattice map (omega-2theta scan) can be a valuable technique. The result is reported in Figure 2.13 and the mosaic spread, which corresponds to the vertical section of the peak, has a measured value of about $0,3^\circ$. This fact indicates a very low misorientation of the mosaic domains with respect to the (100) direction.

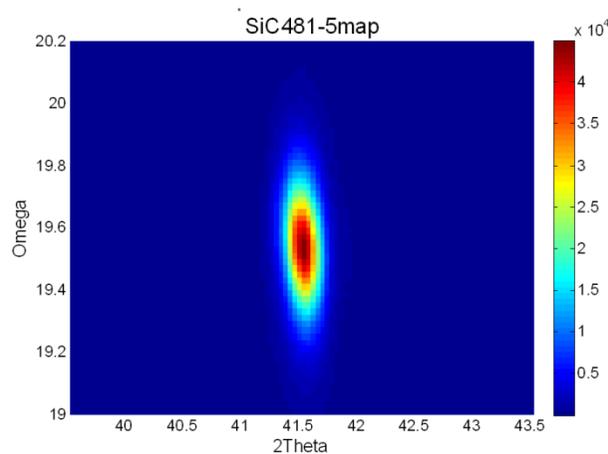


Figure 2.13: reciprocal lattice map around 002 silicon carbide node on the SiC thin film sample.

A high density of planar defects, mainly antiphase boundaries (APB) and twin boundaries (TB), at the SiC/Si interface is highlighted by TEM cross-section observations (Figure 2.14 a). It is well known that the formation energy of these defects is very low in silicon carbide (see section 1.3.2), so it is energetically favourable to create these defects in order to release the strain due to the high lattice mismatch between SiC and Si. However, as previously discussed, the annihilation of many defects like APB and TB has been observed in 3C-SiC. APB are eliminated by two factors: annihilation between two of them or crossing with stacking faults. Since the SF reverses the stacking order of Si and C, when an APB and a SF cross, the APB disappear at the junction with the SF. In Figure 2.14 b a high magnification TEM cross section image is reported and on the right it is possible to see the annihilation of a planar defect at the cross point of two of them. As a consequence of this phenomenon, the defect density reduces with the distance from SiC/Si interface. As a rule of thumb, it has been recognised that for 3C-SiC epilayers using silicon as substrate, APBs and TBs almost disappear from the film surface when a SiC film thickness higher than $5\mu\text{m}$ is reached [30]. The progressive reduction of defect density is evident in the upper part of the STEM image (Figure 2.14 a). SAED patterns in different areas highlight once again this variation: near to SiC/Si interface (bottom inset in Figure 2.14 a) the pattern shows continuous streaks in the $\langle 111 \rangle$ directions suggesting a high density of planar defects in this direction, while the absence of these streaks in SAED carried out in an area far from the interface (top inset in Figure 2.14 a) is a clue of a lower defect density. XRD measurements involve the whole thickness of a thin film, so, even if the most superficial layers have low defect density, the XRD results are an average of the layers at different depths. For this reason, in general, a heteroepitaxial thin film quality is better near to the surface than what is assessed from XRD in the bulk.

This was precisely the reason of the choice of (100) oriented Si: APBs and TBs tend to propagate along four equivalent $\{111\}$ planes, on a perfect (100) Si substrate the elimination of these defects through mutual cancelling with increasing thickness should occur. In addition to that, on an ideal (100) Si substrate, APB shouldn't form at all, since APB are generated by odd-atom height steps at the interface. However, in real world Si substrates have a residual roughness that cannot be eliminated and this is the origin of APB in our case.

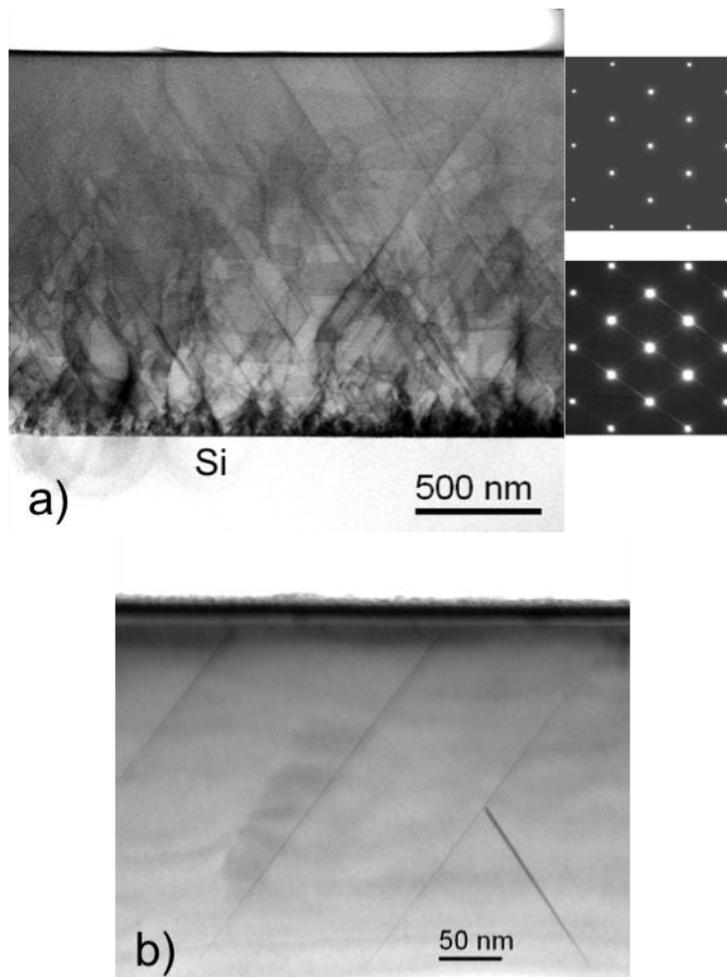


Figure 2.14: **a)** low magnification STEM-HAADF image with inverted contrast of the SiC thin film cross section. On the bottom the silicon substrate is visible and a high density of stacking defects can be inferred from the presence of streaks in the image. Moving towards the top, the defect density reduces. SAED patterns of two different zones are reported on the right, taken from the top and the bottom part of the layer. The continuous streaks in the $\langle 111 \rangle$ directions in the bottom SAED suggest the presence of a high density of stacking faults on those planes in the bottom part of the layer. The absence of such streaks in the top part SAED suggests a much reduced density of stacking defects as the layer thickness increases. **b)** High magnification image taken in two-beams diffraction contrast mode with diffraction vector $g=\langle 004 \rangle$ of the film top part. On the right it is possible to observe the point where one stacking defect annihilates into another.

The formation of APB can be totally avoided promoting a step flow epitaxy on slightly misoriented Si (100) substrates as it promotes domain expansion in a specific direction. However, in this way, there is a reduced probability for TBs parallel to the {111} planes to vanish by annihilating each other. In fact, it is necessary to have exactly the same density of TBs parallel to (111) and (-1-11) planes, while a misoriented substrate promotes the formation of TPs along one direction. To avoid these problems “undulant” Si substrates are sometimes used in research [180], but the difficulties in the preparation of good substrates with easy and cheap methods still limit the use of this technique.

The results of our choice to use (100) oriented Si substrates and obtain defect reduction with adequate film thicknesses could be verified using AFM: APB are easily detected on the surface by this technique. In the studied sample, a very smooth surface is revealed by AFM analysis (Figure 2.15) and anti-phase domains with area on the micrometre scale are evident, although much less than in the buffer layer, thanks to the higher thickness of the film in this case. The root mean square (RMS) surface roughness is about 2 nm, but the presence of anti-phase domain boundaries misrepresents this fact, because it isn't explanatory of a single domain roughness.

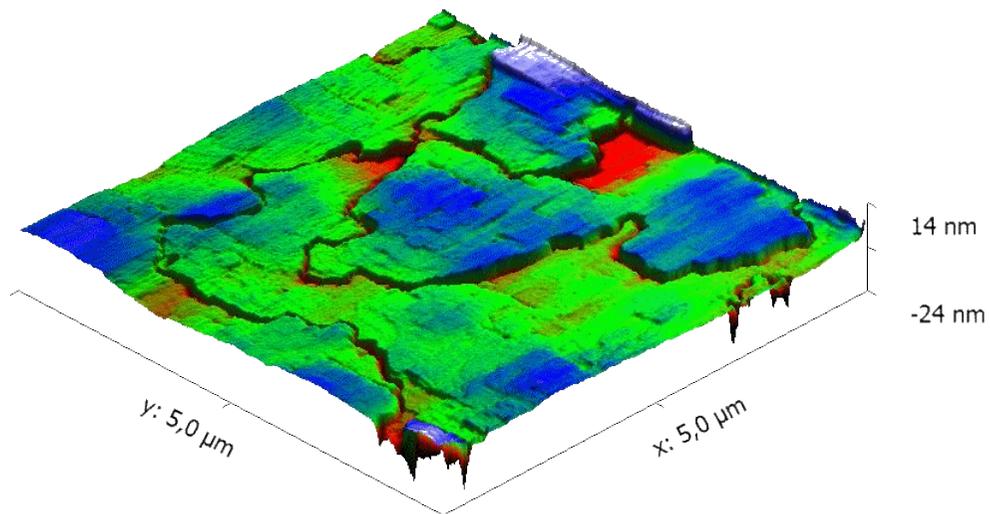


Figure 2.15: AFM analysis of the SiC thin film. Wide anti-phase domains are well visible, while inside a single domain the surface is extremely smooth. Note that z axis scale is much higher than x and y scale.

To study more accurately the surface, high resolution AFM investigations were carried out. In order to obtain a better accuracy, and to get rid of the signal generated by the anti-phase boundaries that could spoil the image, the analysis was limited inside a single anti-phase domain in a $1\mu\text{m}$ -side square (Figure 2.16). Here the RMS roughness is below 1nm and terraces are evident on the entire surface. It is evident a development from the situation observed by AFM at the end of the buffer layer (Figure 2.6) the small islands previously observed evolved in large plateaux. As already observed in many heteroepitaxial systems such as GaN on sapphire or AlN on sapphire, etc. [181], islands formed in the low temperature buffer layer have different orientations and they grow at different rates. The fast-growing islands coalesce to form larger domains and the resulting surface roughness is lower.

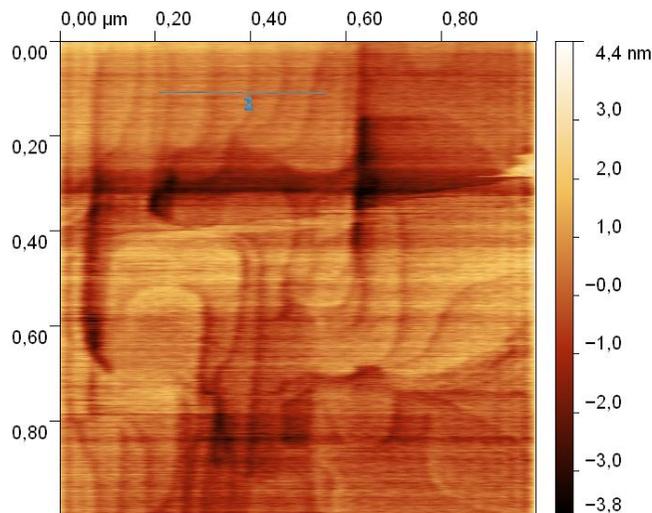


Figure 2.16: high resolution image acquired using AFM inside a single anti-phase domain in a $1\times 1\mu\text{m}$ square.

The single steps between the terraces are evident from a one-dimensional AFM scan, as presented in Figure 2.17: the surface is formed by a series of ladders with a height of approximately 0,5 nm. Knowing that the 3C-SiC lattice constant is 0,43596 nm [8] and keeping into account the error correlated to this kind of measurements, one can say that each terrace is formed by a single SiC bilayer and this suggests a highly uniform and ordered step-flow growth.

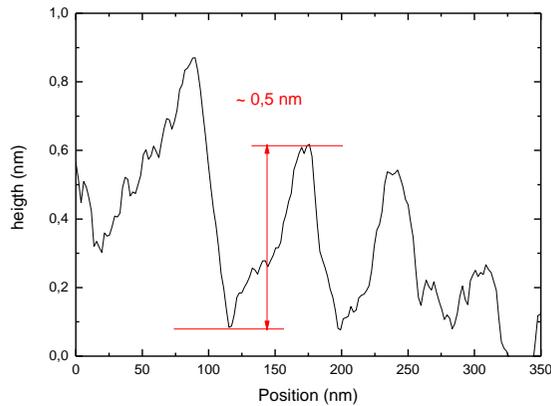


Figure 2.17: one dimensional AFM profile along the line highlighted in Figure 2.16.

A meaningful indication on the strain of an epitaxial layer can be obtained using Raman spectroscopy.

Raman on silicon carbide is particularly effective, since the large bandgap energy avoids luminescence emission at wavelength similar to that of the laser. In addition to that, SiC has a good Raman efficiency thanks to his strong covalent bonds and the signal is easily obtained. No particular sample preparation is needed and the data gathered from the Raman spectrum such as peak intensities, positions, width, and polarization give abundant information on crystal quality, strain and sometimes also carrier density.

Owing to the relatively small thickness of the SiC film, a contribution of silicon substrate to the Raman signal was expected. In order to take into account this, the Raman signal measured on a silicon wafer was acquired (Figure 2.18) in order to subtract it to the measurement. Figure 2.19 shows the spectrum acquired “as it was” and after removal of the background (fit of the silicon spectrum). Two peaks are evident, corresponding to TO mode at 795.3 cm^{-1} with $\text{FWHM} = 6 \text{ cm}^{-1}$ and LO at 970.8 cm^{-1} with $\text{FWHM} = 4.4 \text{ cm}^{-1}$.

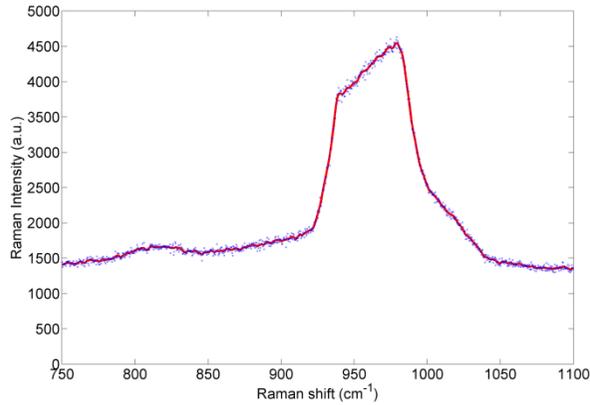


Figure 2.18: Raman spectrum of the silicon substrate. A spline interpolation is drawn in red.

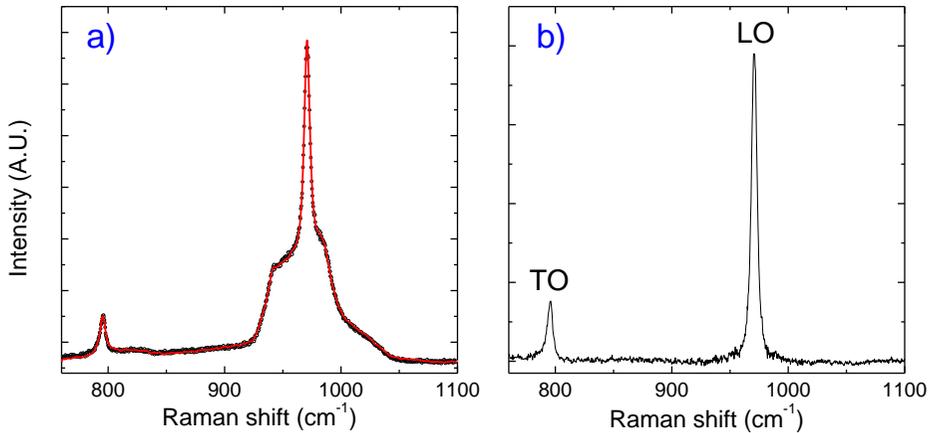


Figure 2.19: **a)** Raman spectrum of the 3C-SiC thin film. **b)** Silicon carbide film spectrum isolated after removing silicon substrate contribution. The transverse optical and longitudinal optical modes are highlighted.

As said, the shift of the Raman peaks is very sensitive to the crystal strain. In 3C-SiC, in particular, a linear relation is present between lattice mismatch $\Delta a/a$ and TO and LO peak shift[182]:

$$\omega_{\text{TO}} = 796.5 - (3734 \pm 30) \Delta a/a$$

$$\omega_{\text{LO}} = 973 - (4532 \pm 30) \Delta a/a$$

2.2

Comparing the positions of LO and TO peaks in the film and comparing them to the bulk, it is possible to estimate a residual strain of about 0,03%, a very low value for a film thickness of about 1,5 μm [179]. The low FWHM of the two peaks is an additional indication of the good crystalline quality of the film.

The absence of a rotating sample holder in the reactor causes a film thickness gradient from inlet to outlet [183] and, to demonstrate the thickness influence on the defect density, this fact was exploited for another kind of measurement. XRD was performed in different positions of the same sample (Figure 2.20):

- Inlet – higher film thickness
- Centre
- Outlet – lower film thickness

We concentrated on the (002) peak of 3C-SiC because is the most intense for a monocrystalline film. The result is shown in Figure 2.20: the thickness has an influence on the diffracted beam intensity as expected, but there is also a variation in the FWHM, if the data is normalized basing on the (002) peak height (Table 2.2). In particular, the FWHM is lower towards the inlet, where the film is thicker, indicating a better crystal quality. It is worth reminding that this kind of measurement is an average on all the film thickness, so it is always influenced by the area near the SiC/Si interface, where the defect density is higher.

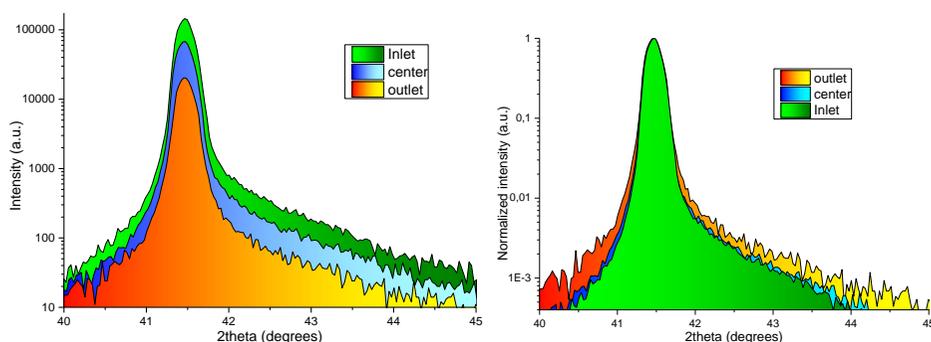


Figure 2.20: (left) X-ray diffraction measurement centred around (002) peak of 3C-SiC performed in different parts of the same sample. (right) Same measurement normalized by the (002) peak height.

Table 2.2: comparison between a Gaussian fit of the (002) peak of the XRD diffraction presented in **Figure 2.20**.

Position	Peak intensity	FWHM (arcsec) (normalized peak)
Inlet	144460	807,372
Centre	68206	814,356
Outlet	20376	819,468

2.3.2 Use of Methyltrichlorosilane

The use of single-source precursors (SSPs), such as monomethylsilane (CH_3SiH_3), methyltrichlorosilane (CH_3SiCl_3), tetramethylsilane ($(\text{SiCH}_3)_4$), and hexamethyldisilane ($\text{Si}_2(\text{CH}_3)_6$) have been extensively studied for the deposition of 3C-SiC thin films [28]. In all the alkyl compounds listed above a silicon-carbon bond is contained, therefore they are considered more efficient than using silicon precursor + carbon precursor. In most of the cases there are less safety issues to handle these compounds than silane, so this was the first reason that pushed this research line. To discuss about the crystalline quality, it is difficult to compare the results in literature, since the films are obtained under different growth conditions (carbonization, buffer layer, growth temperature) and different characterization techniques are used (AFM, XRD, TEM, RHEED, Low temperature photoluminescence (LTPL), XPS). Where the results are compared [28], [184], no significant improvement of the material quality is observed using SSP. In addition to that, the mobility on the substrate surface of a Si-C pair is lower than the single C or Si adatoms, so the use of an SSP doesn't help in reducing the growth temperature. Using an SSP one might think that the carbon to silicon ratio is always unitary, but it has been demonstrated [184] that secondary reactions induced by hydrogen reacting with carbon deplete the carbon content of the gaseous phase, so best results are obtained adding a carbon precursor to compensate that.

The real advantage of using SSP, in addition to higher safety, is the higher growth rates obtained at high temperatures ($>1300^\circ\text{C}$). Decomposition species produced by these precursors are more stable so, although higher

temperatures needed for the cracking mean higher synthesis temperatures, there is less probability of parasitic homogeneous reaction to happen. In other words, the stability of the decomposition species means that they are less reactive in the gas phase [28]. A common problem in SiC epitaxy is homogeneous gas-phase nucleation leading to the tendency of Si to precipitate as clusters from the vapour. The use of SSP, thanks to their lower reactivity in gas phase, hinders this phenomenon. Another way to struggle against this problem is the use of halogenous precursors that help in dissociating silicon gas-phase clusters and partially balance silicon and carbon contributions to the surface reaction [185], [186].

In the case of methyltrichlorosilane (MTS), three chlorine atoms are linked to a single carbon atom (Figure 2.21), so the use of MTS as precursor brings both the advantages of SSP and halogenous precursors, allowing to increase the growth rate without degrading the film properties.

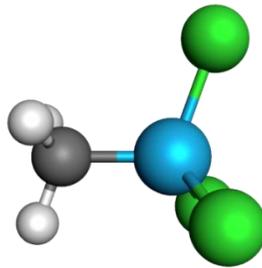


Figure 2.21: Structure of methyltrichlorosilane (CH_3SiCl_3)

As mentioned in the previous section, the achievement of high thicknesses can be advantageous not only for the realization of devices such as Schottky barriers or sensor probes, but also to obtain a higher crystalline quality exploiting the defect density reduction. Together with many advantages, the achievement of thick heteroepitaxial layers brings problems associated with wafer warp or bow, caused mainly by the large lattice mismatch and the difference of thermal expansion coefficient between 3C-SiC film and Si substrate. For this reason, the development of a process to grow thick 3C-SiC film on Si substrate with high throughput, high quality and low bow is highly desirable.

The fixed carbon-to-silicon ratio of the SSP has to be balanced, so we decided not to use MTS alone, but to add it to our standard growth process with silane and propane. MTS was stored in a standard stainless steel bubbler for metal organics liquids kept at 1200 mbar and 10 °C in a thermostatic bath. A controlled amount of MTS was delivered to the growth chamber by the use of a standard double dilution metalorganic line. SiH₄ flow was fixed at 3 sccm and the Si/H₂ ratio was 7.5×10^{-4} for all the experiments reported in this section.

Owing to the reduced reactivity of SSPs at low temperature, we decided to keep the carbonization and buffer layer procedures only with propane and silane, as described previously, and to add MTS only after reaching the growth temperature, after the end of the buffer layer.

MTS flow effect

Different MTS flows were tried and the effect of MTS concentration on growth rate was verified. The MTS addition was tested starting from the growth process described above, carried out at 1380°C and using silane and propane as precursors. The relationship between MTS supply and growth rate, reported in Figure 2.22, shows a nonlinear dependence. Even a small addition of MTS to the gas phase ($F(\text{MTS})/F(\text{SiH}_4)=1/20$) can significantly increase the growth rate (50% more), while the same doesn't occur for higher MTS concentrations. This is a further demonstration that MTS helps the silicon and carbon incorporation into the silicon carbide film. More than the actual supply of silicon and carbon from MTS, the growth rate is increased by the more efficient silane and propane precursors deposition, without the formation of Si droplets or aggregates. The deposition mechanism changes from being in surface limited or reaction limited regimes with low MTS concentrations to be transport limited [187] with high MTS concentrations.

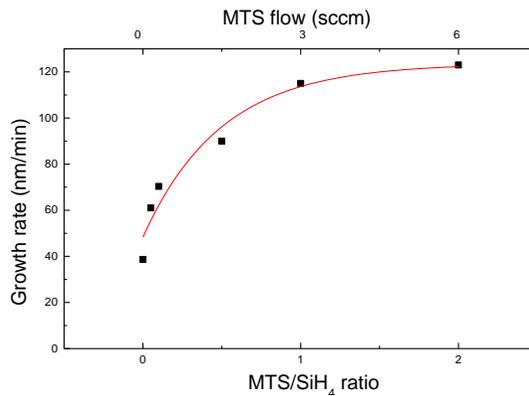


Figure 2.22: Growth rate obtained in samples synthesized with different MTS flows *ceteris paribus*.

To compare the crystalline quality, XRD was employed on three different samples, but, as said before, sample thickness plays an important role in defect reduction. In order to decouple the effect of thickness, we chose different positions in the samples so that the film thickness was always the same even with different growth rates. The presence of (002) SiC peak (Figure 2.23) testifies the good crystalline quality of the obtained films. This peak was selected to make the comparison and the FWHM allows to judge the crystalline quality and estimate the defect density. A small MTS addition seems to improve the crystal quality, decreasing the peak's FWHM, while for the sample with high MTS flow the FWHM increases (see Figure 2.23 and Table 2.3).

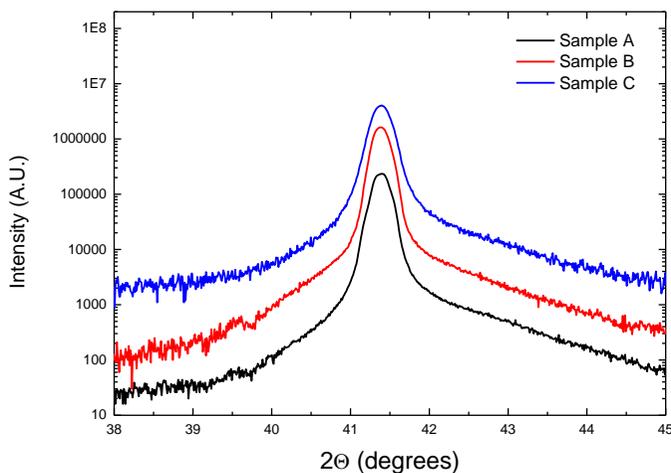


Figure 2.23: XRD of samples obtained with different MTS flows. Sample B and C curves were shifted of 10x and 100x respectively for clarity. See **Table 2.3** for samples details.

Table 2.3: comparison between (002) SiC XRD peak of samples obtained using different MTS flows.

Sample	MTS flow	FWHM of (002) peak
A	0 sccm	850 arcsec
B	0.3 sccm	810 arcsec
C	6 sccm	950 arcsec

To better understand the effect of MTS on the crystalline structure, cross section of two samples were studied using TEM. Figure 2.24 shows a comparison between the cross section of two samples grown with different MTS concentrations: α obtained using 0,15 sccm of MTS ($\text{MTS}/\text{Si} = 1/20$) and β synthesized with 3 sccm ($\text{MTS}/\text{Si} = 1$). On the right of Figure 2.24 SAED patterns are reported and, using them, it is possible to make a comparison. The diffraction pattern of sample α , with a low MTS concentration, has some streaks, but slightly less than the sample synthesized without MTS (see Figure 2.14a). A substantial improvement is achieved using higher MTS concentration in sample β : the SAED pattern show an

excellent epitaxial registry between SiC and Si. Still it is possible to observe stacking faults in the image, but their density is lower than in sample α .

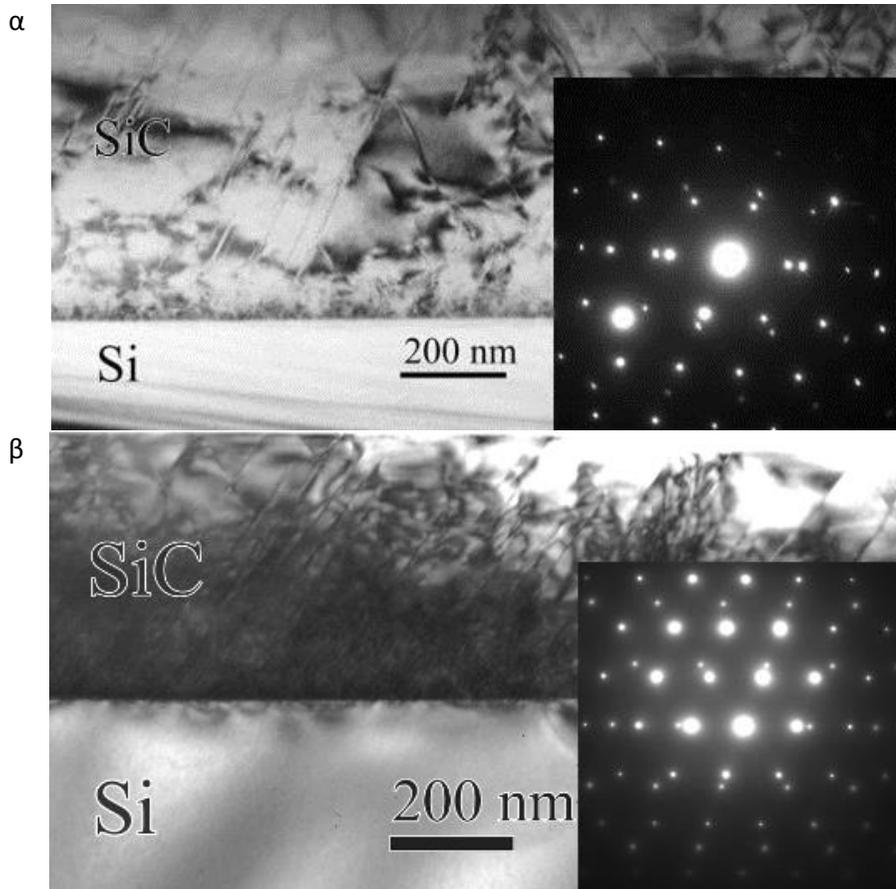


Figure 2.24: cross section TEM images of samples obtained with different MTS flow: α) obtained using 0,15 sccm of MTS and β) synthesized with 3 sccm. In the right inset SAED patterns of the SiC films are reported.

The improvement of crystalline quality adding small quantities of MTS confirms what previously assessed using XRD.

In conclusion it is possible to state that the addition of MTS up to a unitary ratio with silane reduces defect density, while reaching higher MTS flows (MTS/Si=2) causes a degradation of the crystalline quality. It has been observed [179] that increasing the growth rate by increasing precursors flows or precursors concentration, increasing reactor pressure, etc. in general results in a degradation

of the crystal quality, with broader XRD peaks FWHM, while the addition of MTS up to certain amount brings higher growth rates and higher crystalline quality.

Temperature effect

We tested different synthesis temperatures (1300 °C, 1350°C, 1380 °C, 1400 °C) with and without the addition of a fixed MTS amount (flow of 0.3 sccm Flow(MTS)/Flow(SiH₄) = 1/10). For the sake of comparison between the results, the buffer layer was always the same and a fast ramp in hydrogen only was added to reach temperatures different from the end of the BL. Growth time was 30 minutes for all samples. The schematics of the process is reported in Figure 2.25.

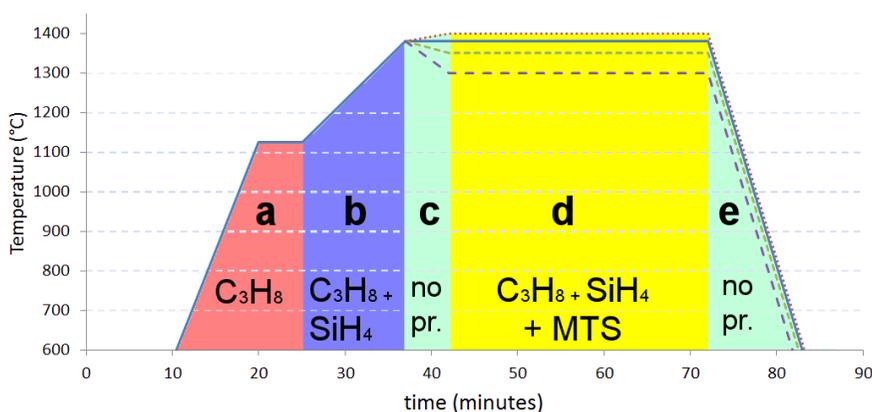


Figure 2.25: schematic drawing of the growth processes (see **Figure 2.11** for comparison). MTS was added during thin film growth (step d) while no precursors were used for the temperature ramp between buffer layer and growth (step c) and during cool down (step e).

Since there is a thickness gradient due to the non-rotating sample holder, we studied the thickness gradient more than the film thickness in a single point to speculate on the precursors depletion in addition to the growth rate. The samples thicknesses measured in different parts are reported in Figure 2.26.

The measurements confirm the fact that MTS addition causes higher growth rates both at low and high temperatures for chlorine effect as reaction catalyst, for MTS contribution to silicon and carbon supply and for all the reasons treated in the introductory part of this section. From the data shown it is possible to infer that the growth rate increases with higher temperature, as it was expected according

to literature [28]. This indicates that the kinetics limits the reaction at low temperatures: lower energy means lower probability of precursor molecules cracking and less energy available to activate surface reactions.

Different models have been proposed to explain 3C-SiC synthesis from MTS precursor. MTS is not likely to be the direct growth specie in a first-order reaction. On the contrary, some models propose that MTS pyrolytic decomposition contributes to the growth with the possible formation of more than 50 species. Some of them play important roles in the reactions: they participate directly to silicon carbide formation and/or act as catalysts. Each one has different activation energy and consequently, there are different equilibrium concentration distributions for different temperatures. Increasing the temperature promotes the decomposition of more species and higher growth rates are expected. For a more comprehensive dissertation on the thermodynamics of the gas-phase reactions occurring to MTS in gas phase see Ge et al. [188].

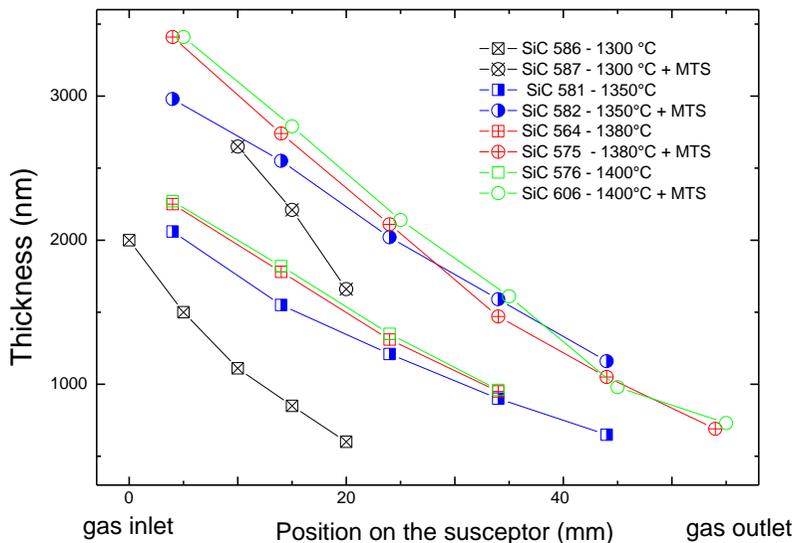


Figure 2.26: SiC film thickness of samples grown at different temperatures measured in different positions in the growth chamber.

MTS influence on defect density reduction

As previously demonstrated, MTS promotes higher growth rates and, up to certain quantities increases the crystalline quality. It is necessary to remember that, in general, to obtain a thicker SiC film means to reduce defect density thanks to the mutual annihilation of many defects like APB and TB. To study the effect of these two factors combined, we performed an additional growth at 1380 °C with MTS flow = 0.6 sccm and with doubled SiH₄ flow (6 sccm) with respect to the previous experiments, lasting 3 hours in total and resulting in a 3C-SiC layer about 15 μm thick. The growth was divided in two steps in order to minimize the thickness gradient: after a 90 minutes growth carried out following the standard already described, the sample was rotated 180° and another 90 minutes growth was carried out on it. In the second growth the buffer layer was not needed. The film thickness gradient reduction was effective and the resulting thickness gradient was less than 3% over the entire sample area. In Figure 2.27 the result of XRD carried out on the samples obtained with different growth temperatures is summarized and compared with the “thick” film sample. The FWHM reduction with the film thickness is once again evident from this graph and indicates the improvement in the crystal lattice quality as the thickness increase.

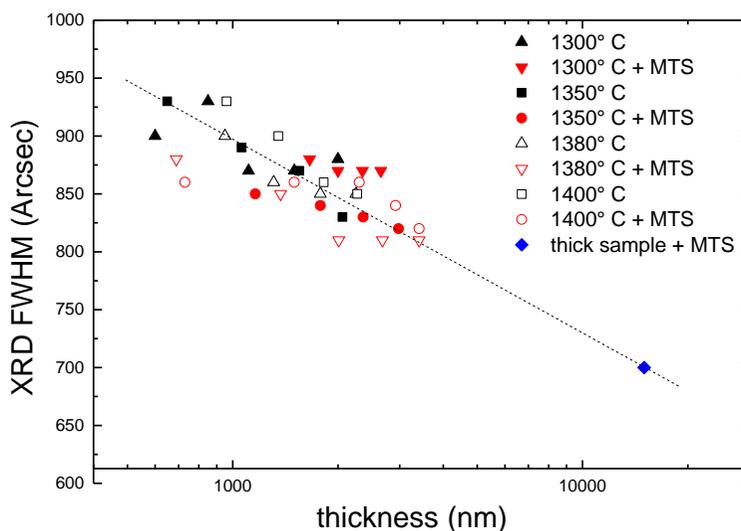


Figure 2.27: FWHM of (002) 3C-SiC peak obtained measuring XRD in different areas of the samples. Given the instrumental resolution, error bar of +/- 15 arcsec should be considered. The line was added as a guide to the eye.

A cross section of the “thick sample” was prepared and in Figure 2.28 a STEM-ADF image is reported. The bright contrast of the defects is obtained thanks to the medium collection angle of the ADF image. Once again the defect density reduction with increasing film thickness is evident and can be calculated to be about $13\%/μ\text{m}$, suggesting the almost complete disappearing of this kind of defects upon reaching thicknesses greater than about $7.5 μ\text{m}$.



Figure 2.28: STEM-ADF image of a cross section of the “thick” sample. The image was obtained as composition of two.

The use of MTS and its effect on nitrogen doped cubic silicon carbide is discussed in the next section.

2.3.3 Nitrogen doping

In order to tune the electrical properties of the epitaxial silicon carbide films it is fundamental to control the doping level. Not many dopant species have been studied for 3C-SiC, for a comprehensive exposition see section 1.5. One of the most used and straightforward method to obtain n-doped 3C-SiC is the addition of gaseous nitrogen to the reaction chamber during CVD. To obtain this, a gaseous nitrogen line was installed into the reactor during the present work. In Figure 2.29 a scheme and a photo of the line is reported: it is necessary to finely control the gas flow and be able to rapidly start or stop the dopant introduction in the chamber. A mass flow controller was installed and connected with the reactor software and two switching valves were connected to the line in order to divert nitrogen toward the reaction chamber or bypass the hot zone directly to the exhaust treatment.

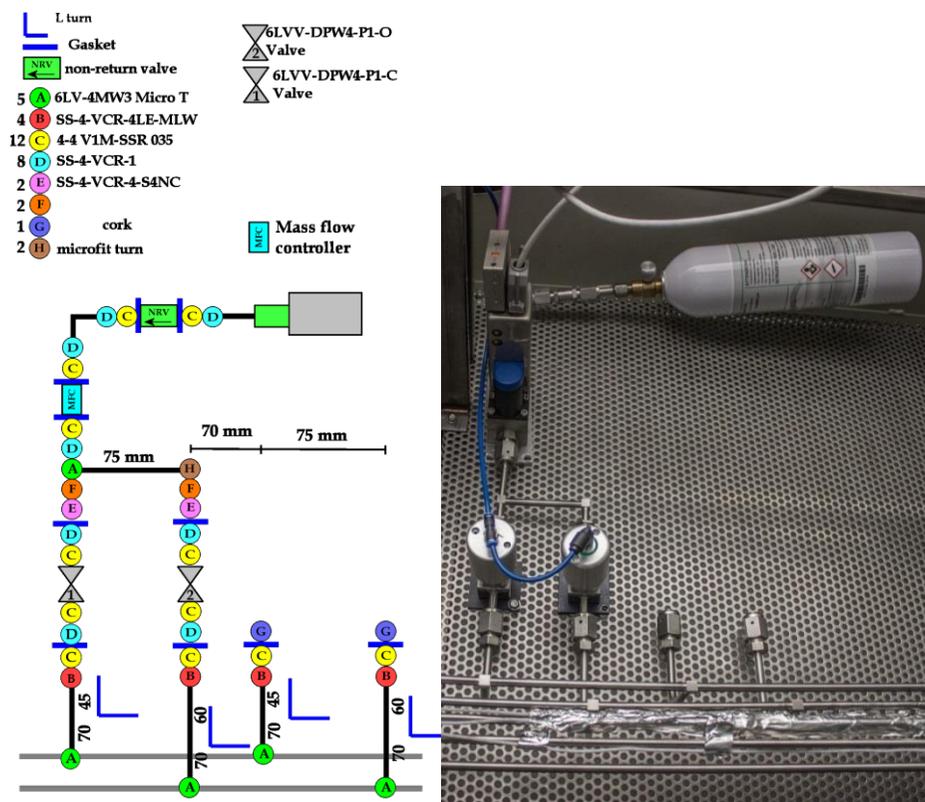


Figure 2.29: Left: connections scheme of the nitrogen doping line. Right: photo of the line with a 1 litre nitrogen cylinder connected.

The nitrogen is non-toxic and the small quantity contained in the 1 litre – 12 bar cylinder allowed us to avoid the installation of safety devices against gas leakage. In all the experiments N_2 was introduced at the end of the buffer layer, along with the thin film growth. As explained in section 1.5, there are several tools to vary the nitrogen incorporation in the film during the growth: nitrogen partial pressure, reactor pressure, C/Si ratio, growth rate and temperature. We decide to vary the nitrogen flow leaving unmodified all the other growth parameters in order to have a reliable model to design films with the desired doping level.

While some techniques like SIMS allow to investigate the quantity of incorporated nitrogen, several methods allow to measure the electrically active nitrogen and the consequent doping level. Hall effect and C/V measurements are very precise and they can be reliable, but they require ohmic contacts and the former requires also good Schottky contacts. Low temperature photoluminescence can be the best solution but it requires a dedicated apparatus and a good cryostat in order to obtain reliable measurements. In the case of 3C-SiC nitrogen doping there is a non-destructive and straightforward technique that can be used: Raman scattering.

In III-V semiconductors with high carrier mobilities, Raman scattering from longitudinal optical (LO) phonon-plasmon coupled modes has been widely studied. It is possible to estimate quite accurately carrier concentration and mobility from frequency and band shapes of the coupled mode. 3C-SiC has, however, large collision damping and the upper branch of phonon-plasmon coupled modes presents a small shift and broadening of the bands as the carrier concentration is increased. Yet, high crystalline quality 3C-SiC substrates show sharp Raman peaks and the relatively small peak shift can be measured. See [189] for a detailed study.

The correlation between the 3C-SiC LO phonon frequency at room temperature and carrier density was obtained from literature [190] and reported in Figure 2.30. The peak shift is higher for higher carrier density, but the relation isn't linear, therefore a higher accuracy of this measurement can be obtained with high doping levels ($>10^{17} \text{cm}^{-3}$). Only the LO peak at $970,8 \text{ cm}^{-1}$ represent a phonon-plasmon coupled mode, while the other intense peak at $795,3 \text{ cm}^{-1}$ corresponds to a transverse optical (TO) phonon mode which has no plasmon coupling, therefore no changes in frequency and FWHM were observed. The TO peak at

$795,3 \text{ cm}^{-1}$ was used as a reference to check measurements calibration and to compare our remarks with literature data. Being (100) silicon the preferred substrate in this work, also the silicon Raman peak located at 520 cm^{-1} can be used as additional reference to calibrate the instrument, since it is quite intense and sharp.

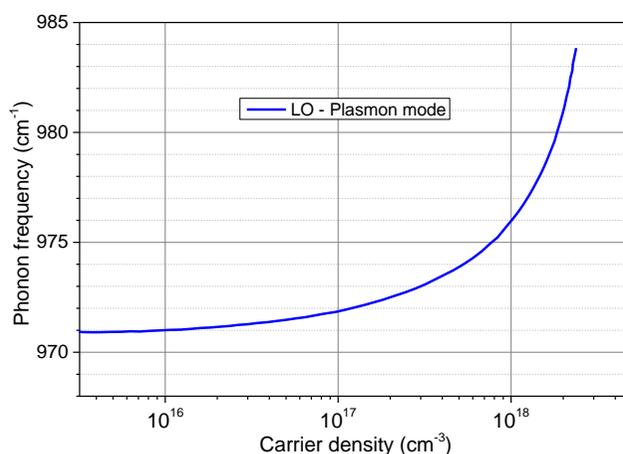


Figure 2.30: peak position of the LO-plasmon mode in 3C-SiC Raman scattering plotted as a function of the carrier concentration (Adapted from [190]).

For the Raman spectrum of undoped “standard” 3C-SiC thin film please refer to Figure 2.19. We synthesized different samples with increasing dopant precursor flow to investigate its incorporation rate in the film. A linear relation is expected between gaseous dopant supply and doping level [46]. In Figure 2.31a a comparison between samples obtained with different dopant precursor flow is reported. Raising the dopant flow in the reactor, the LO peak shift increases and its shape broadens. The comparison between the TO peak of the same samples is presented in Figure 2.31b: no shift caused by the different doping level can be measured, as expected. We studied the nitrogen incorporation in two series of samples, obtained with or without the addition of methyltrichlorosilane (MTS) following the procedure already presented (section 2.3.2). The comparison between Raman spectra of nitrogen doped samples obtained using MTS is presented in Figure 2.32. The same trend already described for the samples without MTS is still valid: increasing the dopant precursor flow results in peaks shifting and broadening.

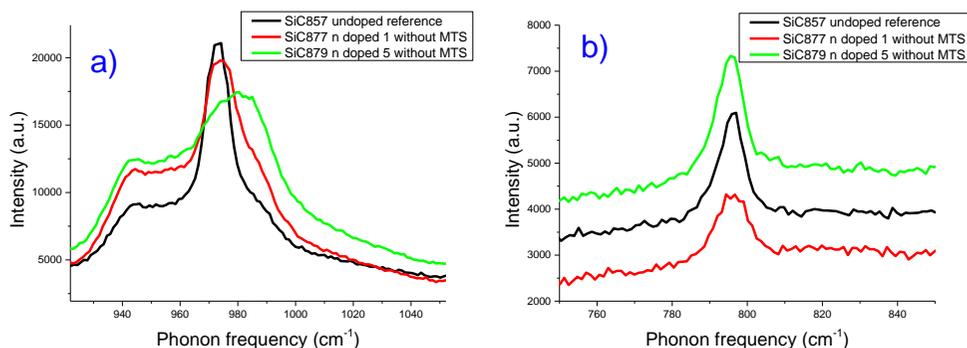


Figure 2.31: a) comparison between Raman scattering measurements around 3C-SiC LO phonon mode ($970,8 \text{ cm}^{-1}$). Samples obtained with different nitrogen flows are presented (the number reported in the legend is nitrogen flow in sccm). b) Comparison between Raman spectra of the same samples centred around 3C-SiC TO phonon mode (the spectra intensity is shifted for a better reading). No frequency shift between the TO peaks is measurable.

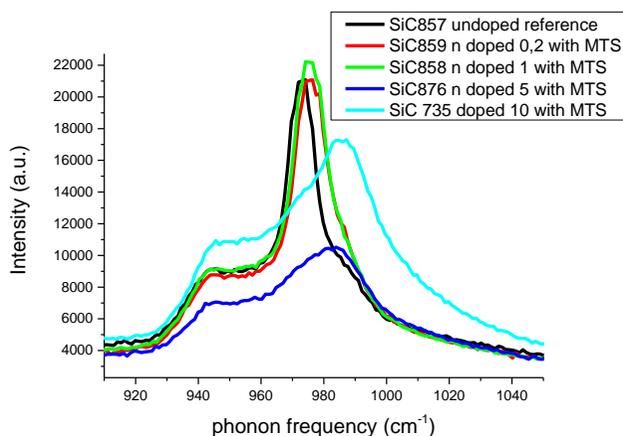


Figure 2.32: comparison between Raman spectra centred around 3C-SiC LO phonon mode ($970,8 \text{ cm}^{-1}$) of films grown with different nitrogen flows. 3C-SiC films were obtained using MTS according to the procedure described in the previous section.

We fit the LO peaks of the Raman spectra and we found the exact peak position for each sample. When we plotted the LO mode Raman shift vs. nitrogen flow (Figure 2.33) we found that there was a constant discrepancy between the doping level obtained in samples synthesized using MTS and those without MTS. Was MTS acting like a dopant? We checked the LO peak position in the reference

sample obtained using MTS but without the nitrogen addition (Figure 2.31a) and we compared it to the “reference” spectrum without MTS and without nitrogen (Figure 2.19). The peak position was unchanged. MTS alone cannot dope silicon carbide. Only when adding nitrogen from gas phase the doping level changed with or without MTS.

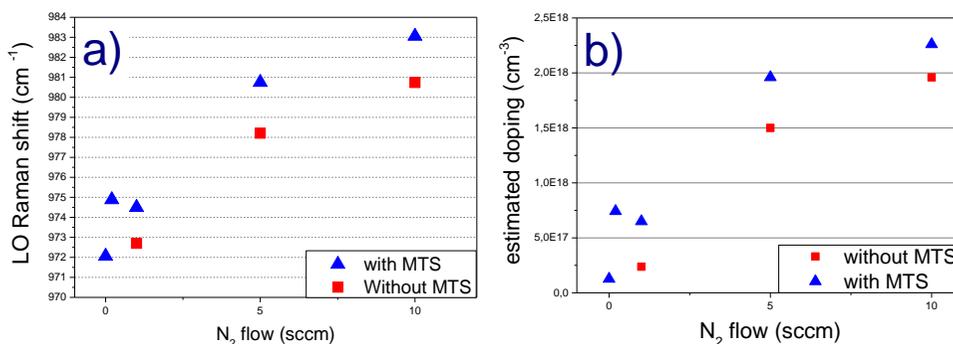


Figure 2.33: a) LO mode Raman peak position as function of the nitrogen flow in n doped 3C-SiC thin films. Blue triangles and red squares are samples obtained respectively with and without the addition of MTS. b) Doping level extracted from the same data according to the relations presented in [190] (**Figure 2.30**).

It has been demonstrated [46] that increasing the growth rate by raising the precursors flows results in a lower doping level. On the contrary, in our case with the addition of a small quantity of MTS we reached a higher growth rate and a higher doping level. As previously discussed, nitrogen enters in the silicon carbide lattice as a substitutional specie for carbon. As a well-known consequence, the variation of carbon to silicon ratio C/Si has a direct effect on nitrogen incorporation in SiC [46], in particular, increasing the C/Si results in lowering the dopant incorporation. We thought that the introduction of MTS could change the C/Si. The “standard” process has a C/Si equal to 0,7, now we are adding MTS, which has a C/Si equal to 1, so the addition of MTS increases the C/Si. According to the site competition principle, the addition of MTS should have decreased the doping level, while we observed the opposite phenomenon.

We thought that MTS could affect nitrogen incorporation in two possible ways. The first hypothesis was that chlorine helps the dissociation of nitrogen molecules forming nitrogen chloride (NCl₃) or intermediate compounds whose reactivity is higher than nitrogen molecule. In the second scenario, since the presence of

chlorine helps the dissociation of silicon clusters in gas phase, silicon-terminated sites are more copious and available for carbon or nitrogen adatoms binding.

To verify that the nitrogen incorporation into SiC thin films didn't worsen the crystalline quality, XRD was carried out on samples with different doping level Figure 2.34. We couldn't measure a variation in the X-Ray pattern and the (002) 3C-SiC peak FWHM didn't change sensibly with the doping level.

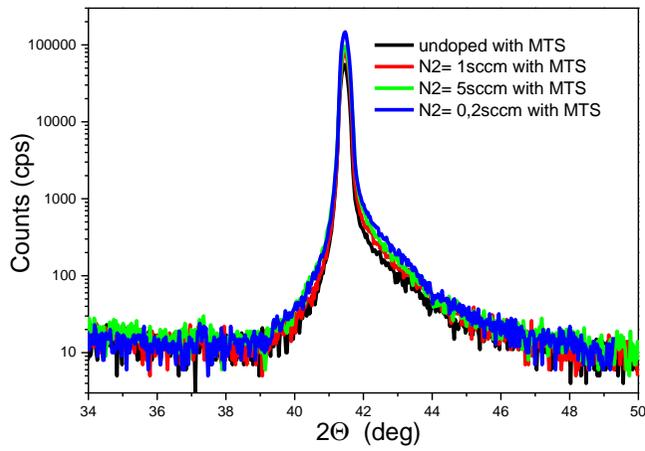


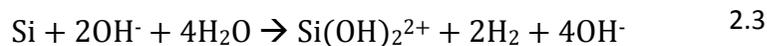
Figure 2.34: X-ray diffraction patterns of samples with different dopant concentrations. The pattern is centred on (002) SiC peak.

2.4 Micromachined structures

As previously mentioned, using silicon wafers as substrates for the synthesis of silicon carbide brings many economical and physical advantages. One of them is the possibility to obtain silicon carbide suspended structures by means of silicon micromachining techniques. Dry etching techniques such as reactive ion etching (RIE) and deep reactive ion etching (DRIE) are currently employed especially to obtain high aspect ratio structures thanks to their high anisotropy, but chemical etching still is diffused for many processes due to its higher etching rate, better surface smoothness, high anisotropy, low cost, simple etch setup. Among the well-known chemical micromachining techniques to process silicon substrates, three wet etching were tried to obtain silicon carbide suspended membranes. The final aim was to evaluate optical and mechanical properties of the material.

2.4.1 Potassium hydroxide

The mechanism of hydroxide-based silicon etching is founded on the transport of an electron from an OH⁻ group to surface silicon [191]. This brings to the silicon atom coordination with hydroxyl groups. Silicon is oxidized, water is reduced and the redox reaction is:



The silicate species further react with hydroxyl to form water soluble complexes:



The number of chemical bonds present on the crystallographic plane influences the reaction kinetics [192]. In addition to that, temperature and solution concentration sensibly influence the etching rate on the different crystal orientations. Potassium hydroxide (KOH) is one of the most commonly used silicon etchants, because of its high etching rate and low cost. As for other hydroxide-based etching reactions, the etching is anisotropic and influenced by temperature and concentration. Table 2.4 after Hull [25] was used as reference for the experiments. A KOH:H₂O 3:7 solution was used for the experiments

because this concentration ensures smoother surfaces according to literature [193]. The chosen etching temperature was 80° because it allows a fast etching rate, while the water evaporation rate from the solution is still low enough to avoid using a condensation column. A continuous stirring was provided in order to avoid high concentration gradients inside the reaction vessel. Glass is slowly attacked by KOH, so a polytetrafluoroethylene vessel was used because it is inert to KOH.

Table 2.4: Silicon orientation dependent etch rates of KOH tested for different compositions and temperatures. Adapted from Hull [25].

Etchant	T (°C)	Direction (plane)	Etch rate (μm/ min)	Remarks
20% KOH: 80% H2O	20	(100)	0.025	Near Peak etch rate at the conc. across temperature
	40	(100)	0.188	
	60	(100)	0.45	
	80	(100)	1.4	
	100	(100)	4.1	
30% KOH: 70% H2O	20	(100)	0.024	Smoother surfaces than at lower concentrations [193]. Faster etch rate for (110) than for (100)
	40	(100)	0.108	
	60	(100)	0.41	
	80	(100)	1.3	
	100	(100)	3.8	
	20	(110)	0.035	
	40	(110)	0.16	
	60	(110)	0.62	
	80	(110)	2.0	
	100	(110)	5.8	
40% KOH: 60% H2O	20	(100)	0.020	
	40	(100)	0.088	
	60	(100)	0.33	
	80	(100)	1.1	
	100	(100)	3.1	
20% KOH: 80% 4 H2O: 1 IPA)	20	(100)	0.015	Lower etch rate, Smoother, Less undercutting, Lower (100) : (111) etch-rate ratio
	40	(100)	0.071	
	60	(100)	0.28	
	80	(100)	0.96	
	100	(100)	2.9	
44% KOH: 56% H2O	120	(100)	5.8	
		(110)	11.7	
		(111)	0.02	
23.4% KOH: 63.3% H2O: 13.3% IPA	80	(100)	1.0	Sensitive to boron concentration
		(110)	0.06	

One of the main KOH drawbacks is the relatively poor selectivity to SiO_2 (etching rate $\text{Si}:\text{SiO}_2 \approx 1:100$), in addition to that, most of the photoresists cannot withstand the high pH environment. Silicon nitride (Si_3N_4) allows to obtain higher selectivity ($\text{Si}:\text{Si}_3\text{N}_4 < 1:1000$) and it is often used as a mask [194]. Being silicon carbide a material with high chemical inertness owing to his strong covalent bonds (see section 1.1) we thought of using it as an etching mask. A $15\ \mu\text{m}$ thick 3C-SiC film was grown on silicon (100) substrate with the process described in the previous section. This was used as substrate and another SiC film was grown on the other side on bare silicon. A graphite mask was placed prior to the growth, thus protecting a selected area from the SiC deposition. The result was a film deposition obtained on the whole surface except in the area covered by the graphite. When exposed to KOH etching only bare silicon was attacked. The etching was performed in a 30% KOH in water solution at 80°C for 8 hours. The etching was slower than expected, probably because the presence of boron doping in the wafer sensibly slows down the etching rate on all the crystalline planes [195]. The results are shown in Figure 2.23: the SiC film couldn't endure to the stress and broke. The SiC mask worked for the first hours of etching, then the silicon beneath was attacked. Two mask shapes are shown in figure: the circular mask minimizes the stress on the edge, but still the membrane broke in the centre.

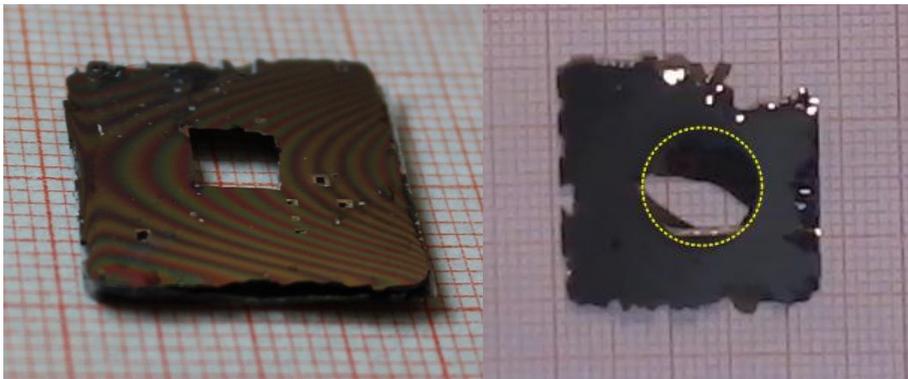
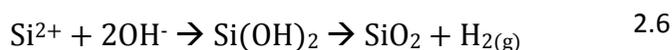
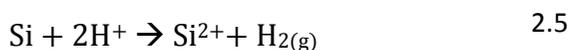


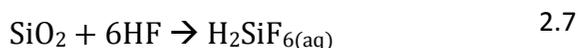
Figure 2.35: SiC film on Si substrate after 8h KOH etching: in both samples the SiC film could not withstand the stress and broke.

2.4.2 HNA solution

Hydrofluoric acid, Nitric Acid and Acetic Acid (HNA) etching mixture was also tried to fabricate the SiC membranes. The base mechanism rely on sequential silicon oxidation and dissolution processes, so the availability of H^+ ions and dissolvability of SiO_2 at the different etch fronts determine the etch rates. Schwartz and Robbins deeply examined the reactions [196], [197] and, according to their studies, the etching is initiated by H^+ ions from nitric acid, which loosen silicon covalent bond and oxide Si atoms. OH^- ions can be provided from the acid or from the solvent (water and/or acetic acid) to produce silicon oxide.



The hydrogen emission can be easily observed as bubbles are released by the sample in the liquid solution. The role of hydrofluoric acid (HF) is dissolving the silicon dioxide to produce H_2SiF_6 which is dissolved in the solution.



Acetic acid (CH_3COOH) is added to the solution to play the role of solvent and to prevent excessive dissociation of nitric acid, having CH_3COOH a lower dielectric constant than water (6,15 for CH_3COOH versus 81 for H_2O). Acetic acid is also less polar than water and this allows a better wetting of hydrophobic surfaces such as the one of silicon.

HNA etching rate is affected by several parameters such as the relative concentration of the three components (varying with time as the etching is in progression) and the temperature (but usually the etching is performed at RT). This is the reason why in this case results are not always reproducible.

As in the case of KOH, most of the photoresists cannot withstand and the selectivity of SiO_2 mask is relatively poor (etching rate $Si:SiO_2 = 1:100$), so silicon nitride masks are mostly used. We tried once again to use a silicon carbide mask, we thought that thanks to the high energy SiC covalent bonds, the material should be resistant to this kind of etching mechanism.

The etching was tried with a low concentration (8,3% HF, 25% HNO₃, 66,6% CH₃COOH) and using a circular mask, both choices in order to minimize the stress. The result is shown in Figure 2.36: the etching was almost complete and the mask could perfectly withstand the chemical attack.

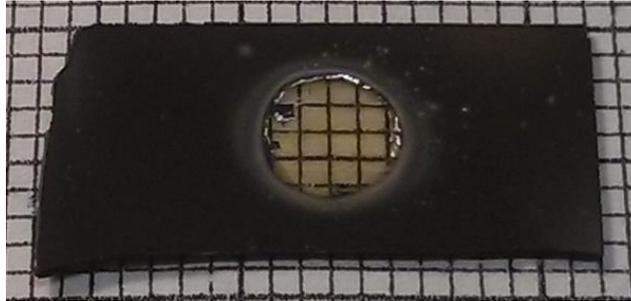


Figure 2.36: rear view of the SiC membrane obtained etching silicon substrate with HNA solution. A SiC etching mask was used.

This technique allowed the use of a mask extremely resistant to the chemically harsh environment. The mask wasn't damaged even after hours of chemical etching. The drawbacks are related to the infiltration of the etching solution underneath the mask, so long "channels" were created in the silicon before the etching was completed (see Figure 2.37). This is most probably due to the anisotropy of the etching, facilitating lateral etching. Etching rates along different crystallographic directions may vary according to the reaction parameters (reactant relative concentration), but in general the etching rate of the (110) planes is the fastest ((110) > (100) > (111)) [196], [197].

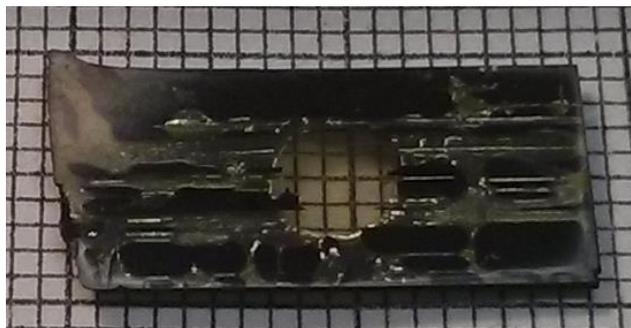


Figure 2.37: front view of the SiC membrane obtained using HNA etching: the channel created by the etching infiltration beneath the SiC layer are visible thanks to the film transparency.

2.4.3 Tetramethylammonium hydroxide

Tetramethylammonium hydroxide (TMAH) is a quaternary ammonium salt with the molecular formula $N(CH_3)_4^+OH^-$ and its low toxicity together with the absence of metallic ions contributed to its diffusion as silicon wet etchant despite its high cost. The main advantages of the TMAH-based solutions are related to their full compatibility with integrated circuits technology. Other basic solutions such as KOH or NaOH frequently cause contamination with mobile alkali metal ions (K^+ or Na^+) which drastically reduce carrier lifetimes of CMOS processes. In addition to that, TMAH presents an extremely high selectivity towards silicon oxide: the silicon etching rate is three order of magnitude higher than the one of SiO_2 [198]. For this reason a silicon oxide mask obtained with photolithography techniques is suitable even for long time etchings. On the other hand, even the thin native oxide on silicon can stop TMAH etching, so it is crucial to protect the sample from oxidation between photolithography and etching. The chemical reaction is similar to the etching obtained with other hydroxides and it is briefly explained in section 2.4.1: a redox reaction creates silicon water soluble species. As other wet chemical attacks, TMAH produces anisotropic silicon etching and the etching rate on (100) planes is from 10 to 40 times faster than on (111) planes [199]. The etching rate varies sensibly with the concentration and temperature, with the highest etching rate ($81\mu\text{m/h}$) reached for a TMAH solution concentration of 8 wt.% and an etching temperature of 90°C [198]. With higher concentrations the etching rate decreases but the surface is smoother. As a result, pyramidal hillocks are often observed on etched Si(100) surfaces and they are produced by anisotropic etching especially at low TMAH concentrations. Landsberger et al. [200] noticed that the faces of the pyramids corresponded to (111) planes and proposed an explanation to the mechanism. Hillocks are formed by anisotropic etching which is sensitive to the dissolved Si content. Higher TMAH concentrations give lower dissolved Si content and lower anisotropy. Lower TMAH concentrations result in higher dissolved Si content as the etching proceeds and (100) planes are dissolved faster than (101) planes. A long etching in low concentration TMAH may result in such a high hillock density that the etching rate may decrease suddenly and the etching may stop. To avoid this, some precautions are often used before the etching: adding silicon powder in the solution and subsequently ammonium persulfate $(NH_4)_2S_2O_8$ reduces the etching rate ratio between (111) and (100) planes [201]. Ammonium persulfate is a weak acid and

act as buffer for TMAH (base), in addition to that, $(\text{NH}_4)_2\text{S}_2\text{O}_8$ is an oxidizing agent, thus serves as radical initiator of the etching reaction.

In this work TMAH etching was used for silicon substrate micromachining with a photolithographic process to prepare a photoresist mask. Buffered oxide etch (BOE) was then used to selectively remove silicon oxide. Concentrated HF etch is too quick, a good process control is difficult and photoresist mask may be damaged or completely removed, so a mixture of ammonium fluoride (NH_4F), used as buffering agent, and hydrofluoric acid (HF) called BOE is frequently used [194]. In our case we found that the photoresist masks used couldn't withstand pure HF and they were completely removed, while a 6:1 volume ratio of 40% NH_4F in water to 49% HF in water proved to be effective in removing the oxide but preserving the photoresist.

- A 7 μm thick 3C-SiC film was synthesised on (100) silicon substrate.
- The sample was oxidized in dry air at 1000° C for 8 hours thus forming a 100nm thick SiO_2 layer on the back (silicon carbide oxidation rate is slower, thus we expect a layer of 10-20 nm on it).
- Photoresist was spread on the back of the silicon substrate, exposed to UV irradiation for 30 seconds using a custom-designed prototype mask (shown in Figure 2.38).
- After resist development, 2 minutes BOE etch was carried out on the sample, thus removing the uncovered silicon oxide layer.
- Acetone was used to remove the residual photoresist.
- TMAH etching was started immediately.

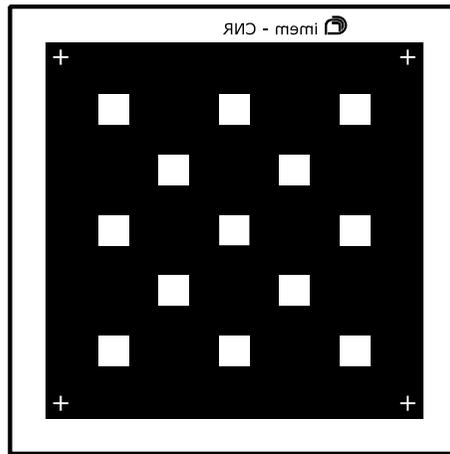


Figure 2.38: Photolithography mask used to selectively etch thermal oxide. Please note that masks design must be mirrored in order to see the final pattern.

The etching was carried out at 90°C in a 5% TMAH solution in water with 0,1% wt. ammonium persulfate and lasted 8 hours. The result is shown in Figure 2.39: silicon carbide demonstrated to be inert and the film wasn't deteriorated from the chemical etching. The outcome was the formation of square SiC membranes suspended on a silicon substrate acting as a frame.

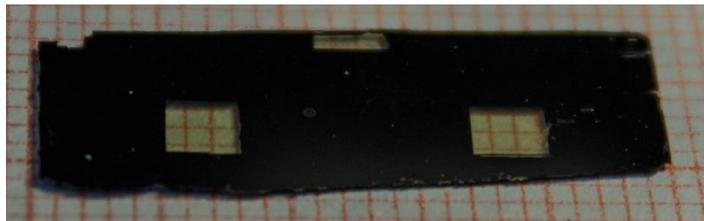


Figure 2.39: SiC membranes obtained with the etching of silicon substrate using TMAH

The main advantages of this technique, in comparison with the others illustrated before, were the sharp edge left by the etching at the membrane border (no "channels" in the silicon) and the absence of a visible strong stress bending the membrane.

2.5 Stress evaluation using Raman spectroscopy

A quantitative measurements of the stress in the film can be of great help for the development of MEMS-based devices. Instead of performing resonant frequency and bending tests on MEMS fabricated on purpose, Raman spectroscopy is a simple, non-destructive technique that can evaluate the stress in a SiC film[202].

It is well known that Raman modes are strictly correlated to the strain field distribution in 3C-SiC [182]. In this case the TO mode was measured and its variation was correlated to 3C-SiC membrane deflection. An artificial stress was applied to the membrane fabricated with the procedure previously described and the variation in the Raman spectrum was measured.

A membrane model was calculated for 1000 mbar pressure (Figure 2.4) and it showed the stress distribution to be higher near the borders than in the centre. For this reason we tried to perform Raman measurements near to the point of maximum stress.

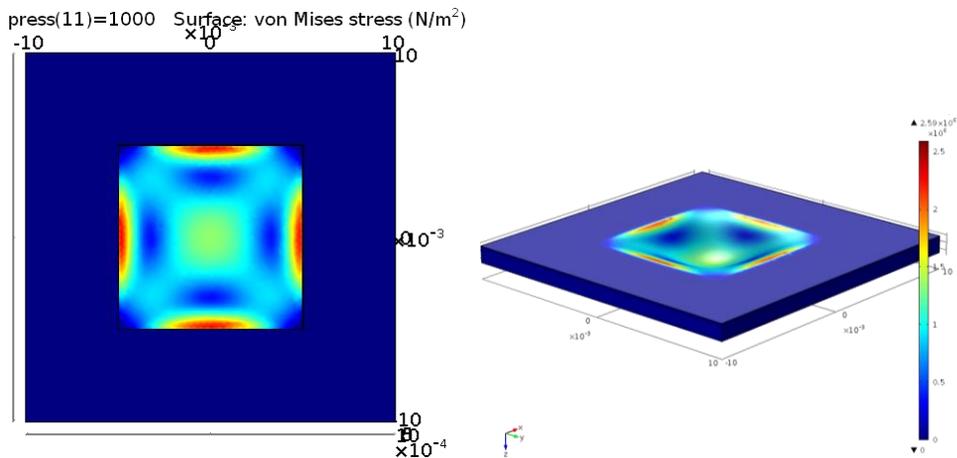


Figure 2.40: colour map of stress distribution over a simulated membrane with applied uniaxial pressure

The sample was sealed to a sample holder. A hole corresponding to the membrane position allowed us to connect the sample holder to a vacuum pump. The pressure was varied using two valves and it could go from atmospheric

pressure (1013 mbar) to 300 mbar. Silicon peak from the substrate was used as reference to calibrate each measurement.

The result is shown in Figure 2.41: there is a shift of TO peak, as expected while the trend in LO peak shift isn't clearly estimable.

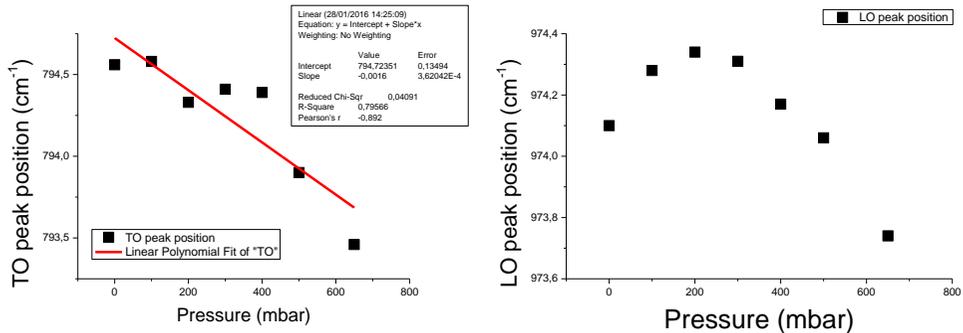


Figure 2.41: On the left: plot of the Raman TO phonon peak position as a function of the pressure applied to the membrane. On the right: LO phonon position as function of the applied pressure. Note that in the graph the differential pressure is indicated: 0 mbar correspond to absence of membrane deflection.

TO Raman is more affected from the stress field within the material. The LO Raman mode is affected by doping (see section 2.3.3) and unintentional doping can spoil the measurement. For these reasons we think that TO Raman peak measurements are suitable to be used as quantitative evaluation of stress in 3C-SiC MEMS.

Chapter 3 - SiC nanowires: processes and new developments

During this PhD work, particular efforts were devoted to the synthesis of silicon carbide and silicon oxide nanowires. For a rapid review on SiC nanowires properties and applications please see section 1.7. Chemical vapour deposition was chosen as synthesis method for its simplicity, high yield and the possibility to finely control growth parameters such as temperature, pressure, flows, precursors concentration. The nanowires were grown on silicon substrates using CO as precursor in an open-tube reactor. Different structures were obtained depending on the growth conditions: core-shell SiC/SiO₂ nanowires and carbon-doped silicon oxide nanowires. More details are provided in the following.

3.1 Substrate preparation

The procedure for the growth of silicon carbide nanowires starts with the chemical cleaning of the substrate, then the metal catalyst is deposited onto it and finally the sample is inserted into the reactor chamber where the growth takes place.

In vapour phase epitaxy of semiconductor species the substrate plays a fundamental role and the growth interface has a direct influence on the structure of the epi-layers. In addition, what produces the uniaxial elongation in a catalytic growth mechanism, is the presence of nucleation points on the surface of the substrate, so, for nanowires synthesis, the presence and the arrangement of the catalyst hold sway on the final nanostructure morphology and organization. For that reason a peculiar attention must be paid to substrate preparation and catalyst deposition.

In this section, after a brief description of the substrate preparation procedure, different catalyst deposition techniques are illustrated and the dewetting process is studied with selected examples.

3.1.1 Chemical cleaning

The preparation of the substrates prior to the deposition is critical for the result of the dewetting process. Since the catalyst has to form an alloy with the silicon of the substrate to transform to liquid phase, the presence of an interlayer between the metallic layer and the substrate may hinder the process. To avoid that, the substrate is prepared by removing impurities and clean the surface.

The first step is an ultrasonic bath in deionized water, then in acetone to dissolve organic molecules present on the surface.

Later RCA SC-1 and RCA SC-2 processes [203] are performed to further remove organic and ionic contaminants. HF etchings are done between RCA SC-1 and RCA SC-2 and at the end to remove the silicon oxide layer formed by the chemical processes and exposition to air.

3.1.2 Catalyst deposition method

Catalyst distribution stage has a pivotal role aiming to uniform and controlled growth. The essential step prior to VLS growth is to have uniform catalyst particles coverage of the substrate. In order to obtain that, it is possible to deposit a thin film and then induce the so-called “dewetting” process (see section 1.7.1 for a more detailed dissertation).

For the growth of core-shell SiC-SiO₂ nanowires and silicon oxide nanowires, the best and most straightforward method was found to be the drop casting of an ethanol solution of metal nitrates (Ni(NO₃)₂ or Fe(NO₃)₃).

Silicon wafer HF treatment is a very well-known technique to remove silicon surface oxide and to obtain a stable H-terminated surface. The result of this process is a (100) Si surface with most of Si atoms bonded with 2 hydrogen atoms each (Figure 3.1) and small percentage of them bonded with 1 or 3 hydrogen atoms or oxygen or fluorine depending on the conditions of etching treatment (HF concentration, time, temperature, pH) [204]. Water rinse after this treatment tends to remove fluorine terminations and to replace them with hydroxyl groups[205].

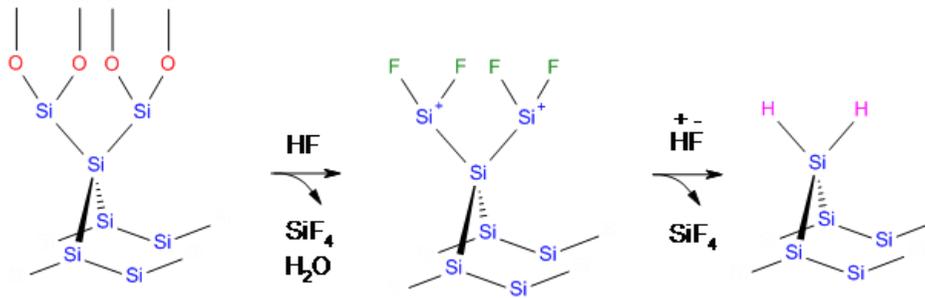


Figure 3.1: Possible mechanism explaining the formation of Si-H bond on (100) silicon surface after HF treatment (after Ubara et al. [204])

This surface has a low wettability with ethanol solution because it is non-polar, so the catalyst ethanol solution forms droplets when dispersed onto it. The formation of a uniform layer is hindered. To avoid that, it is necessary to increase the wettability, thus minimizing the contact angle of the solution on the surface.

The contact angle θ formed by a liquid droplet placed on a homogeneous smooth solid surface, can be calculated using Young relation [206]:

$$\cos \theta = \frac{\gamma_{sv} - \gamma_{sl}}{\gamma_{lv}} \quad 3.1$$

where γ_{sv} , γ_{sl} and γ_{lv} are the interfacial tensions of the solid-vapour, solid-liquid and liquid vapour phases, respectively.

One way to reduce the contact angle is then to lower the surface energy of the solid-liquid interface. Therefore we thought to enhance the hydrophobic surface wettability by adding an organic surfactant to the catalyst solution. If the hydrophobic “tail” of amphiphilic molecule is in contact with hydrophobic silicon surface, then the hydrophilic “head” is facing the polar solution and the overall result is a lower surface energy. The presence of a surfactant leads to the formation of a uniform film on silicon substrate after catalyst solution drop casting on silicon substrate [137]. A schematic view of surfactant distribution on H-terminated 100 Si surface is shown in Figure 3.2.

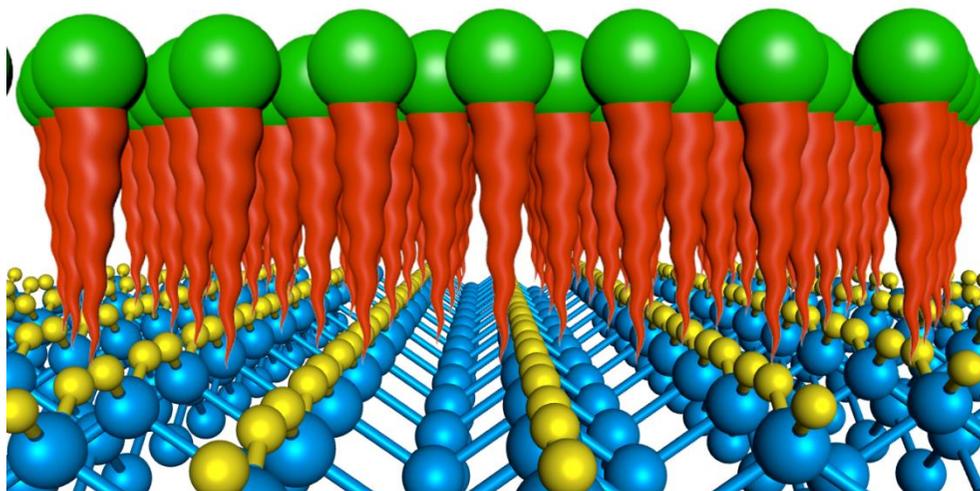


Figure 3.2: simplified view of the H-terminated silicon (100) surface and the disposition of the surfactant. Each surface silicon atom (big blue spheres at the bottom) is bonded to two hydrogen atoms (yellow smaller spheres) and this creates a hydrophobic surface. Surfactant molecules tend to dispose in ordered manner on the top: the hydrophobic tail of the molecule (orange, curvy cones in the centre) is in contact with the hydrophobic surface, while the hydrophilic head of the oleylamine molecule (green spheres on the top) is close to the ethanol-catalyst solution (not shown in the picture).

The choice of the surfactant specie is extremely important, since it remains on the surface and it can contribute to the synthesis. We needed a non-ionic surfactant that couldn't contribute with dopant elements or add oxygen to the reaction, so we chose oleylamine (OAm). OAm is a long chain primary alkylamine, it is an unsaturated fatty amine related to the fatty acid oleic acid. It is widely used for the synthesis of nanoparticles, it can act as surfactant, solvent but it can also behave as electron donor at elevated temperatures, acting as reducing agent as a function of other synthesis parameters [207]. It has low cost and It is liquid over 21°C, so this fact simplify the washing procedures. However, as indicated in the material safety data sheet, OAm can be corrosive to the skin, so precaution should be taken during handling.

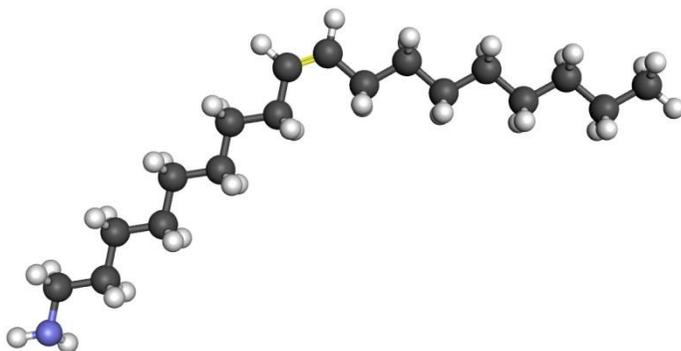


Figure 3.3: oleylamine chemical structure ($\text{CH}_3(\text{CH}_2)_7\text{CH}=\text{CH}(\text{CH}_2)_8\text{NH}_2$). It is a long-chain primary alkylamine with a double bond (in yellow in the figure) at its centre. Carbon, hydrogen and nitrogen atoms are depicted as black, grey, blue spheres, respectively.

The drying process is performed at 40°C for less than 20 minutes to limit the formation of silicon oxide on the surface; as a result, a uniform layer of nitrate is obtained. Thanks to the presence of the surfactant, even during the drying process, when ethanol evaporates and the catalyst concentration increases, the wetting of the substrate remains complete until a film of dry nitrate is formed on the silicon.

The uniformity of the nanowires bundle covering the whole substrate after the CVD synthesis is visible with bare eye (Figure 3.4).

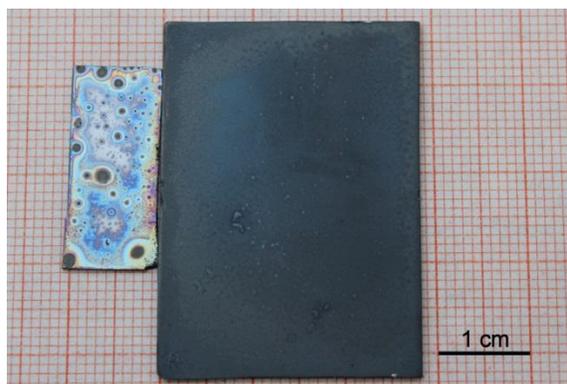
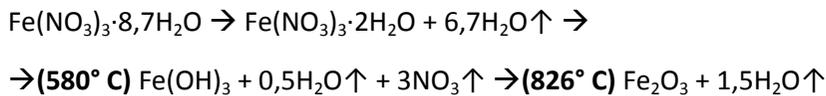
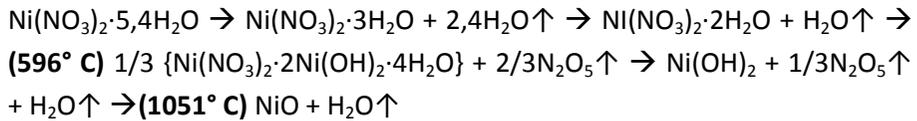


Figure 3.4: Silicon substrates covered by core/shell SiC/SiO₂ nanowires (white areas). On the left: sample obtained without using surfactant. On the right: catalyst deposition carried out using a surfactant in the catalyst solution.

3.1.3 Dewetting procedure for nitrates

Both ferrous nitrate and nickel nitrate undergo a dehydration and a thermal decomposition and the result is the formation of the corresponding oxide:



(after Elmasry et al. [208])

Gaseous species that are formed during heating are designated with \uparrow symbol and it means they drift apart.

After the introduction of carbon monoxide for nanowires growth (see following section) a reduction process of ferric oxide or nickel oxide takes place and it produces metallic iron or metallic nickel respectively through different reduction paths, depending on kinetics and thermodynamic conditions [209], [210].

Subsequently the metal forms an alloy with the silicon of the substrate and, after transformation into liquid phase, it creates a droplets array on the surface.

In semiconductor technology nickel silicides are finding increasing interest, therefore nickel diffusion in silicon is widely studied and it is possible to find many examples in literature of studies on this topic. The nickel diffusion through the bulk is faster than that on silicon surface and the transport to the surface is caused by the segregation when the solubility of nickel reduces owing to the temperature decrease. The shape and the state of the structures on surface is dependent on the cooling rate [211]. The observation of square-shaped island is typical for the segregation of nickel on (100) surface of silicon.

3.2 Growth of core-shell silicon carbide – silicon oxide nanowires

Core-shell SiC-SiO₂ were synthesized from carbon monoxide in vapour phase and silicon coming from the substrate. This method allow to obtain core-shell nanowires in an easy and cheap way and it has high yield, since the growth procedure is quite fast. The optical properties of the so-obtained nanostructure are peculiar because an enhancement of the core near-band-edge emission due to the presence of the amorphous silica shell has been demonstrated.

3.2.1 Experimental procedure

Experiments were carried out in an open tube reactor placed with a conventional horizontal tube furnace with a constant temperature region 10 cm long. (100) silicon was used as substrate as well as silicon source for the growth.

After catalyst deposition and drying (as explained in the previous section), the samples were placed in an open tube reactor purged with vacuum-nitrogen cycles to remove oxygen from the growth chamber.

The temperature was then raised to the synthesis setting (1100° C) and CO was provided under a constant flow ($4 \cdot 10^{-6}$ m³/s) for 30 minutes at atmospheric pressure in nitrogen carrier gas flow (Figure 3.5). Subsequently the sample was brought to ambient temperature during 10 minutes.

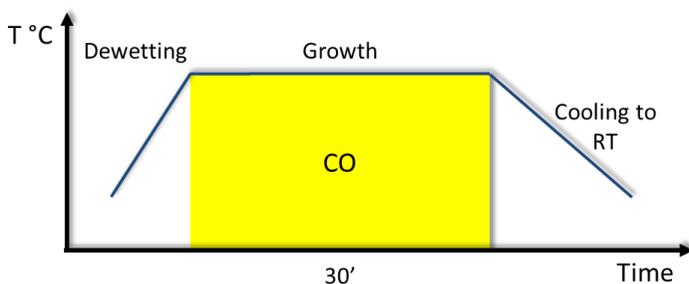


Figure 3.5: scheme of the growth procedure for obtaining SiC/SiO₂ core-shell nanowires. The dewetting procedure is as fast as possible and CO is introduced only when the growth temperature is reached.

The cool down was carried out in pure nitrogen without the presence of CO. After the cooling step, the sample was covered with a white coloured deposit indicating the presence of a dense wires network all over the surface.

Using gaseous CO as precursor instead of a solid state reaction between C and WO_3 as proposed by Park et al. [212] allowed a continuous control over CO flow, so the concentration during the growth, and prevented tungsten contamination inside the chamber.

3.3 Structural and compositional analysis

The shape of the wires is cylindrical, the average diameter is 60 nm and the length is more than 100 μm . From SEM observation it is possible to see the dense nanowire bundle forming a layer of about 100 μm on the substrate (Figure 3.6) the shape of the wires is curvilinear (Figure 3.7) but it is rare to spot abrupt folds.

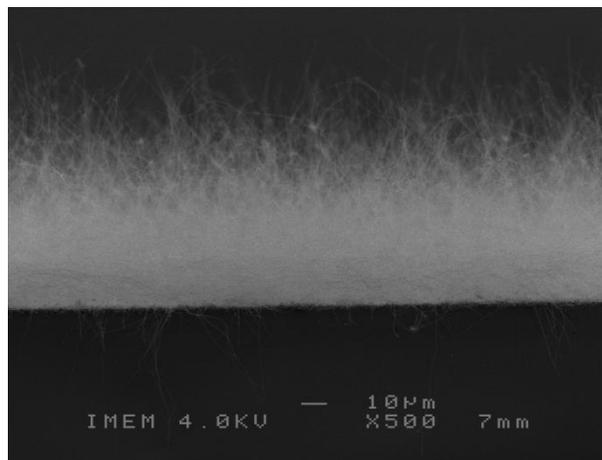


Figure 3.6: SEM cross-section image of a core-shell SiC/SiO₂ nanowires sample. The average length exceeds 100 μm .

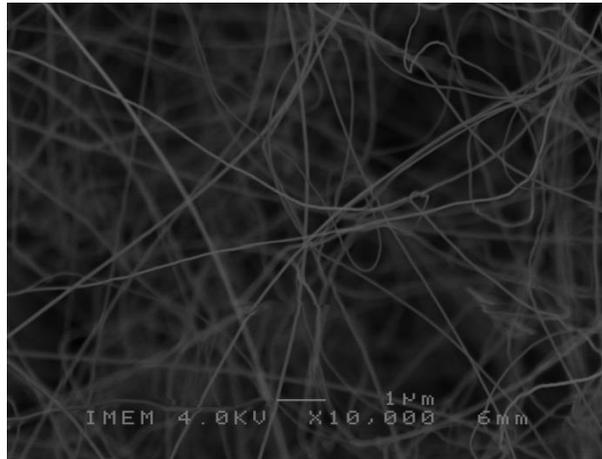


Figure 3.7: SEM top view of a typical core-shell SiC/SiO₂ nanowires sample

TEM analysis highlights the core-shell structure (Figure 3.8); the core is continuous along the whole wire without interruption and it is connected to the particle on the tip of the wire.

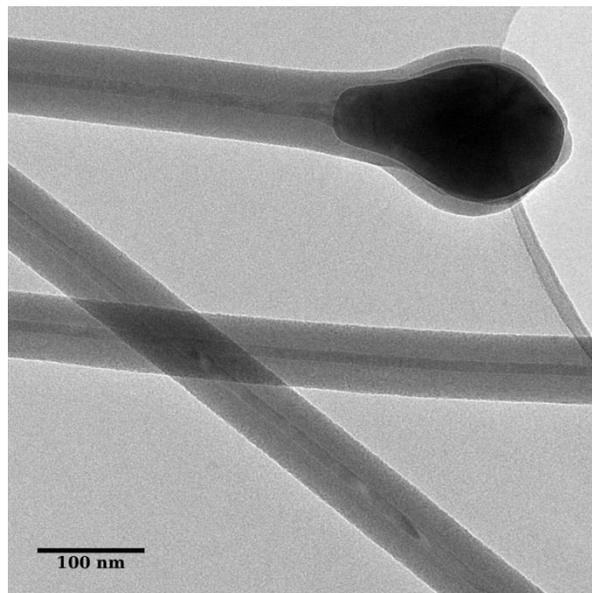


Figure 3.8: TEM image of three different nanowires. The core-shell structure is evident from contrast difference. All the wires end with a particle bigger than the wire diameter, as it is visible in upper part of the image.

The structure can be resolved by means of HRTEM (Figure 3.9): the shell has an amorphous structure, while the symmetry and lattice spacings of the crystalline core correspond to 3C-SiC, with $\langle 111 \rangle$ axis along the growth direction.

Quite long segments of the core are almost free of planar defects. In some other areas it is possible to observe the occurrence of (111) stacking faults with the manifestation of stacking sequences of 2H, 4H and 6H polytypes.

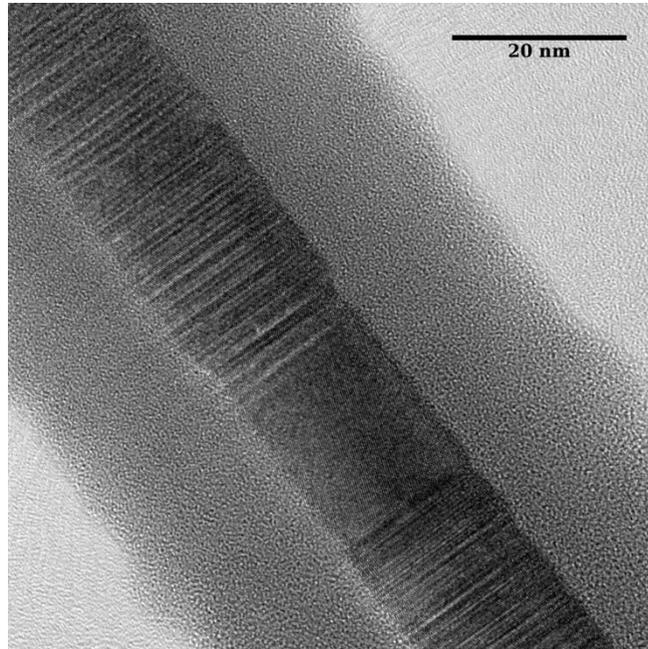


Figure 3.9: HRTEM image of a single wire. The area chosen for the image shows areas of the core with good crystalline quality near to planar defects

TEM-HAADF analysis (Figure 3.10 left) shows a confirmation of core-shell structure: this technique, called also z-contrast discriminate elements with different atomic numbers (Z) and highlights those with higher Z [213]. In this case it shows the presence of iron in the particle on the tip, suggesting a mechanism of so called “float growth” [99] kind.

TEM-EDX analysis (Figure 3.10 right) carried out on the particle reveals the presence of iron and silicon, this composition could suggest an iron-silicon alloy forming the particle.

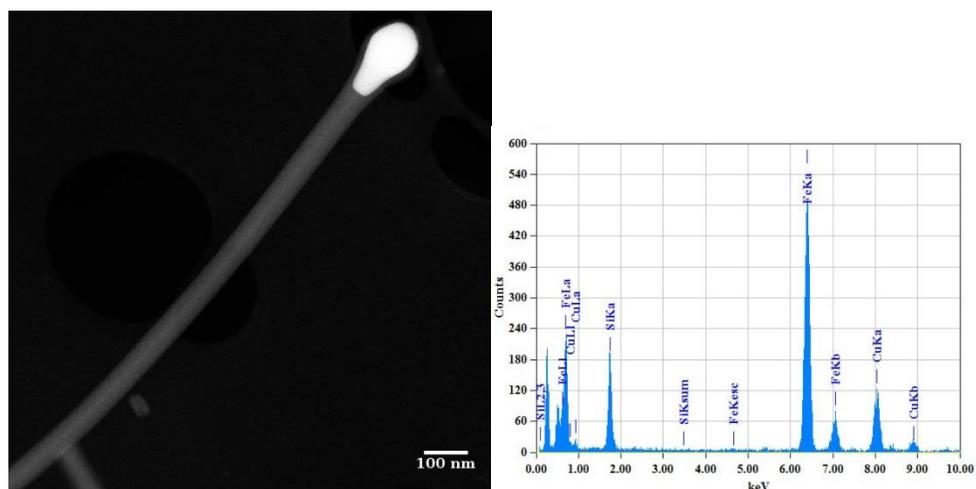


Figure 3.10: on the left: TEM-HAADF image of a core-shell nanowire. This imaging technique allows to identify elements with higher atomic weight, in this case, the particle on the tip of the wire is brighter because of the presence of iron. On the right: TEM-EDX spectrum of the tip particle. Peaks corresponding to iron and nickel presence are highlighted. Copper presence is ascribed to the use of a TEM copper grid as sample holder in the microscope.

The presence of a silicon carbide core and silicon oxide shell is confirmed by TEM-EDX elemental maps on the body of the nanowires (Figure 3.11). Carbon maps are more difficult to prepare since carbon and copper are commonly used for TEM sample holders. Special “holey” grids are consequently used and it is necessary to find wires positioned on the holes, since only on them EDX carbon detection will be reliable. The carbon density is higher in the SiC core, in contrast with the SiO₂ shell as expected, but carbon presence is evidenced also in the outer part of the shell. This may be due to contamination, but most probably it is a high carbon concentration in the silicon oxide outer layer. To better analyse the nature of this carbon presence please see XPS investigations in the following. Carbon doping can explain the reason why the silicon oxide shell is resistant to chemical etching with concentrated HF, a well-known etchant for silica. The silicon presence is confirmed in the whole radius of the wire, both in the silicon carbide (higher Si concentration) and silicon oxide. EDX analysis of light elements such as oxygen isn't possible with the apparatus used.

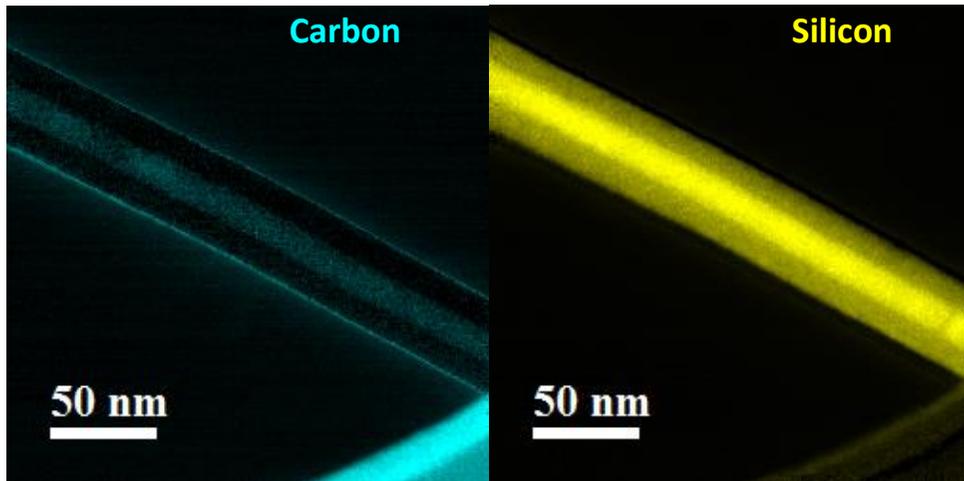


Figure 3.11: TEM-EDX elemental map of a core-shell nanowire. On the left, the carbon map highlights the SiC core, with high C concentration, in contrast with the SiO₂ shell. Silicon presence is detected both in the core and in the shell.

By varying growth parameters it is possible to achieve a certain control over nanowires structure and morphology, for example it was previously demonstrated that the carbon monoxide partial pressure in the reactor during the synthesis can have a direct influence over the core thickness. Figure 3.12 reports a TEM image of a typical wire synthesized with a smaller CO concentration (0,2%). In this sample the average core diameter is 12,7 nm, while in nanowires grown with 0,4 % CO concentration the average core diameter is 20,1 [137].

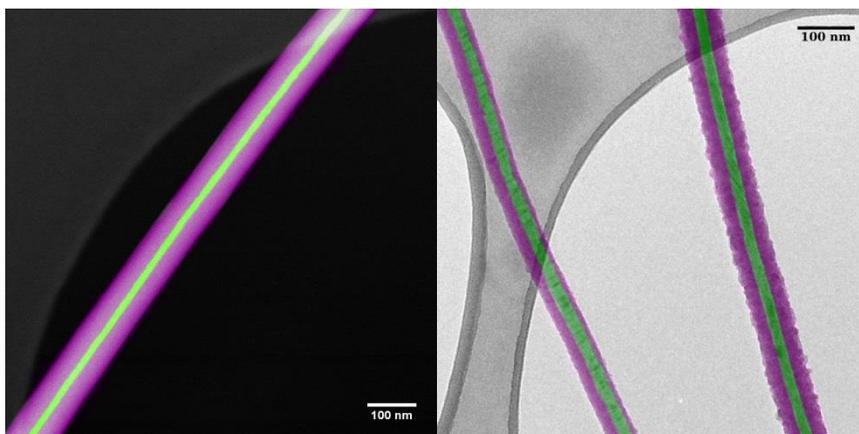


Figure 3.12: TEM images in false colours: SiO₂ shell is highlighted in violet, while SiC core is emphasized using green colour. On the left: STEM-HAADF image of a

core-shell nanowire obtained using low CO precursor concentration. On the right: TEM image two different wires of the same sample obtained using higher CO concentration. The average core diameter shows a strong dependence from growth conditions, in particular from CO concentration.

To deeply study the nanowires surface composition, XPS is a preferential technique, involving a few nanometres thick surface layer. Photoemission from core level of Si2p/C1s were analysed with photon energy at 250eV/400eV, respectively, in order to have the better and same surface sensitivity (about 2-3nm). The NWs have been previously etched using hydrofluoric acid in attempt to remove the thick silicon oxide shell, in order to enable the analysis also of the embedded SiC NW core. The Si2p peak broadening and the C1s double peak lineshape shown in Figure 3.13 a and b respectively, clearly reveals the presence of several chemical components. The detailed lineshape analysis reveals the SiC related components (blue peaks in Figure 3.13) Si_A and C_A, respectively at binding energies (BEs) of 101.0 eV and 283.3 eV, together with other features that can be generally ascribed to oxidized species. The Si_A-C_A energy distance is 182.3eV, compatible with the presence of a cubic SiC [214].

Regarding the Si2p core level analysis, the Si_B peak at 102.1eV falls into the typical BEs region of silicon oxycarbides [215], [216], while the Si_C peak at 103.0eV is related to silicon oxides. In order to better identify the in depth distribution of the different chemical species, we analysed the Si2p core level with a larger in-depth sensitivity of about 3-4nm using a 400eV photon (Figure 3.13 c). With respect to Figure 3.13a, features showing the same BE but different relative intensities are present (the higher width is due to the different photon used). As a rule of thumb, by increasing the in-depth sensitivity the more external layers are depleted while the more internal ones are enhanced. In our case, we are dealing with a SiC core surrounded by a silicon oxycarbides structure and, finally, and external very thin SiO_x layer. This also suggests that the HF chemical treatment has effectively etched only the more external shell, leaving a residual thin layer with a thickness $\leq 0.5\text{nm}$ on a $\leq 2\text{nm}$ thick silicon oxycarbide layer.

Regarding stoichiometry, the Si/C intensity ratio for the SiC components is 0.85 ± 0.05 , with a slight carbon excess, while the overall Si/C intensity ratio is 2.23 ± 0.30 , with a net silicon excess. This figures out an increasing silicon

concentration gradient going from the NW core towards the surface, as well as a higher carbon stoichiometry located around the oxycarbides/SiC interface.

Both the C_B/C_C peaks at 284.7eV/286.2eV can be ascribed to C1s emission in oxycarbides, typically located in a BE range of 285-289eV. However, the C_B component larger width suggests also the presence of sp^2 - sp^3 carbons aggregates, clusters, typically showing a C1s emission around 285eV. The wet chemical treatment did not remove this peak, evidencing that the carbon clusters are not surface contaminants. These carbon aggregates are responsible of the observed carbon excess, previously indeed located at the interface between the oxycarbide and the SiC layers.

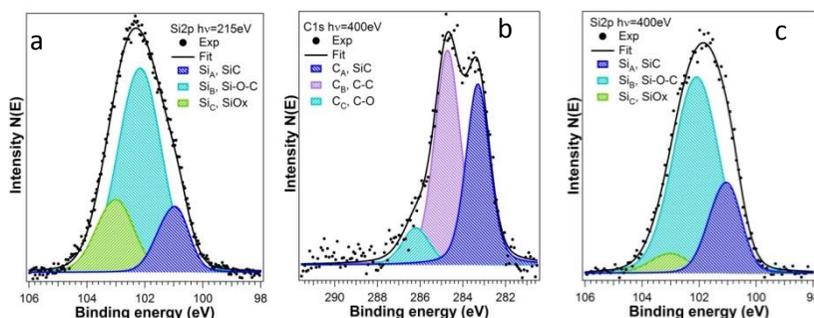


Figure 3.13: Core levels photoemission of Si2p (a, c) and C1s (b). Photon energies used are 215 eV(a) and 400 eV (b, c). Experimental data are shown as dots, the fit curves as black lines and the single deconvoluted components as colour areas.

3.3.1 Optical properties

The optical properties of the NWs, with and without the oxide shell, were studied by Cathodoluminescence (CL) spectroscopy. Figure 3.14 shows the comparison between typical room temperature CL spectra acquired on bundles of core/shell NWs (red curve in Figure 3.14) and SiC NWs (blue curve, x10 in Figure 3.14). The shell was removed with the procedure explained in the next section. The comparison highlights that the emission from SiC NWs is very faint and broad, whereas the core/shell structure favours a more efficient luminescence emission, with quite sharp peaks at 2.3 eV due to the near-band-edge (NBE) recombination in the cubic SiC core and at 2.7 eV related to the SiO_2 shell [217], [218].

To explain why the presence of the silicon dioxide shell increases the radiative recombination in the silicon carbide core, we can analyse the energy diagram of the nanosystem. A type I band alignment [219] of 3C-SiC and SiO₂ can be hypothesized (on the right of Figure 3.14). The conduction and valence band-offsets have been experimentally found in [96] in the case of bulk material and they are equal to $\Delta E_c = 3.6$ eV and $\Delta E_v = 2.9$ eV respectively. In this framework, the carriers generated by the electron beam in the shell diffuse into the core, and here recombine according to the allowed transitions in 3C-SiC. The diffusion of the carriers could be considered as an energy transfer from the shell to the core. In our system, the amorphous shell results to be beneficial to enhance the luminescence intensity of the crystalline core, preferentially the SiC NBE radiative recombination. Besides the effectiveness as a carrier injector region, this could be partly related to the fact that the shell can act as a passivation layer to reduce the non-radiative recombination related to surface states, likewise in the case of entirely crystalline core/shell systems (e.g. GaAs-based NWs [220]).

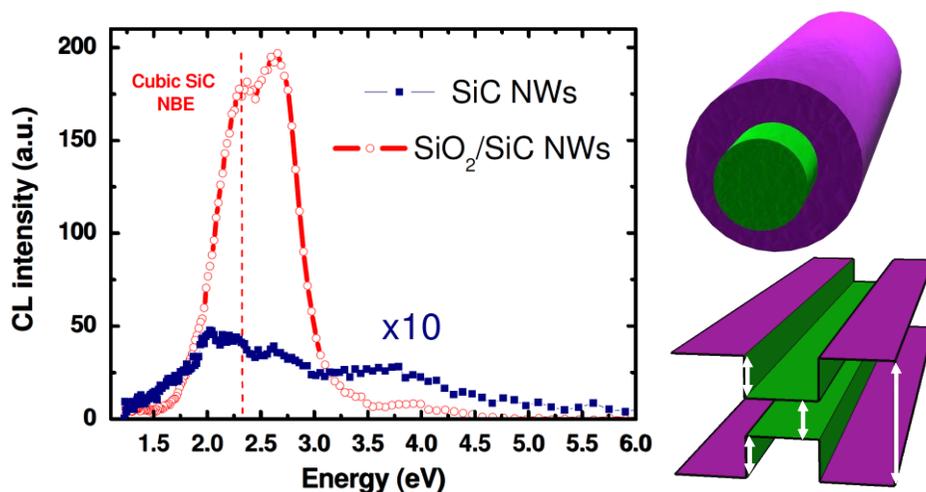


Figure 3.14: On the left: Cathodoluminescence spectra acquired at RT on core/shell nanowires (red circles) and SiC NWs (blue squares). On the right bottom: simplified diagram of the type I band alignment between 3C-SiC core (in green) and SiO₂ shell (in violet).

3.4 Carbon-doped SiO_x nanowires

Many materials have been used to obtain nanowires, among them, oxides are particularly promising owing to their biocompatibility and because they can be easily functionalized.

Silicon oxide optical fibres are widely used to transmit optical signal, but silica can act as optical waveguide also at nanometric level as demonstrated by Tong et al., who used subwavelength-diameter silica wires as low-loss waveguides within the visible to near-infrared spectral range [221] this is very interesting for future applications as high resolution optical heads in scanning near-field optical microscope probes. Studying the optical emission of silicon oxide would allow to integrate emission and transmission in the same material.

Strong efforts are currently devoted in looking for materials with white light emission but they are difficult to synthesize. Nevertheless SiO_x nanowires possess peculiar features such as intense light emission [222] and their electronic behaviour can vary widely from insulating to metallic depending on the number of Si-O bonds [223]. For these reasons they have been studied extensively for optic and optoelectronic devices and applications such as laser emitters, sensors and for semiconductor full-colour displays

The quest for the fabrication of light emitting compounds is well known even outside the research environment and nourished many studies in different fields. In particular, the replacement of white light phosphors is still challenging, because the highest emitting efficiency is still achieved using rare-earth based phosphors [224], [225]. The realization of Si-based compounds working as light emitters to replace white light phosphors would be a breakthrough in the field of display and lighting technologies. Recently, different studies have been devoted to looking for nanostructured materials with intense white light emission. In this field, different classes of SiO_x based nanostructures, as nanowires and nanoparticles, possess peculiar features such as a high emission yield [222], [226]. SiO_x nanostructures have promising opto-electronic properties for possible device applications e.g. in full-color displays, laser emitters, and chemo/bio sensors [227].

The same chemical vapour deposition reactor used to obtain core-shell SiC/SiO₂ nanowires proved to be highly adaptable and, changing the growth condition,

allowed us to obtain carbon-doped amorphous silicon oxide nanowires. These new nanostructures fostered our attention also because we could use the functionalization chemistry already developed by our group for core-shell SiC/SiO₂ nanowires [3]. Since the optical properties of SiO_x materials, both thin films and nanostructures, are mainly governed by defects, defect engineering allowed us to tune the light emission by changing the concentration of radiative centers.

3.4.1 Synthesis procedure

The CVD system described previously was used as reactor to fabricate silicon oxide nanowires on Si(100) substrates using nitrogen as carrier gas and carbon monoxide as dopant precursor. Nickel nitrate (Ni(NO₃)₂) was used as catalyst and a 0,01 M solution in ethanol was dispersed on a silicon substrate leaving the native oxide (\approx 1nm [228]) on the surface. A non-ionic surfactant was added to ensure an optimal catalyst distribution on the substrate (see previous section). The CVD synthesis was carried out at 1050°C for 45 min. After the growth, the sample was rapidly quenched in nitrogen gas and atmospheric pressure to ambient temperature. The carbon doping is most likely obtained due to the good diffusivity of CO in silicon dioxide, already reported by Krafcsik et al. [229].

3.4.2 Structural and compositional analysis

Figure 3.15 shows typical plan-view and cross-sectional **SEM** images of the as-grown SiO_x NWs. The nanowires, which are uniformly distributed over the entire substrate surface, have average tip size of about 200 nm (see size statistics in Figure 3.16, red bars), average diameter of a hundred nm (Figure 3.16, blue bars) and lengths of few tens of microns. The areal density of the NWs is evaluated as 2.3 ± 0.1 NWs/ μm^2 on the substrate surface. The fast Fourier transform (FFT) of the SE image (inset in Figure 3.15) reveals a one-fold growth with a preferential nanowires alignment.

Figure 3.17 shows a typical high-angle annular dark-field (**HAADF**) **STEM** image of a single NW. It is known that the HAADF intensity is proportional to the atomic number (Z) of the elements present in the sample [213], therefore any intensity contrast at constant thickness can be related to a Z contrast. While the intensity

does not vary along the wire length, indicating that the NW body is homogeneous, a sudden contrast is set at the tip. The presence of a bright particle at the tip is indicative of a root-growth mechanism (see section 1.7.1), catalyzed by nickel. Electron diffraction patterns (not shown here) confirm the NW bodies are amorphous. Compositional analyses were carried out by acquiring energy-filtered TEM images of the NWs supported on holey-carbon grids: silicon (from Si L edge) and oxygen (from O K edge) maps did not show any inhomogeneity, while carbon maps (from C K edge, see Figure 3.17 on the right) showed a weak signal spread over the NW body and the presence of a few aggregates, in particular near the outer surface. This reveals the formation of small amorphous carbon-rich clusters inside the SiO_x NWs.

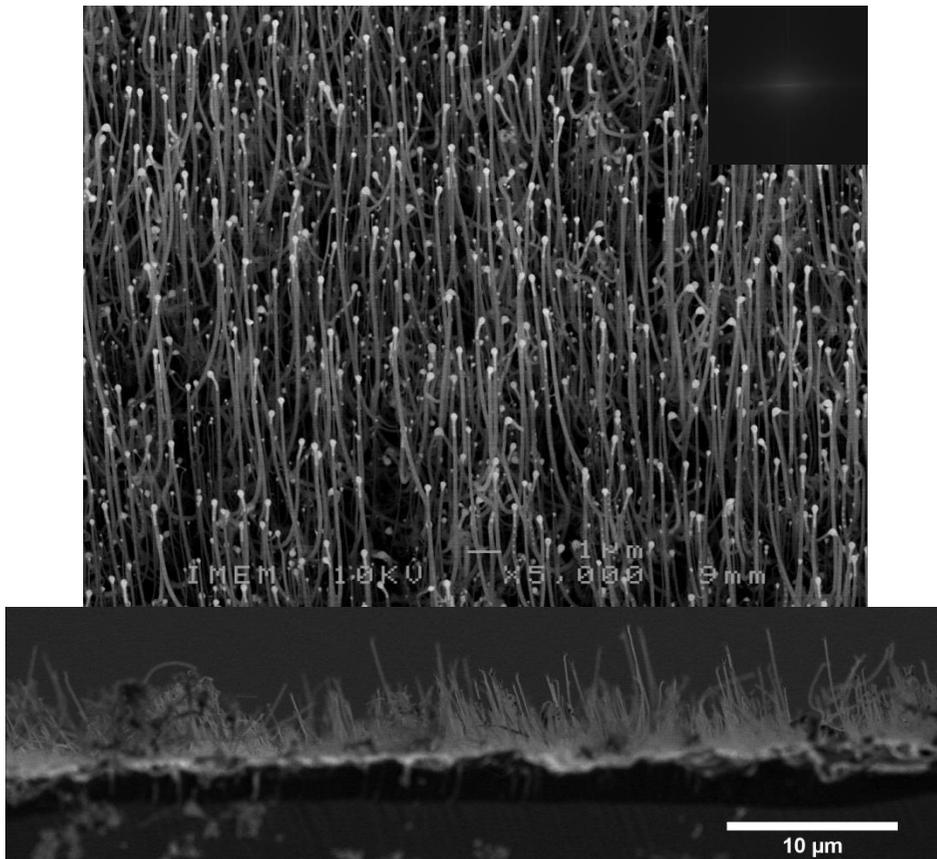


Figure 3.15: Top: SEM secondary electron image of the as-grown carbon doped nanowires sample. In the inset the fast Fourier transform of the image shows a

preferential growth direction. Bottom: Cross-sectional SEM image of the same sample evidences the nanowires alignment.

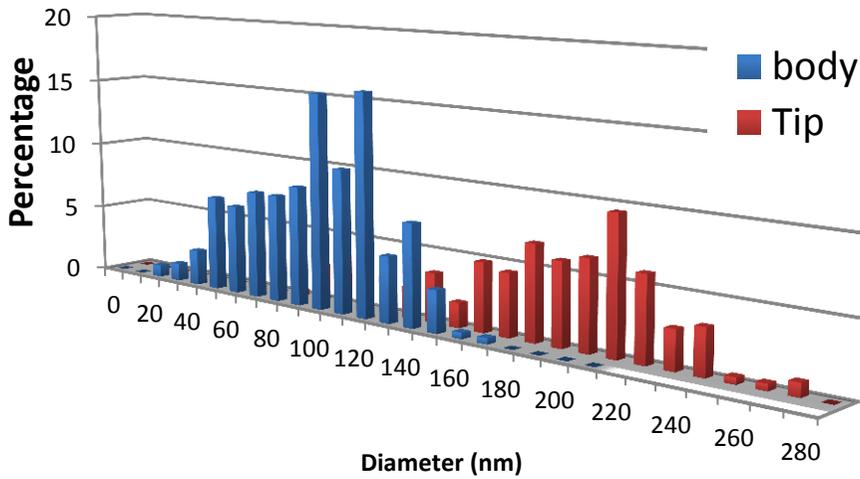


Figure 3.16: statistical distribution of nanowires body (blue) and tip (red) diameters.

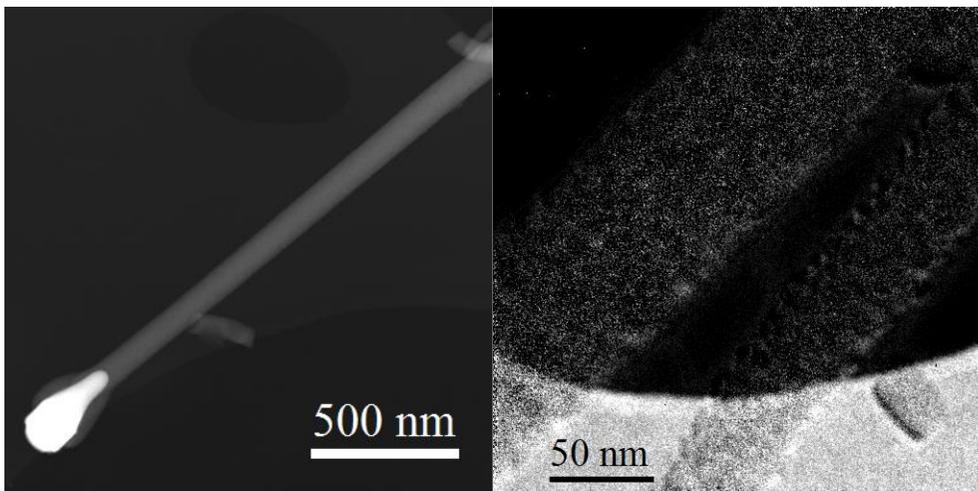


Figure 3.17: On the left: STEM-HAADF image of a silicon oxide nanowire. The particle on the tip contains high-Z elements, so it is brighter in HAADF image. On the right: Carbon map obtained with energy filtered TEM. The map is taken on two wires lying close together across a hole of the holey carbon support film.

X-ray photoemission spectroscopy (XPS) was performed ex-situ in a UHV apparatus for surface electron spectroscopy. The Mg-K α emission at 1253.6 eV was used as x-ray source while the photoelectrons were analysed by a PSP-Vacuum Technology electron energy analyser, leading to a total energy resolution of 0.1 eV. Spectra were acquired at low (pass energy PE=50 eV) and high resolution (PE=10 eV) to characterize the whole surface and the C 1s, O 1s and Si 2p peaks. To remove carbon contaminants, samples were cleaned in an ultrasonic bath of trichloroethylene, acetone and final isopropyl alcohol before the introduction into the analysis chamber. Then they were **outgassed** in UHV to remove unwanted species from the surface and analysed with x-rays. To check whether the carbon phase is located on the surface or deeper in the NW shell, the samples were also **sputtered** with an ion-gun sputtering facility (ions energy at 1 keV; raster 5x5 mm²).

Figure 3.18 shows the low resolution spectra of outgassed and sputtered samples, which highlights the presence of carbon, oxygen and silicon together with a small contribute from nickel, detectable only after sputtering.

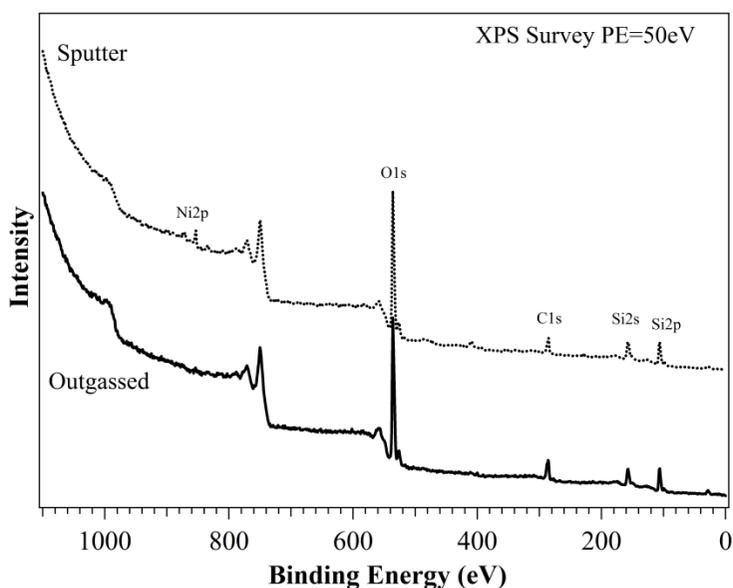


Figure 3.18: XPS survey spectra of silicon oxide nanowires sample after outgassing only (on the bottom) and after outgassing and sputtering (on the top).

High resolution spectra of carbon, oxygen and silicon are reported in Figure 3.19. The fitting procedure has been performed by subtracting Shirley background, then applying Voigt functions with a Lorentzian to Gaussian ratio of 0.3 while uncertainty on binding energy (BE) position is ± 0.05 eV. For all core levels, the experimental curve cannot be fitted by a single peak. The lineshape evolution for C1s, as the sputtering is performed, shows a slight energy shift towards lower BE and a strong reduction of the components at high BE. Two main structures are present that indicate an overall shift of the NW-related components (red peaks in Figure 3b) with respect to substrate peaks (in black), due to charging phenomena at the surface during measurements. The same charging-related shift is observed for O1s and Si2p spectra and it is quantifiable in 3-4 eV. After sputtering, the O1s spectrum shows a slight increase of the shoulder at low BE, while for Si2p there is a clear growth of the Si-Si peak at 99.5 eV; an indication that we are uncovering both the substrate and NW surface.

For C1s we can identify (see Table 3.1) three shifted components related to the NWs (NW1; NW2; NW3) and three unshifted components related to the substrate (Sub1; Sub2; Sub3): Sub1 and NW1 are the main components. Sub1 in particular is at 285.24 eV and can be assigned to species characterized by C-C bonds, typically unreacted and adventitious carbon on the substrate. Sub3 is at higher BE and can be assigned to C-O bonds, again related to contaminants, while Sub2 is at lower BE and falls into a BE region characterized by Si-C bonds, likely a by-product of the reaction [218]. NW1 can be defined in analogy to Sub1 as the fingerprint of C-C bonds, either embedded on the NWs or not. NW3 lays at higher BE with respect to NW1 and can be assigned to C-O or Si-C-O bonds (typically oxycarbides [230]). NW2 is at the same energy difference between Sub1 and Sub2, thus we can reasonably assign it to carbides in the NW shell. The same components can be found for the sputtered samples, but their intensity shows some variations, helping us in defining the distributions of C-C, Si-O-C, Si-C and Si-O compounds from the outer part of the shell towards the core.

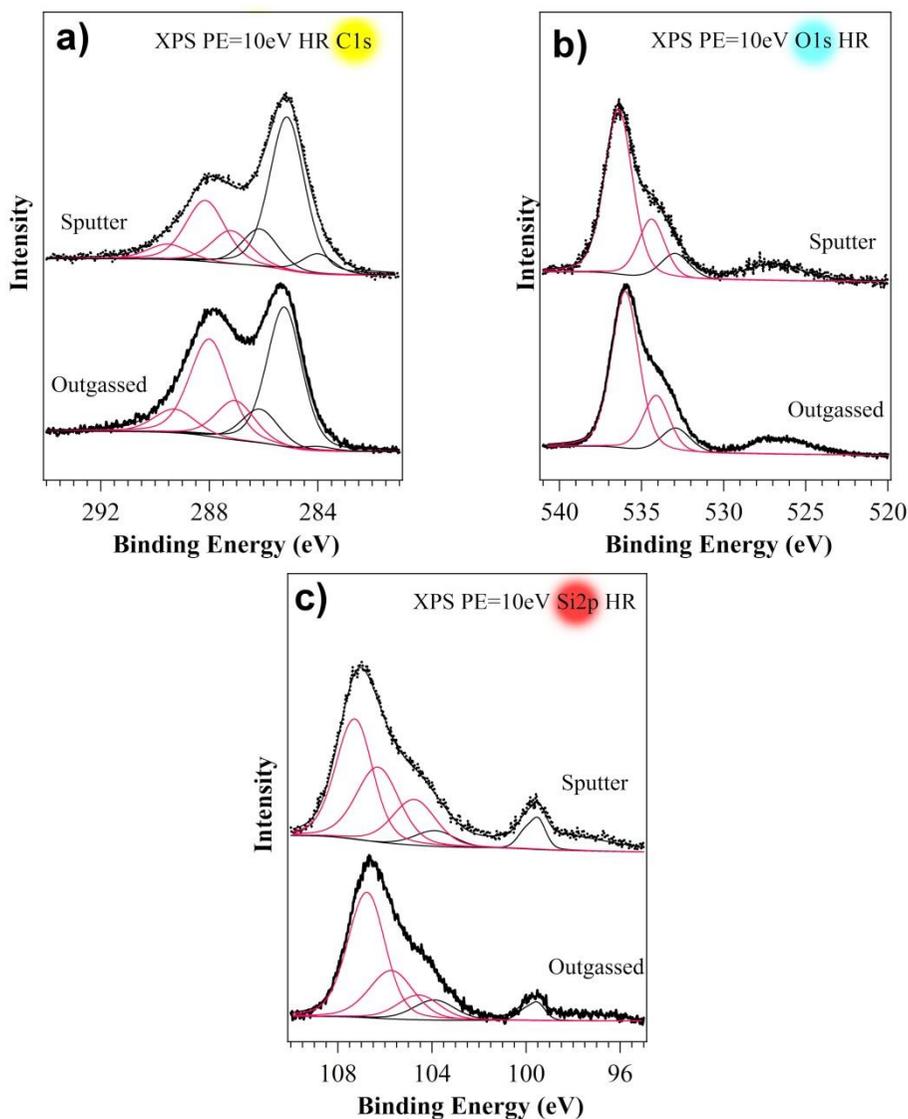


Figure 3.19: a) C1s, b) O1s and c) Si2p high resolution (HR) XPS spectra. Red peaks represent the NW-related components, found after deconvolution. Charging phenomena originated by the insulating nature of the NWs produce the extra binding energy shifts, found for all the core levels.

Si2p lineshape analysis puts in evidence up to four contributions for the NW and two for the substrate. We observed the typical Si-Si peak at 99.5 eV followed by its oxide at 103.7 eV [231], while for the NW we have a main peak at high BE, due to SiO_x (where x is close to 1.4) and other peaks at lower BEs with respect to the

main peak. One peak is the shifted Si-C contribution at 104.37 eV and 104.57 eV for outgassed and sputtered sample respectively, while the peak at about -1 eV from the main peak can be assigned to oxycarbides, already identified in the C1s lineshape. A fourth peak has to be introduced to reproduce the lineshape maintaining the stoichiometry of the other components. This peak appears only for the sputtered sample and can be assigned to the interaction between silicon oxides and nickel/nickel oxides.

Table 3.1: Peak positions of C1s and Si2p contributions resulting from lineshape analysis

Sample	Outgassed	Sputtered	Sample	Outgassed	Sputtered
Component	C1s BE (eV)	C1s BE (eV)	Component	Si2p BE (eV)	Si2p BE(eV)
NW1	288.00	288.15	NW Si-O oxy	106.62	107.08
NW2	287.00	287.20	NW Si-O- C	105.67	106.05
NW3	289.29	289.53	NW Si-C	104.37	104.57
Sub1	285.24	285.14	NW NiO- SiO	--	106.20
Sub2	284.00	284.00	Sub Si-Si	99.51	99.48
Sub3	286.14	286.14	Sub Si-O oxy	103.71	103.68

The atomic composition of the surface (NW, Substrate and Total signal from the sample) is reported in Table 3.2 for the outgassed and sputtered surface. After the sputtering procedure, the overall XPS signal is lower. All the NW related C1s components decrease, but the Si-C component ratio to C-C component is higher, while the NW2/NW1 ratio remains unchanged: a possible interpretation is that the carbide species lie in the inner part of the NWs while oxycarbides and carbon “dopants” are in the outer shell. The NW1 components do not disappear completely after sputtering thus we can conclude that there is a part embedded into the outer shell. The Si-C component proportionally increases also for the Si2p peak, and the same is observed for the Si-Si peak. We are removing carbon

contamination from both the substrate and the NWs and accordingly we observe more carbides compounds at the substrate surface and nickel compounds on the NW top; an observation supported by the introduction of the fourth component into the Si2p peak. No variation is observed for the oxide components both in O1s and Si2p peaks, in agreement with C1s, another indication that the oxycarbides are present in the outer NW shell.

Table 3.2: Atomic composition of the surface (NW, substrate and total signal from the sample)

	Outgassed sample				Sputtered sample			
	C 1s	O 1s	Si 2p	Ni 2p	C 1s	O 1s	Si 2p	Ni 2p
NW	13.46	50.78	35.76	0.00	7.53	51.94	39.44	1.09
Substrate	52.08	25.72	22.21	0.00	48.17	24.63	20.89	0.00
TOT	21.3	45.7	33.0	0.00	16.3	46.8	36.0	0.87

3.4.3 Optical properties

Auger electron spectroscopy (AES) was performed in the same apparatus used for XPS to check the surface composition before and after sputtering. AES was operated using an electron beam at 3 keV and constant retard ratio (CRR) of 10 leading to an emitted sample current of 100 nA. The AES analysis has brought an interesting evidence. When the electron beam is operated on the sample surface, an intense white luminescence suddenly appears, and this luminescence decreases as the electron beam current is lowered. The luminescence appears weaker as the electron beam spot is widened, resulting in a lower current density at the surface. Figure 4a shows the NWs sample in the UHV analysis chamber under the electron beam operated at 3 keV and small spot size. The white spot at the image centre is the cathodoluminescence coming from the interaction between the NWs and the electron beam used in the AES experiments, which is strong enough to be visible from outside the analysis chamber and photographed.

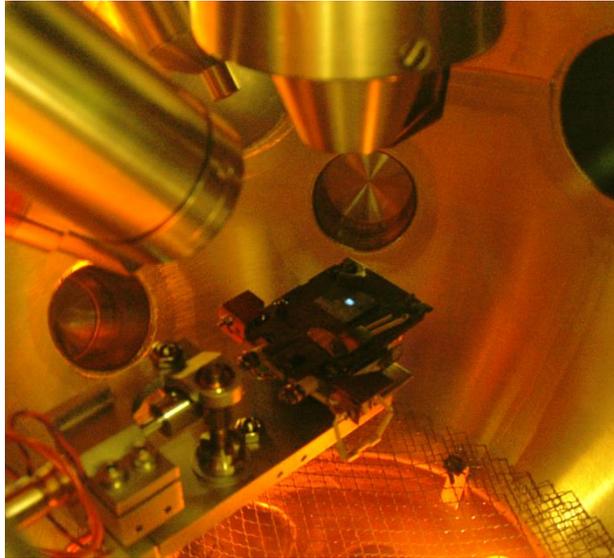


Figure 3.20: photo taken during AES analysis: the white cathodoluminescence emission of the sample under electron irradiation in the UHV chamber is visible in the centre.

To deeply analyse the optical emission spectrum of the nanowires, **cathodoluminescence** measurement were carried out in a SEM. Figure 3.21 shows the typical CL spectrum of a NW bundle. The spectrum is a complex broad band ranging from 3.0 eV to 1.7 eV. Accurate fitting procedure allows us to define the different peaks that compose the spectrum. It is worth noting that the spectrum features are peaked at 2.7 eV, 2.3 eV and 1.9 eV, i.e. a blue, green and red emission, respectively. These can be ascribed to the following point defects of the amorphous silicon oxide:

- the oxygen-deficiency center, ODC II, ($\equiv\text{Si-Si}\equiv$), responsible for the blue component [232].
- the carbon doping, responsible for the green component [233].
- the non-bridging oxygen hole center, NBOHC, ($\equiv\text{Si-O}^*$) responsible for the red component [232], [234].

The sharp peak at about 2.0 eV is probably related to amorphous carbon, likely from the carbon-rich outer layer found by XPS as discussed above, as reported by references [235], [236]. Concerning the green emission, different attributions have been suggested in literature. A 2.3 eV emission has been found in

amorphous silicon dioxide thin films at low temperatures ($T < 200$ K) and attributed to self-trapped excitons (STE) luminescence [237]. The SiO_2 STE emission energy is an open issue, and, to the best of our knowledge, no studies about the relationship between stoichiometry and STE emission are reported in literature. Moreover, some authors set the STE energy at about 2.8 eV, typically the position for crystalline silica [238], even in case of amorphous silica nanoparticles, claiming that the position of the STE is the same in the case of amorphous and crystalline SiO_2 [226]. Considering these contradictory results and a number of previous works where undoped silica NWs or under-stoichiometric silicon oxide NWs present only blue and red luminescence [222], [239], [240], without reporting any emission in the green range, the 2.3 eV emission in our samples is most likely related to carbon doping.

In addition it is possible to propose a possible coordination of the carbon atoms in the host lattice. Previous work, concerning carbon isoelectronic dopant (as germanium [232]), reports that the germanium atoms form a cluster with a particular coordination $\equiv\text{Ge}-\text{Ge}\equiv$. These small clusters are responsible for the 3.1-3.2 eV emission, typically reported for germanium doped silica. It is possible to propose a similar coordination for carbon dopant atoms, in agreement with the observation of carbon-rich clusters by energy-filtered TEM.

It is worth noting that the concurrent presence of both the 2.7 eV and 1.9 eV emissions, i.e. the ODCII centre (oxygen deficiency) and the NBOHC (oxygen excess), in the CL spectra suggests a gradient of concentration of oxygen. The XPS analysis suggests that this gradient is radial. This effect could be due to an impoverishment in oxygen of the surface with respect to the body of the NWs.

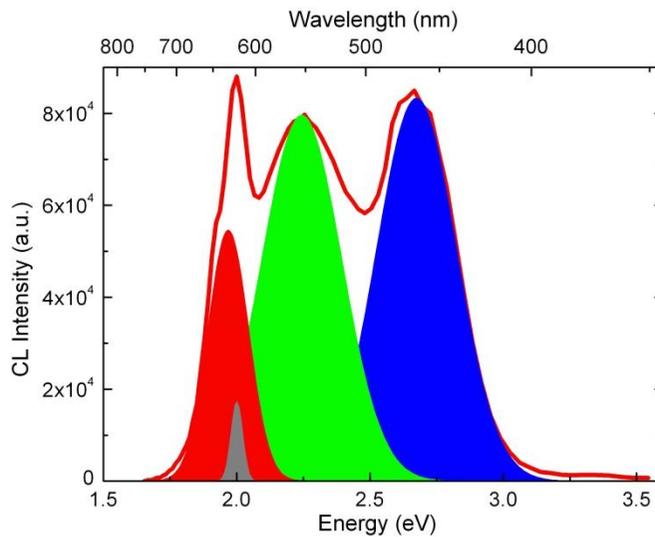


Figure 3.21: SEM-CL spectrum taken at room temperature of the carbon-doped silicon oxide nanowires. The Gaussian deconvolution highlights the different components in the red, green and blue range.

3.5 Processing the core-shell nanowires

To study the conductivity and carrier density in semiconducting nanowires the first achievement is to contact them. In addition to the well-known issues of contacts on semiconductors explained in section 1.4, to contact nano-sized objects requires a high precision in depositing metallic contacts and extremely low currents to perform the electrical characterization. What is routine on a bulk semiconductor often becomes an issue when speaking of nanosized objects.

3.5.1 Chemical etching

In order to perform electrical measurements on the nanowires, it was essential to remove the insulating silicon oxide shell. As previously described, the high carbon content in the silicon oxide of the core-shell nanowires prevents the hydrofluoric acid etching of the shell. As a consequence, a complex chemical procedure was developed in order to remove the shell.

A standard RCA clean followed by a second chemical treatment with Piranha solution and final etching ($\text{HCl}:\text{H}_2\text{O}$ 2:1 and $\text{H}_2\text{O}:\text{HF}$ 50:1) was found to be the right processing sequence to remove the carbon-doped silica. The chemically-etched NWs resulted in almost bare 3C-SiC, with a sub-nanometric residual coating.

TEM images evidence the difference after the treatment: in Figure 3.22 a comparison between an as-grown sample and after chemical etching is reported. Bright field TEM images of the sample (on the right of Figure 3.22) show nanowires with reduced diameter and almost complete removal of the shell. High resolution TEM studies (Figure 3.22 right inset) highlight a residual amorphous layer. This film, whose thickness is below one nanometer, is most probably made of silicon oxycarbide compounds, which are resistant to the etching procedure. The average diameter calculated from several SEM images (not reported here) of the as-grown core-shell nanowires is 66,2 nm, while the average diameter is reduced after etching up to 21,5 nm, as calculated from the SEM image reported in Figure 3.23.

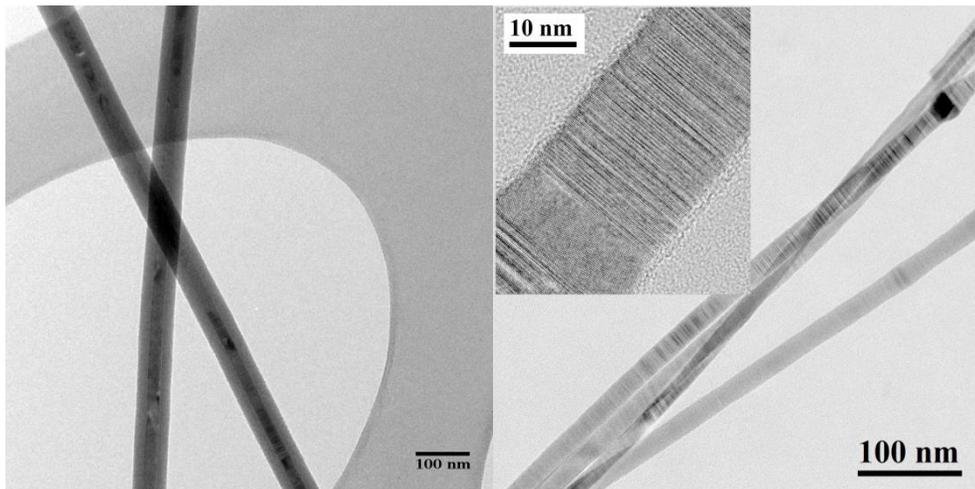


Figure 3.22: On the left: zero-loss energy-filtered transmission electron microscopy (EFTEM) of two typical core-shell SiC/SiO₂ nanowires. On the right: bright-field TEM image of same kind of nanowires after chemical etching, resulting in almost bare 3C-SiC. A HRTEM image of a nanowire is reported in the inset, showing a thin residual amorphous surface layer.

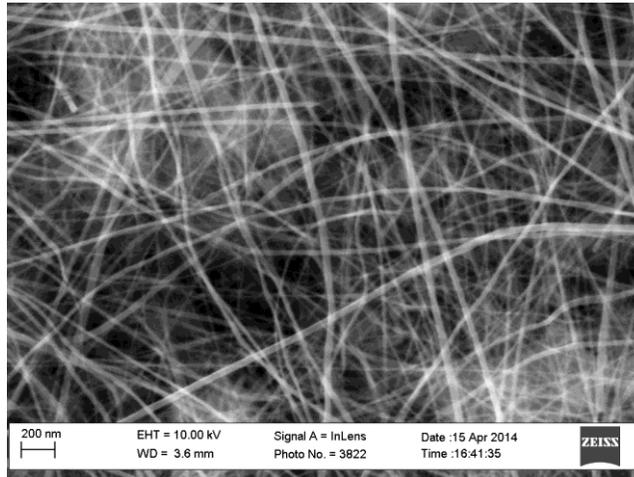


Figure 3.23: SEM image of the chemically etched nanowires.

3.5.2 Contacting the nanowires

Dielectrophoresis [241] has proven to be a valid method to position the nanowires even on 4 probes contact geometries [242], direct placement of a single nanowire can be achieved using a FIB-assisted nanomanipulator [243], but the use of interdigitated contacts (IDCs) allows to obtain multiple contacts on a single wire simply dispersing randomly a liquid solution containing the nanowires.

In order to remove the nanowires from the substrate, the sample was immersed in Isopropyl alcohol and then put in a ultrasonic bath for few seconds. The nanowires solution was then dropped onto a suitable substrate. Aluminium IDC on an insulating silicon oxide layer was used as substrate. After a random dispersion, some wires will be statistically crossing a number of contacts. Figure 3.24 shows SEM images of the nanowires dispersed on IDC: the nanowires length ($\approx 100 \mu\text{m}$) ensures good probabilities of contacting the nanowires in multiple points.

The electrical conductivity was tested on the as-deposited nanowires: the resistance between two IDC without the wires and with the wires on them was compared. No resistance difference was measured, that means that no contact was formed between the metal and the nanowires. Annealing in hydrogen atmosphere was tried in order to improve the contact: the sample was put in

hydrogen at ambient pressure and the temperature of 600° was kept for 30 minutes. After the annealing the electrical measurements confirmed that still no electrical contact was formed, therefore, we decided to deposit metal on the nanowires to contact them to the IDC beneath.

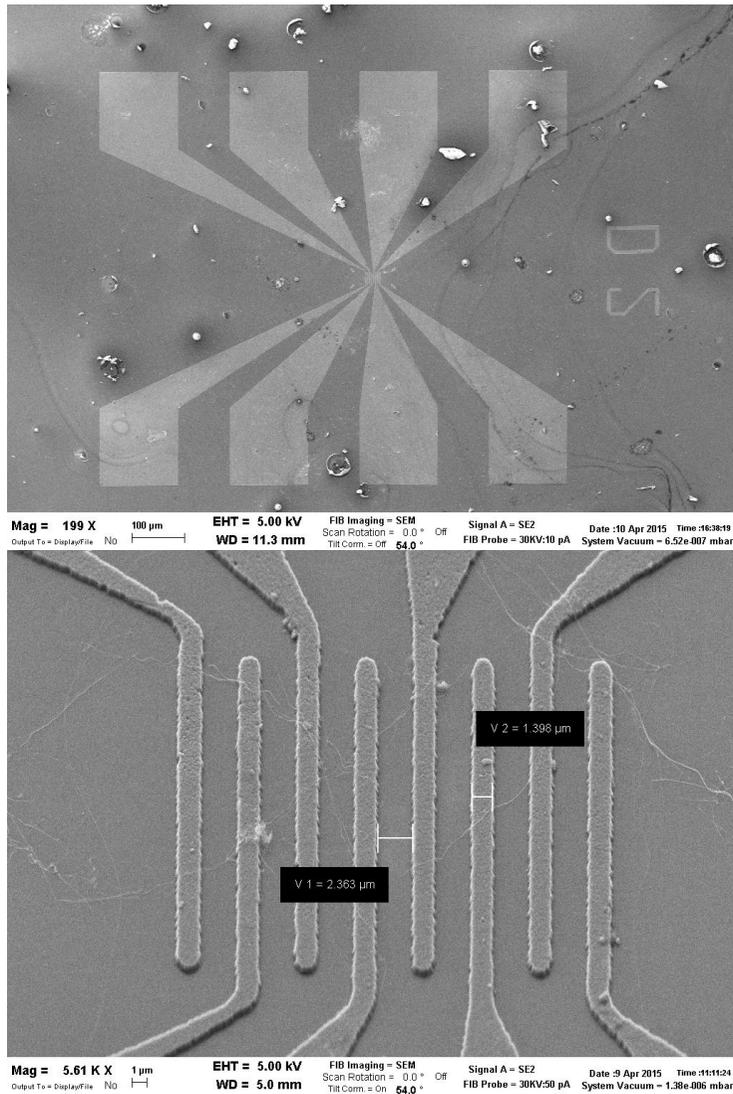


Figure 3.24: SEM BE images of the bare 3C-SiC nanowires deposited on interdigitated aluminium contacts. On top: low magnification view of the contacts. On the bottom: detail of the centre. It is possible to identify the wires deposited. The gap between contacts and contact width is 2,4 μm and 1,4 μm, respectively.

The most precise methods to obtain contacts on single nanostructures are electron beam lithography (EBL) and electron or ion beam induced deposition. Chronologically, the first method used has been EBL, which consist in drawing customized shapes on a surface covered by an electron-sensitive film using a focused beam of electrons. While expensive dedicated systems are used in commercial applications, the scanning electron beam is most frequently the one of a SEM in research applications. Metal deposition followed by resist deposition and patterning by EBL is though a long process and with many problems. Polymethyl-methacrylate is often used as resist, but it is difficult to locate the nanostructures underneath the film and this results in misalignment. Incomplete lift-off of the resist is eventually a recurrent cause of poor yield. Direct-write patterning allows to avoid these problems and this is the reason for the diffusion of the electron and ion beam induced deposition techniques to contact semiconductor nanostructures in research applications.

An organo-metallic precursor is introduced into the SEM chamber and it can be decomposed by the electron beam or the ion beam. The result is a localized deposition of a metal-rich material on the sample surface. In other words, the process can be defined as a localized chemical vapour deposition, using ions/electrons energy to initiate the chemical reaction that brings to the deposition. For this reason the technique is also known as focussed ion beam chemical vapour deposition (FIB-CVD), focussed ion beam induced deposition (FIBID) or electron beam induced deposition (EBID) if the deposition is promoted by an electron beam. The products of the reaction are the deposited metal plus other remaining species that are generally volatile and can be removed from the vacuum chamber by the vacuum pump. Many metals such as Pt, W, Al and Au have been deposited using this technique. For a more complete dissertation on this topic we suggest reading Tseng [244].

We decided to deposit platinum because a Pt source was available in our FIB/SEM system and platinum contacts have already been studied on 3C-SiC (see section 1.4). We tried both EBID and FIBID and we noticed immediately some differences. Figure 3.25 reports the SEM image of two adjacent contacts obtained by EBID and FIBID with the same deposition time. It is worth noting that FIBID is much faster than EBID. Literature reports say that the ion beam deposition rate is approximately 10 times the electron beam deposition rate [245]. It is difficult to

make a quantitative and precise comparison because the beam parameters (energy, dimension, etc.) are different, so we report a qualitative description.

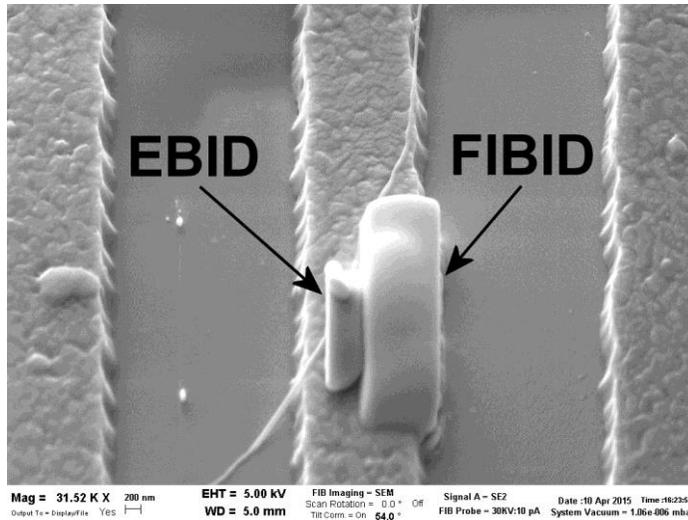


Figure 3.25: SEM image of platinum contacts deposited on a single 3C-SiC nanowire: on the left scanning electron beam induced deposition (EBID), while on the right focused ion beam induced deposition (FIBID) with 70 seconds deposition time.

The deposited material was characterised in other works [245] and is reported to be an amorphous carbon matrix with nanocrystalline platinum grains embedded in it[245]. FIBID material has a higher Pt contents and this results in a lower contact resistance after annealing. Unfortunately the spread of deposited material outside the designed area is a well-known issue of both techniques. Probably, the heating induced by the beam enhances the surface mobility of the decomposed species leading to the distribution of platinum several micrometres beyond the beam raster area [245]. This leads to a leakage current between closely spaced deposited contacts. This problem is less pronounced with FIBID, but in contrast the heavy ions (typically Ga⁺) damage the nanostructures to be contacted.

We decided to use EBID to deposit platinum contacts on nanowires because we could achieve smaller contacts and also with a lower height. We needed small contacts in order not to deposit outside the IDC and low contacts because this would facilitate AFM characterization. In addition to that, damages are produced

on nanostructures by the ion beam, as explained previously, while using EBID avoids this issue.

In Figure 3.26 a SEM image of the platinum contacts on a nanowire obtained using EBID is reported. Some platinum deposition outside the contacts is also visible. In the image obtained using backscattered electrons detector, the platinum, being a heavier element, gives a brighter contrast. The contacts were numbered from left to right for reference, as it is shown in Figure 3.26.

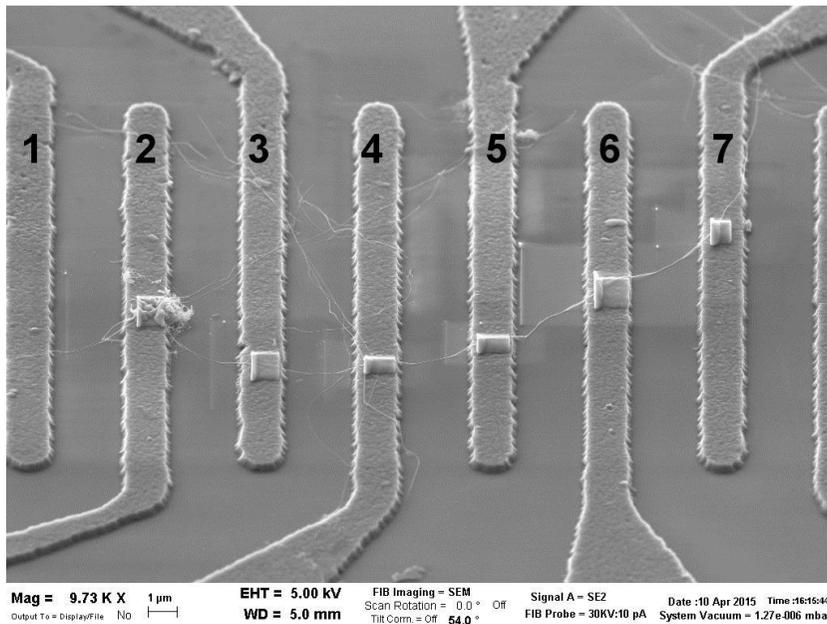


Figure 3.26: SEM backscattered electrons image of platinum contacts deposited onto a 3C-SiC nanowire. The IDC are numbered from left to right.

The electrical measurements were performed on as-deposited EBID contacts and the resistance was too high, outside instrument detection limit. We decided to perform an annealing in reducing atmosphere to avoid any oxidation. An effective annealing procedure was found to be 600° for 30 minutes in 200 mbar hydrogen atmosphere. The electrical measurement was then repeated and the contact behaviour was completely changed. Still between contacts 3 and 4 an extremely high resistance was found, probably due to a crack in the nanowire. The current-voltage characteristic was measured between IDC 7-6, 7-5, 7-4 and it is reported in Figure 3.27. The slope of the current-voltage characteristic corresponds to the conductance of the circuit, so the data was fitted with linear equations and the

inverse of the slope (resistance) was plotted as a function of the distance (Figure 3.28). The linear resistance was found to be about 500 K Ω / μ m.

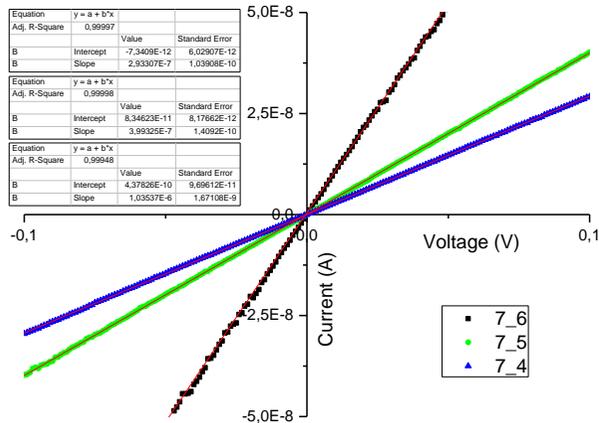


Figure 3.27: Current–voltage characteristic between contact 7 and 6, 5, 4. Linear fits of the curves are reported in red. The conductance (curve slope) decrease with the distance, as expected.

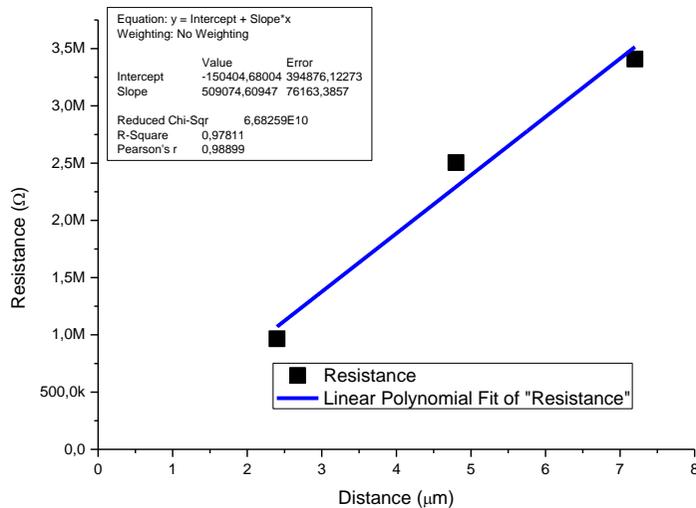


Figure 3.28: resistance (inverse of the slope of the i-V curve) is plotted as function of the distance (in micrometres). A linear fit is calculated and plotted as a blue line. The distances were calculated removing the contacts widths.

This method is the equivalent of transmission line measurement (TLM) used for planar electric measurements in semiconductor physics [246], [247]. The

technique requires making a series of metal-semiconductor contacts separated by different distances. Probes are applied to a pair of contacts at once and the resistance is measured. The overall resistance is a sum of the contact resistance of the first contact plus the contact resistance of the second contact plus the sheet resistance of the semiconductor. By varying the contacts distance it is possible to vary only the last variable (sheet resistance of the semiconductor). If the contact resistances of the different contacts are similar this method allows to decouple and calculate contact resistance and the linear resistance of the semiconductor. For TLM method see [247].

According to these measurements the contact resistance was negligible (intercept of the curve in Figure 3.28 with y axis).

If we take into account the average diameter (20 nm), it is possible to calculate the resistivity to be $1,6 \cdot 10^{-2} \Omega \cdot \text{cm}$.

We tried to do a rough estimation of the carrier density in the nanowires using the simplified relation between conductivity and mobility.

$$\sigma = ne\mu_e \quad 3.2$$

Where σ is the conductivity, n is the carrier density, e is the elementary electric charge and μ_e is the electron mobility. We supposed that the wires were n doped, since 3C-SiC is unintentionally n-doped (see section 1.5) and these nanowires were grown in nitrogen atmosphere, which is a n-doping element for 3C-SiC.

Assuming the same mobility measured for bulk 3C-SiC (See section 1.1) $\mu_e=1000 \text{ cm}^2/(\text{V}\cdot\text{s})$ would be incorrect. Owing to the high defect density in 3C-SiC nanowires, the measured mobility in literature is much lower: 15-16 $\text{cm}^2/(\text{V}\cdot\text{s})$ [146], [147]. Using this value it is possible to calculate a carrier density of $2.44 \cdot 10^{19} \text{ cm}^{-3}$. This high value, together with the estimation of an extremely low contact resistance brought us to think that there was a methodological error. We thought that the current was passing across a percolating path in the platinum that was spread between the contacts and decorating the nanowire. This phenomenon has already been observed in literature [248] and it is a well-known issue of EBID, as explained previously.

We decided to repeat the contact deposition with a limited deposition time (15 seconds) and using high magnification so that the objective lens could thin the beam and avoid platinum dispersion outside the IDC area. The result is shown in Figure 3.29: in the backscattered electrons image it is still possible to locate some spreading of platinum, but sensibly less than in the previous case. Two wires were contacted in parallel between IDC6, IDC7 and IDC8, while a single wire was contacted between IDC 3 and 6.

The electrical measurements were carried out between IDC3 and another contact between IDC 4 and 8, to repeat a sort of TLM as previously explained. In addition to that, the presence of two wires connected in parallel, allowed to perform an additional check.

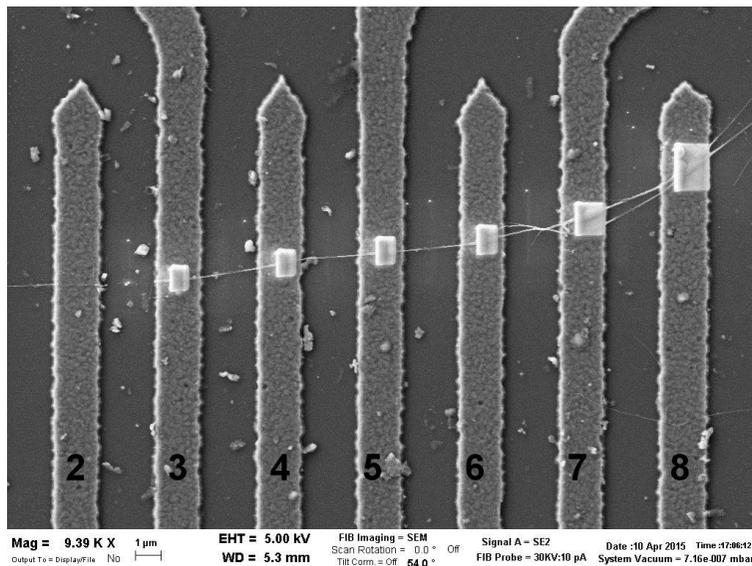


Figure 3.29: SEM backscattered electrons image of EBID platinum deposition on a 3C-SiC nanowire placed on IDC. Pt contacts obtained with a shorter deposition time (15 seconds).

In Figure 3.30 the current-voltage characteristics measured between IDC3 and the others IDC are reported. The characteristics are less linear than in the case previously explained, this means that the contacts are partially rectifying. This fact is a hint that the contact resistance on the wires this time plays a role in the total measurement. The slope of the curves, corresponding to the conductance, decreases with increasing distance.

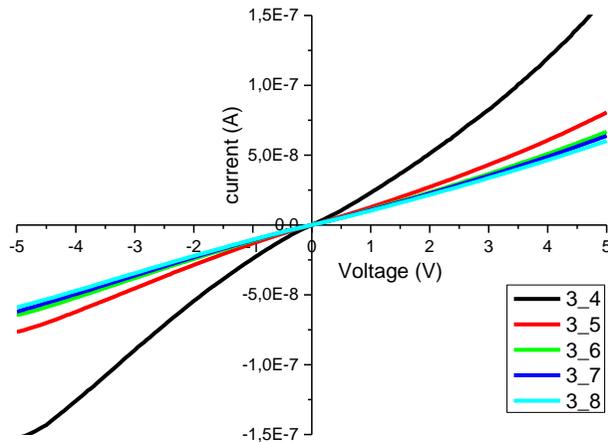


Figure 3.30: Current-voltage characteristics of measurements carried out between IDC3 and IDC 4, 5, 6, 7, 8.

Fitting the curves in Figure 3.30 with linear equations and taking the slope of the fit equations gives the conductance between the contacts. Plotting the inverse of the conductance vs. the distance between contacts brings to graph shown in Figure 3.31.

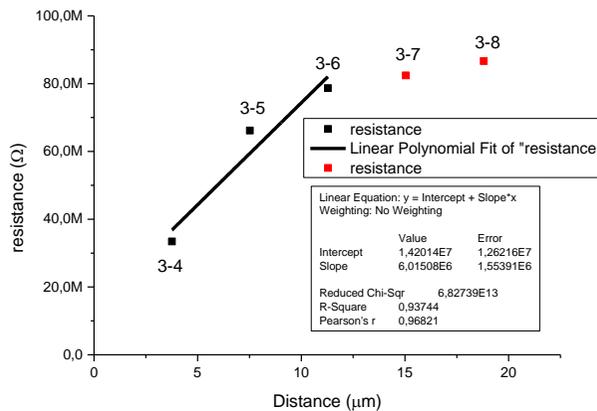


Figure 3.31: Resistance in ohm is plotted as a function of distance in this graph. The numbers reported on the dots are the IDC used to obtain the single measure. Red numbers indicate measurements carried out on two wires in parallel. Red dots represent measurements concerning two wires in parallel.

Taking into account only measurements concerning a single wire (black dots in Figure 3.31), the contact resistance is estimated to be $1,42 \cdot 10^7 \Omega$ (there are two contact resistance in series) and the wire linear resistance is $6,01 \cdot 10^6 \Omega/\mu\text{m}$. This corresponds to a resistivity of $0,189 \Omega\text{-cm}$.

In order to include measurements regarding the two wires in parallel (IDC6,7,8) it is necessary to think of the equivalent circuit. If we assume that the contact resistance between the two nanowires in parallel is zero (e.g. the wires are touching each other under the platinum contacts) and all the current is passing through the wire even when the wire is under platinum contact (e.g. the contact resistances are much higher than the wire linear resistance) the equivalent circuit is presented in Figure 3.32. The contact can be not completely ohmic and, as a consequence the contact resistance can be different depending on the current flow direction.

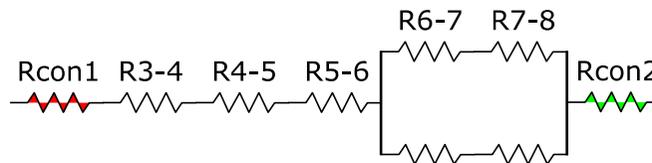


Figure 3.32: Simple equivalent circuit assuming that there is no contact resistance between the two nanowires in parallel and that all the current is always passing through the wire.

If also the contact resistances between the two wires in parallel are reported in the equivalent circuit the result would be as in Figure 3.33.

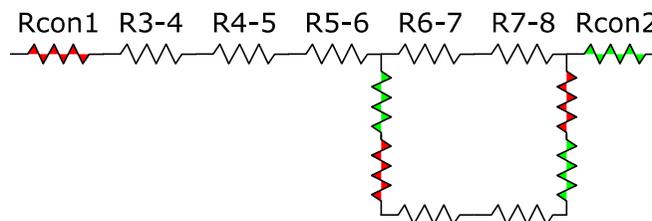


Figure 3.33: equivalent circuit taking into account the contact resistance between the two wires.

Eventually, if the contact resistance is smaller or comparable with the linear resistance one should insert in the equivalent circuit two contact resistances between each and every nanowire segment and the equivalent circuit would be composed of 27 different resistances.

Using the equivalent circuit in Figure 3.32 and assuming that the linear resistances of the two wires in parallel are similar, it is possible to calculate the resistance of a single wire simply doubling the resistance of the two wires in parallel. The result is shown in Figure 3.34. Fitting with a linear equation all the data points gives a linear resistance of $3,78 \cdot 10^6 \Omega/\mu\text{m}$ and a contact resistance of $2,91 \cdot 10^7 \Omega$.

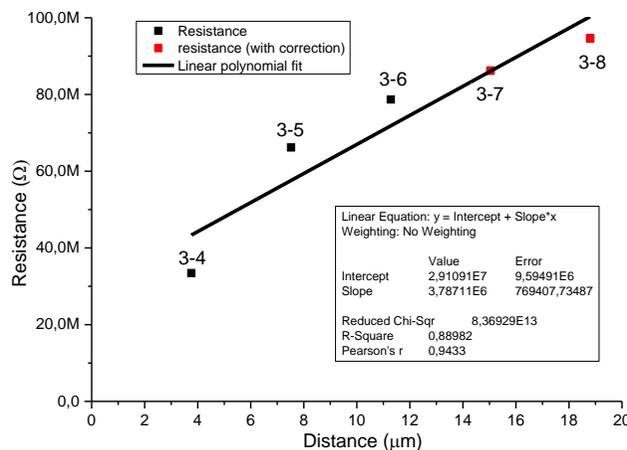


Figure 3.34: Resistance vs. distance plot correcting the values of 6-7 and 7-8 on the base of equivalent circuit in **Figure 3.32**.

The corresponding resistivity (calculated for a wire $1 \mu\text{m}$ long and with 20nm diameter) is $0,119 \Omega \cdot \text{cm}$. If we use this value for equation 3.2 we obtain an estimation of the carrier density to be $3,28 \cdot 10^{18} \text{cm}^{-3}$. These results confirm that a more circumscribed platinum deposition limits the decoration of the contacted nanowires and, as a consequence, the measured resistivity is lower. This method can be a valid choice for an estimation of the carrier density, but to confirm the results a FET fabricated with the nanowire would be needed (see section 1.7.2). In particular, these measurements could provide information on the electron/holes mobility of the material. The high thickness of the oxide beneath ($40\mu\text{m}$) prevented to perform the measurements, so future work will be dedicated to repeat the experiment with a thinner insulating oxide film and the same methods

and procedures developed for the experiments illustrated previously can be employed for this purpose.

3.5.3 AFM measurements on a single nanowire

Nanowires were deposited with the same method on substrates with trenches in order to have suspended segments. The aim was to locate the nanowire with an AFM tip and to test the mechanical and piezoresistive or piezoelectric properties.

Bare 3C-SiC nanowires were deposited successfully and were located using SEM first. Pt contacts were deposited using the electron beam deposition technique previously explained.

After placing the sample in AFM, it was possible to locate the nanowires with the aid of SEM images and the tip scan was set to be perpendicular to the nanowire axis. Topographic images are shown in Figure 3.35. It was possible to bend the nanowire, for this reason the apparent nanowire diameter was larger when the nanowire was suspended, while the real shape appeared in areas where the NW was laying on the sample surface.

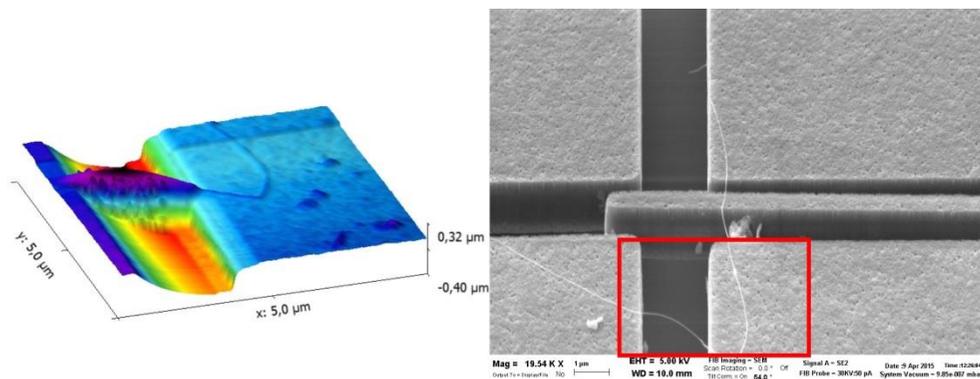


Figure 3.35: On the left: AFM topographic image of a nanowire suspended on a trench. On the right: SEM image of the same area (AFM scan area highlighted in red).

This experiment demonstrated a high flexibility of the nanowire, but unfortunately high electrostatic charges prevented any piezoresistive or piezoelectric measurements.

Conclusions

The present thesis has been devoted to the synthesis and investigation of functional properties of silicon carbide thin films and nanowires. The work took advantage from the previous experience of the IMEM-CNR research group in the synthesis of 3C-SiC from vapour phase [174], [249]–[251].

3C-SiC thin films

Thin films heteroepitaxy on silicon substrates was carried out in a vapour phase epitaxy reactor. The initial efforts were committed to the process development in order to enhance the crystal quality of the 3C-SiC epi-layer. The carbonization process and a buffer layer procedure were optimized in order to obtain high quality monocrystalline 3C-SiC layers. The films characterization was used not only to improve the entire process, but also to assess the crystalline quality and to identify defects presence and typology.

Methyltrichlorosilane (MTS) was introduced during the synthesis process to increase the growth rate and enhance crystalline quality. The effect of synthesis parameters such as MTS flow and growth temperature is studied in order to promote defect density reduction and the release of the strain due to lattice mismatch between 3C-SiC and silicon substrate.

In-growth n-type doping was implemented using a nitrogen gas line and the effect of different synthesis parameters on doping level was studied. Raman spectroscopic investigations allowed a contactless characterization and evaluation of electrically active dopant. The effect of MTS on nitrogen incorporation was investigated and an enhancement of dopant concentration together with a higher growth rate were demonstrated. These result demonstrates an higher doping concentrations without deteriorating crystal quality in 3C-SiC and, to the best of our knowledge, it has never been demonstrated before.

State-of-the-art wet chemical micromachining techniques were employed to etch the silicon substrate in order to produce 3C-SiC membranes. The use of custom designed silicon carbide masks, previously never reported to the best of our knowledge, proved to be effective for KOH and HNA etching solutions. A

comparison of the three most diffused wet etching techniques was carried out on the silicon substrate and the SiC membranes fabrication was demonstrated. Raman spectroscopy proved to be an excellent technique to characterize in real time the stress present in the 3C-SiC thin film. The stress calculation and measurement is of great importance for MEMS fabrication, altering the mechanical response of the micro/nano structures. Moreover, the evaluation of the stress can be of great help in future investigations on piezoresistive properties of the material. The precise on-site correlation between stress and piezoresistive or piezoelectric properties in cubic silicon carbide is a well-known issue that has some tangible possibility to be solved with this approach.

3C-SiC nanowires

Core-shell SiC-SiO₂ nanowires were synthesized using a chemical vapour deposition technique in an open tube configuration reactor on silicon substrates. Metal catalyst were used to promote an uniaxial growth and a dense bundle of nanowires 100 μm long and 60 nm thick was obtained. Substrate preparation was found to be fundamental in order to obtain a uniform nanowire density. Morphological characterization was carried out using scanning electron microscopy and the analysis of structural, compositional, optical by means of transmission electron microscopy reveals how the core-shell structure influences the optical emission properties of the nanowires. The variation of synthesis parameters allowed to obtain two different structures: self-assembled core-shell SiC-SiO₂ nanowires and carbon doped silicon oxide nanowires. Furthermore, an intense white emission from carbon doped silica nanowires was demonstrated during this work. The nanowires were synthesized with a good vertical alignment and the carbon doping proved to be effective in tailoring the optical properties. Cathodoluminescence technique was used to identify the origin of the three main optical emission centres, giving origin to a quasi-white spectrum.

The last part of the work was devoted to the development of processing techniques on the core-shell SiC/SiO₂ nanowires in order to perform electrical characterization measurements. A series of chemical etching processes were carried out to remove the silicon oxide / silicon oxycarbide shell. It was then possible to directly contact the single SiC nanowire after a chemical etch of the insulating layer. The best technique was found to be electron beam induced metal

deposition. After initial tries it was found that platinum from the contact deposition was decorating the nanowires and interfering with the electrical measurements. The deposition technique was improved and more circumscribed platinum contacts proved to be effective to measure nanowires resistivity and to estimate the carrier concentration. In more ambitious efforts, this technique allows to fabricate a single nanowire based field emission transistor by contacting SiC nanowires on interdigitated contacts. This will allow to fully characterize the electrical properties in view of the integration of these biocompatible nanostructures in biomedical devices.

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Acknowledgements

During the three years PhD concluded here I have been working mainly in team. Collaborations allowed to reach many achievements, people was kind enough to teach me, sacrificing work time for explanations. When I went to people's office they gave me a chair and they dedicated time. Even the smoke time was a good chance offered (to a non-smoker) for projects, explanations, advices. In a country with great potentialities but that seems to lose interest in scientific research, things can change thanks to people that sacrifices time and efforts to transmit the passion for research.

First of all I would like to express my gratitude to my supervisor **Giancarlo Salviati**, for believing in me and for his support through this path. "Leader" in the real meaning. Thanks also to **Giovanni Attolini** for his patient guidance and support. "Mentor", as the Odyssey character, rigorous in research and as life talent. Both of them transmitted me two different positive aptitudes to research.

Thanks to **Matteo Bosi**, working in close contact with me and really always there when I needed anything. "Trainer" in lab life, quick, direct, showed me how to get the things done.

I would like to thank **Laurent Montès**, that opened me the doors of his lab beyond the alps. Cordial, kind and friendly from the beginning, I really felt like at home.

Thanks to **Paola Lagonegro**, working, discussing, laughing together, bringing happiness to the group. "Colleague" comes from Latin: *cum legare*: delegated together and accomplice.

A great deal of appreciation is owed to **Filippo Fabbri**, volcanic and captivating. "Instructor", who built a scientist above me (at least he tried).

Many thanks to **Francesca Rossi**, precise, pragmatic, for her courtesy and willingness. "Allied" who helped me each time I asked. Her desk is the Oval Office of the group, where we decided all the strategies.

Many thanks to **Cesare Frigeri** for his patience and availability. I know he won't like public appreciations like these, but I want to say that I was lucky to work with him.

It is difficult for the universe to contain the kindness of **Enos Gombia**. His office door is broken, but I know that it isn't the only reason for being always open for everyone. "Teacher": in Latin *insignare* means to leave a mark.

Many thanks to **Marco Calicchio** for his precious assistance. His work was always careful and precise.

Thanks to **Tiziano Rimoldi** for his versatile help, kindness and helpful observations.

I'm also obliged to **Davide Orsi** for his willingness. "Zen". From him I could learn to control my anger in front of bad luck in everyday work.

Luigi Cristofolini gave valuable suggestions in many topics, raising thoughtful questions. Happy to teach, a lot to learn.

Antonella Parisini shares her gentleness with you. Always available and always passionate about her work.

Marco Gorni learnt his attitude from his former and present tutors. You know that going downstairs you will find him there, anytime. You ask, Marco answers and explains.

Giacomo Baldi finds natural to be willing and kind. Thanks to his accurate work we discovered together the possibilities of a new scientific instrument.

Giuseppe Tarabella and **Pasquale d'Angelo** for their ideas, helpfulness and will to try. They explained me different research topics and taught me from scratch.

Ran Tao: her perseverance and patience were really useful during long measurements.

Edwige Bano, always, always kind and friendly, encouraging me each time I met her.

Thanks to **Elisa Bonnini**, **Elisa Buffagni** and **Claudio Ferrari** for their precious help to be "oriented" in the diffraction universe.

With **Francesco Boschi** I like to think that is a quite rare case of real knowledge exchange. I learnt, he learnt.

Many other People not only from Imem institute collaborated with me during these three years period: **Lucrezia Aversa**, **Tullo Besagni**, **Manuele Bettelli**, **Maurizio Culiolo**, **Davide Delmonte**, **Rosella Magno**, **Francesco Mezzadri**, **Agostino Romeo**, **Greta Rosa**, **Roberta Tatti**, **Roberto Verucchi**, **Marco Villani**. I apologise if I forgot someone.

Many thanks to PEDforPV and Signal groups for letting me use the instruments in their charge.

As "last names in the article authors list" I would like to thank **Luca Ascari**, who thought of the project, together with **Salvatore Iannotta**. As G.K. Chesterton said: "You can only find truth with logic if you have already found truth without it".

Up to here I acknowledged the people who helped directly during the PhD work, but my gratitude goes also to the people that have shared this period with me. Without their support this work wouldn't have been possible.

First of all thanks to my family: my parents **Carla** and **Pierluigi** who have always been at my side with unconditional love. Their uninterrupted support and encouragement was essential. All my close family: my sister **Francesca**, my grandfather **Carlo** and **Vittorina**, my cousins, uncles... great family!

Thanks to **Caterina**, thinking that so many years we are side by side and we sustain each other. More ups than downs, thanks to her, thanks to the confidence in each other.

Thanks to all the people that accompanied me during this period in work time:

Filippo, Giacomo, Silvio, Elisa, Francesco, Matteo, Nicola, Nicola, Maurizio, Lucia, Davide, Paolo, Andrea, Fabio, Paola, Sathish, Sophia, Aldo, Agostino, Greta, Enzo, Marco, Nicola

...and in life:

Valentina, Stefano, Rossella, Tilla, Anna, Annamaria, Jolanda, Marco, Chiara, Alessandro, Andrea, Federica, Luca, Laura, Mirco, Cristina, Francesca, Gabriele, Cristina, Cristian, Alessandro, Cosimo, ...